

NXP BUK964R2-80E TrenchMOS datasheet

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Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

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BUK964R2-80E

N-channel TrenchMOS logic level FET

13 March 2014

Product data sheet

1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{gs(th)}$ rating of greater than 0.5V at 175 °C

3. Applications

- 12V, 24V and 48V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	[1]	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	349	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 11	-	3.4	4.2	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; V_{DS} = 64\text{ V};$ Fig. 13; Fig. 14	-	37.5	-	nC

[1] Continuous current is limited by package.

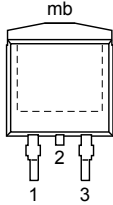
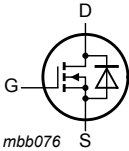


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK964R2-80E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK964R2-80E	BUK964R2-80E

8. Limiting values

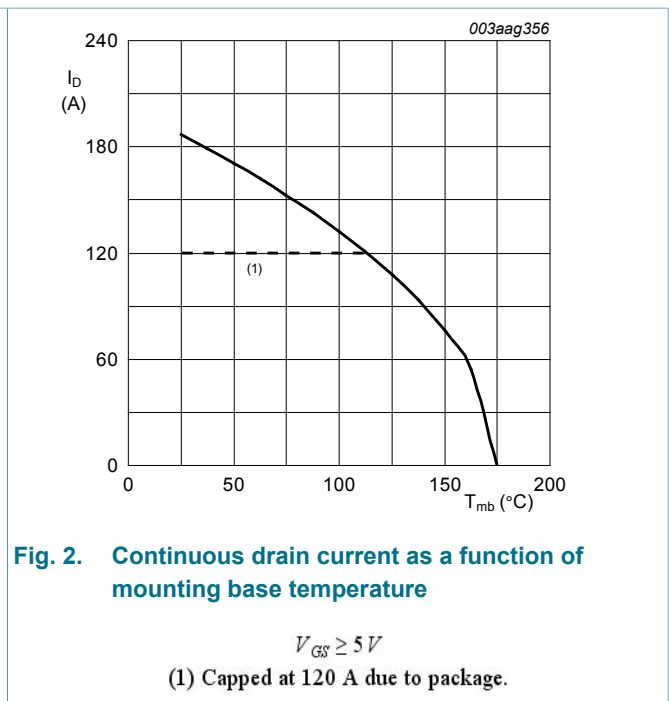
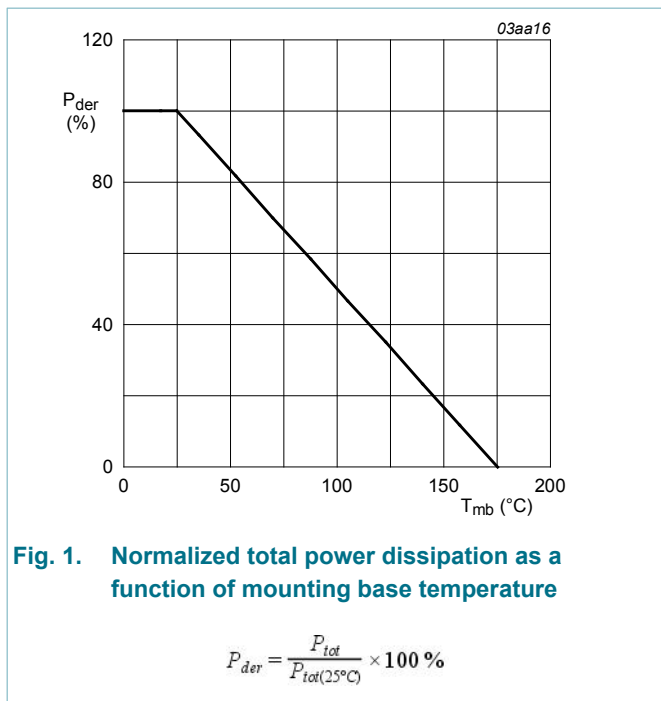
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$	-	80	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ }^\circ\text{C}$; DC	-10	10	V
		$T_j \leq 175\text{ }^\circ\text{C}$; Pulsed	[1][2]	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	349	W
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	120	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3	-	732	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	732	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[4][5]	-	485	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and/or V_{GS}
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



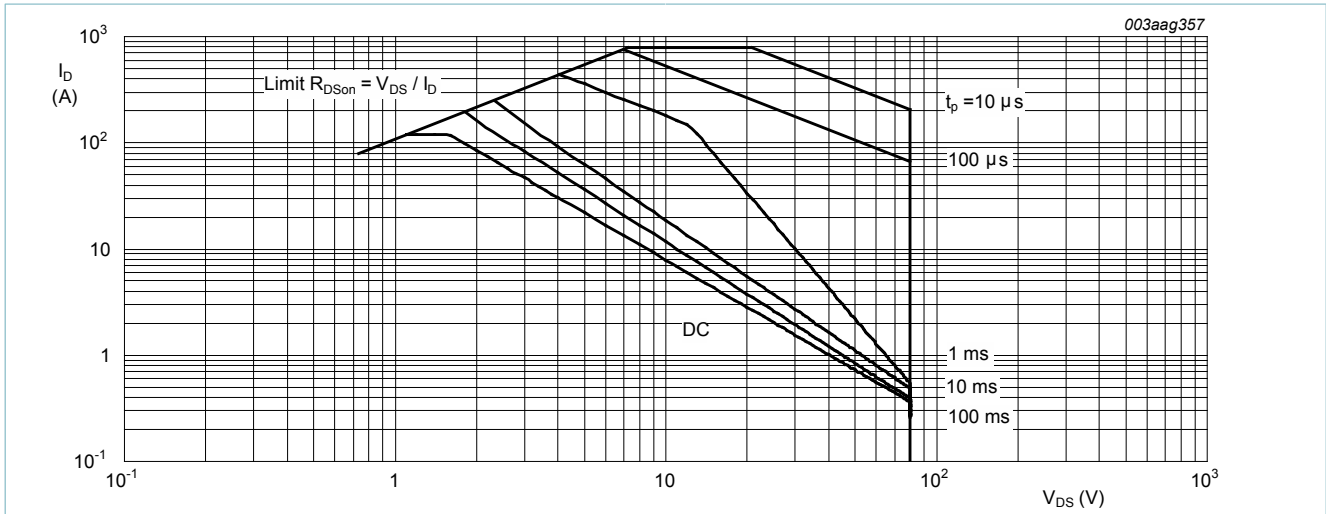


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

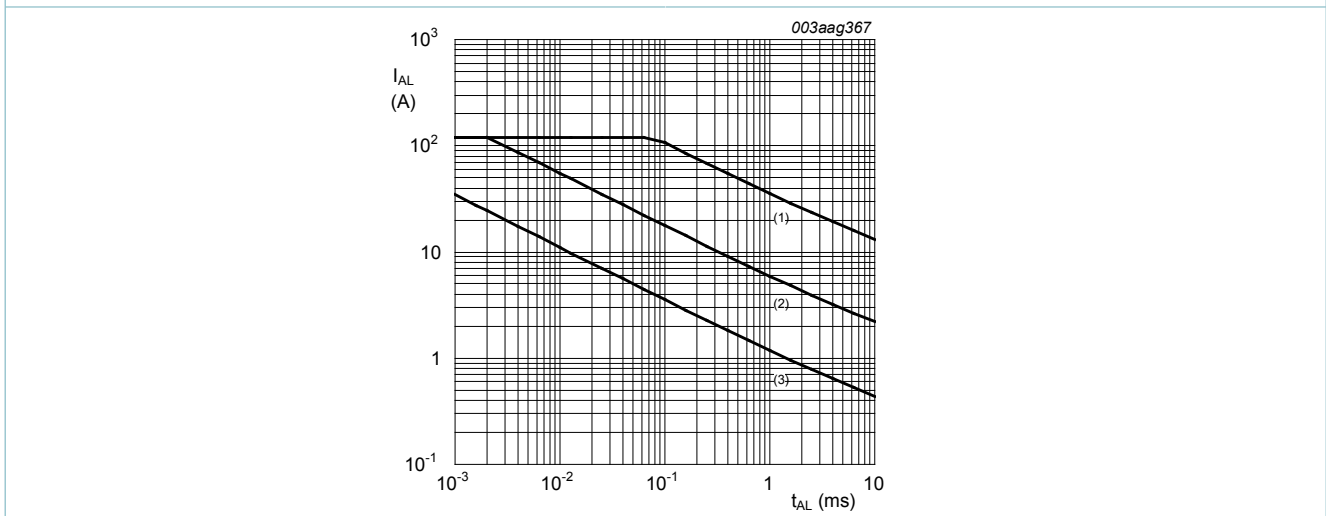


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time.

(1) $T_{j(jnt)} = 25^\circ C$; (2) $T_{j(jnt)} = 150^\circ C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

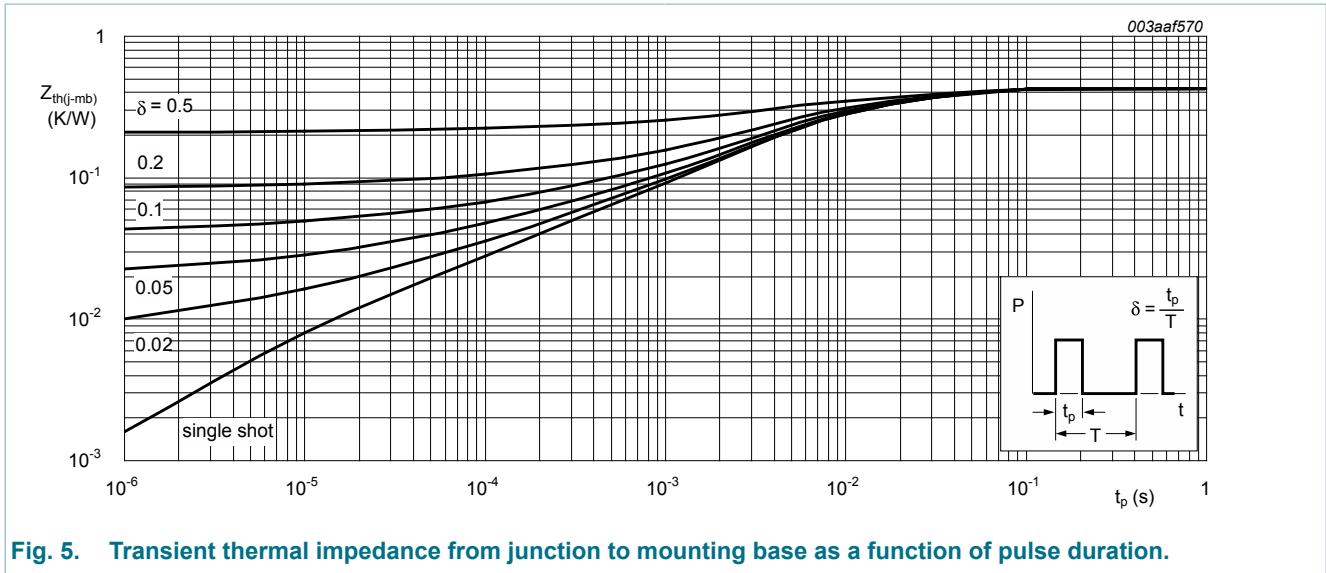


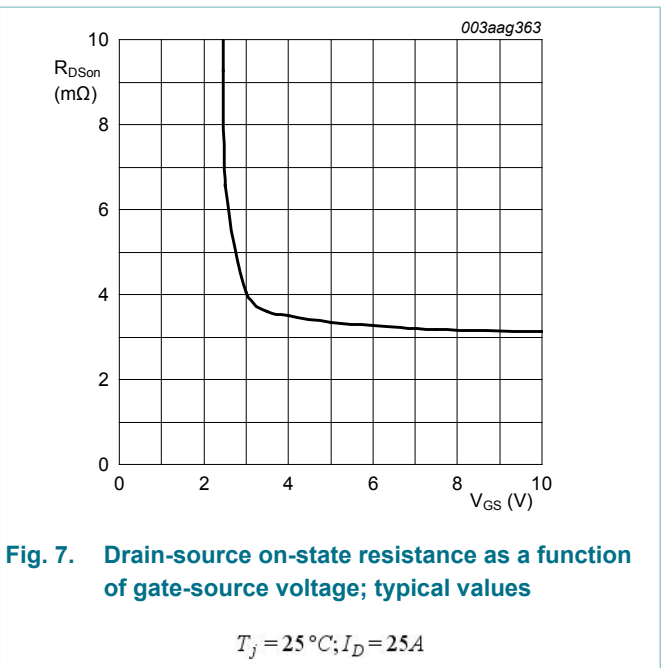
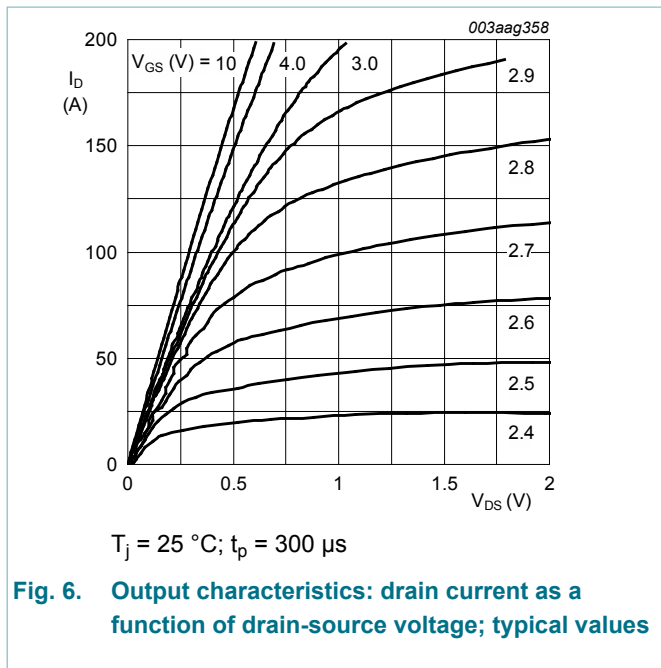
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	80	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	72	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 9	-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	-	0.08	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	3.4	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	3.2	4	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	10.4	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 64 V; V _{GS} = 5 V; Fig. 13; Fig. 14	-	123	-	nC
Q _{GS}	gate-source charge		-	26.6	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GD}	gate-drain charge		-	37.5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	12850	17130	pF
C_{oss}	output capacitance	$T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	850	1020	pF
C_{rss}	reverse transfer capacitance		-	420	580	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60\text{ V}; R_L = 2.4\text{ }\Omega; V_{GS} = 5\text{ V};$	-	70	-	ns
t_r	rise time	$R_{G(ext)} = 5\text{ }\Omega$	-	109	-	ns
$t_{d(off)}$	turn-off delay time		-	203	-	ns
t_f	fall time		-	115	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	61	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	139	-	nC



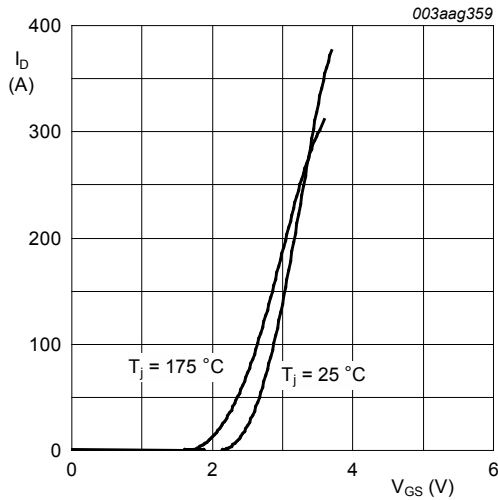


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 12V$

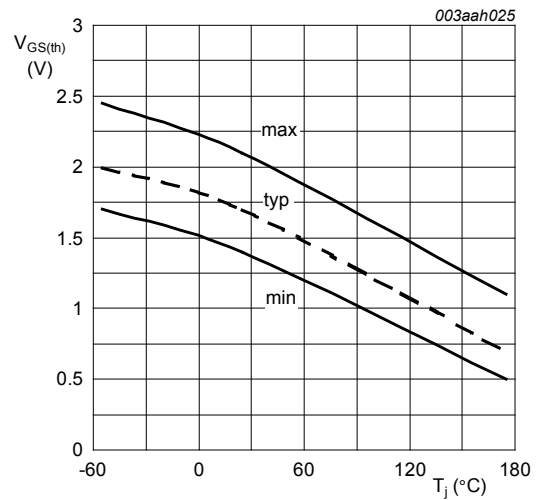


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

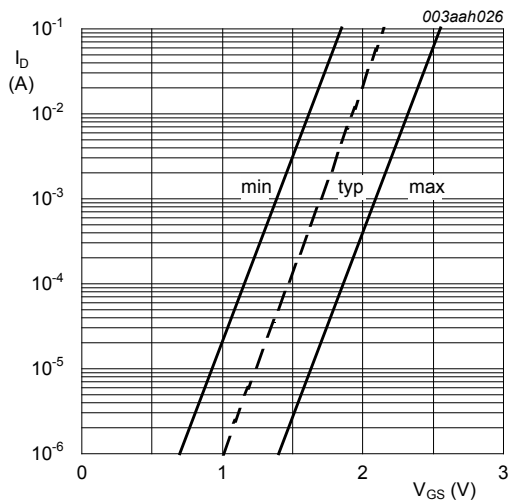


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5V$

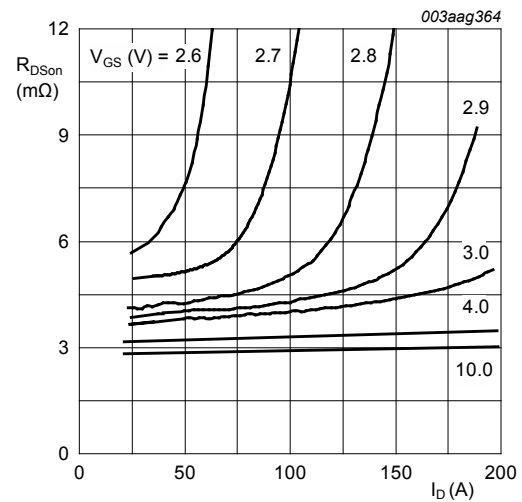


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

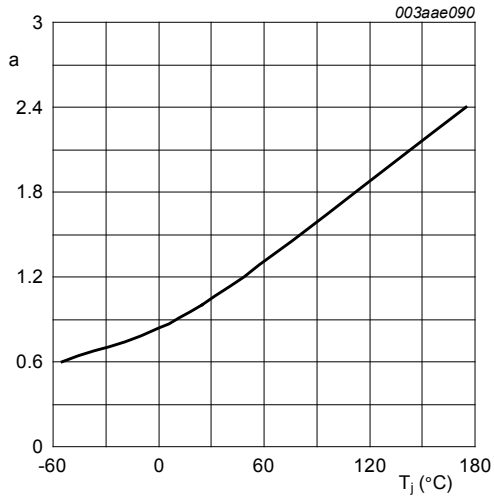
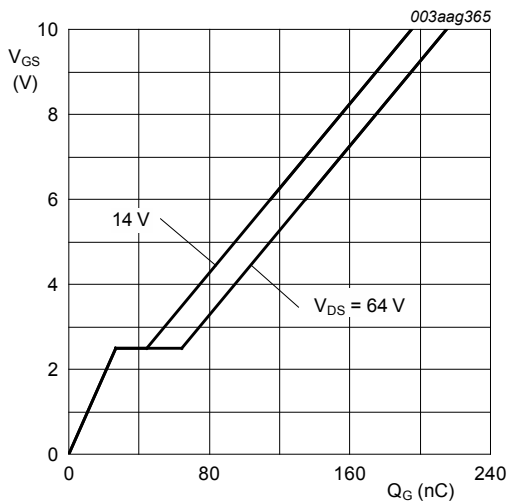


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ C}}$$



$T_j = 25^\circ C; I_D = 25 A$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

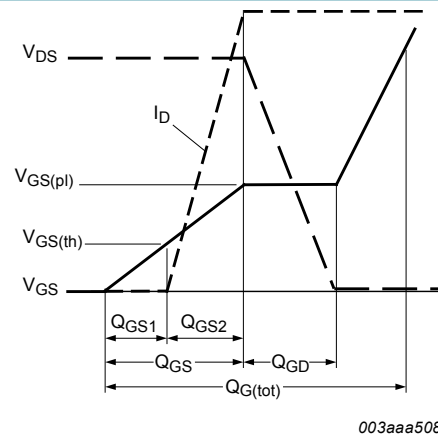
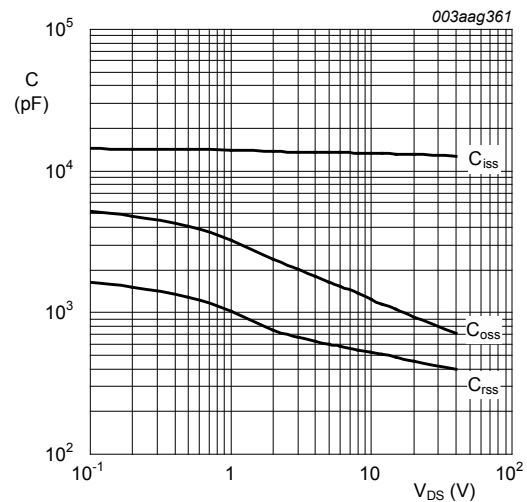


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 V; f = 1 MHz$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

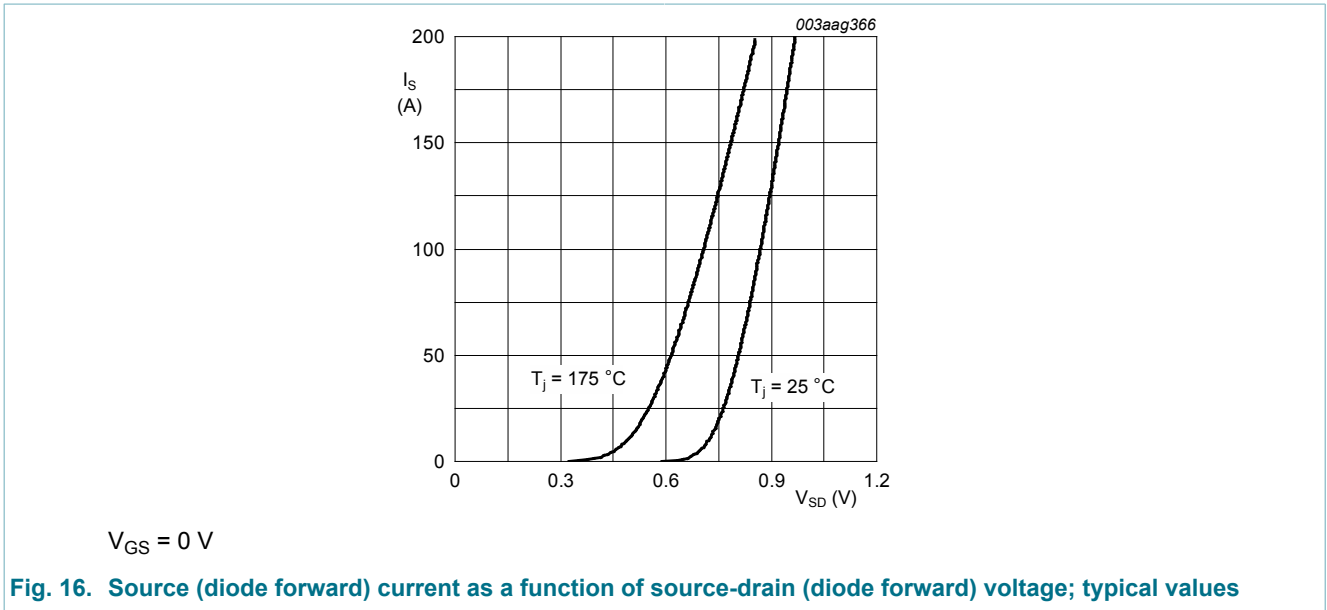


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

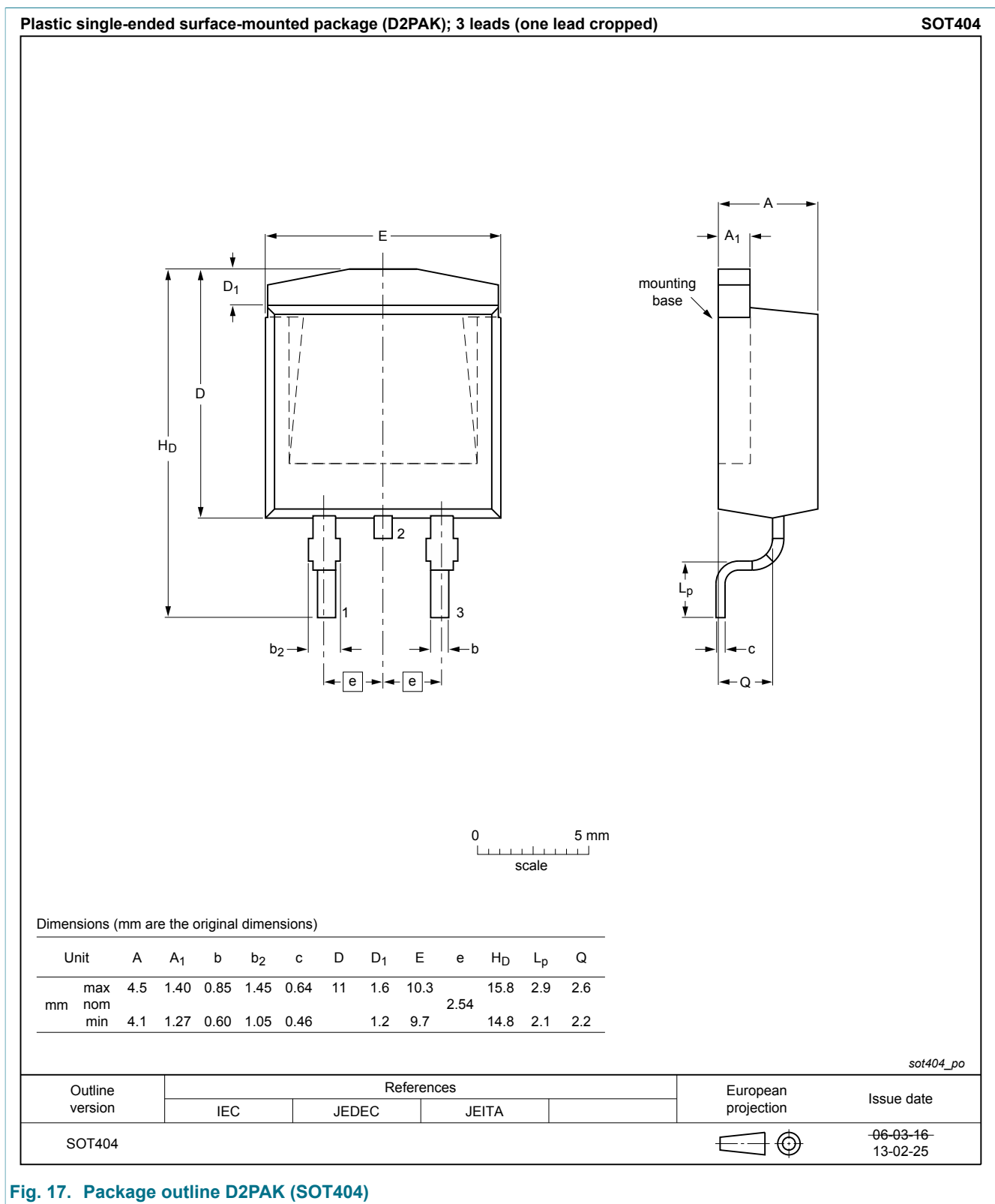


Fig. 17. Package outline D2PAK (SOT404)

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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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