

NXP ACTT4X-800E Thyristor datasheet

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Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

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ACTT4X-800E

AC Thyristor Triac power switch

12 March 2014

Product data sheet

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Isolated mounting base package
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	35	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 94\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	4	A



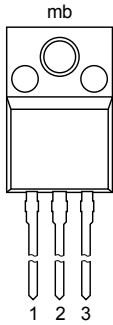
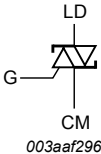
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PP}	peak pulse voltage	T _J = 25 °C; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _J = 25 °C; Fig. 8	-	-	10	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _J = 25 °C; Fig. 8	-	-	10	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _J = 25 °C; Fig. 8	-	-	10	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _J = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _J = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 13	500	-	-	V/μs
di _{com} /dt	rate of change of commutating current	V _D = 400 V; T _J = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 1 V/μs; gate open circuit; Fig. 14 ; Fig. 15	8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>TO-220F (SOT186A)</p>	
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT4X-800E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 94\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	35	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	39	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	6	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_j	junction temperature		-	125	$^\circ\text{C}$
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^\circ\text{C}$; non-repetitive, off-state; Fig. 6	-	2	kV

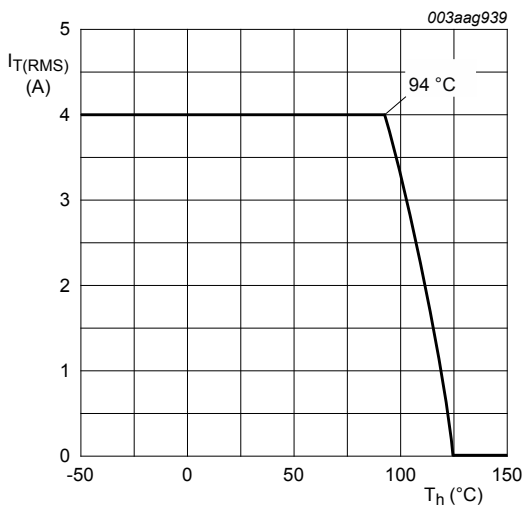


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

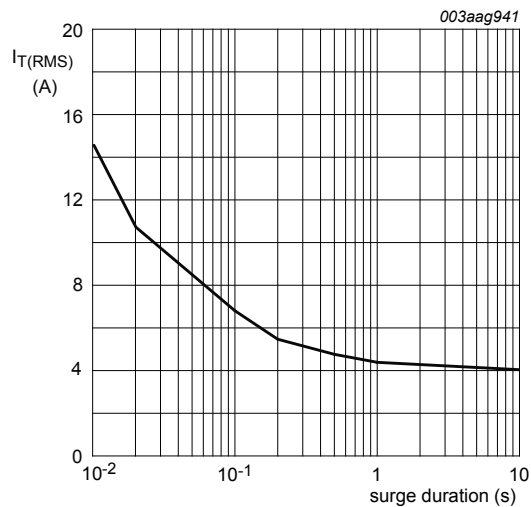


Fig. 2. on-state current as a function of surge duration; maximum values

$f = 50\text{ Hz}$; $T_h = 94\text{ }^\circ\text{C}$

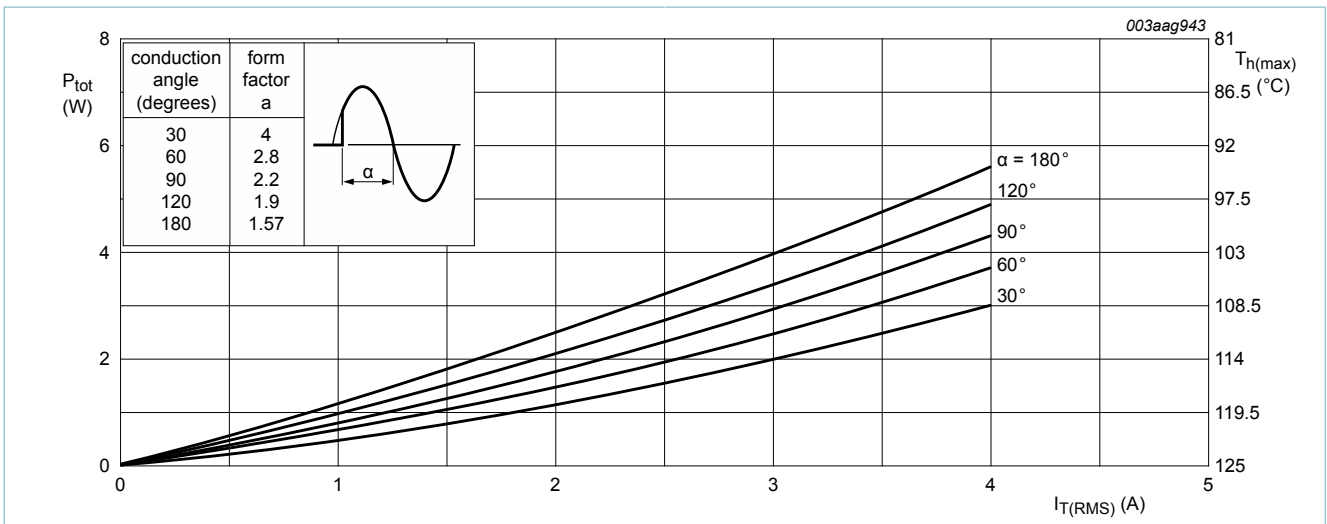


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

$\alpha = \text{conduction angle}$
 $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

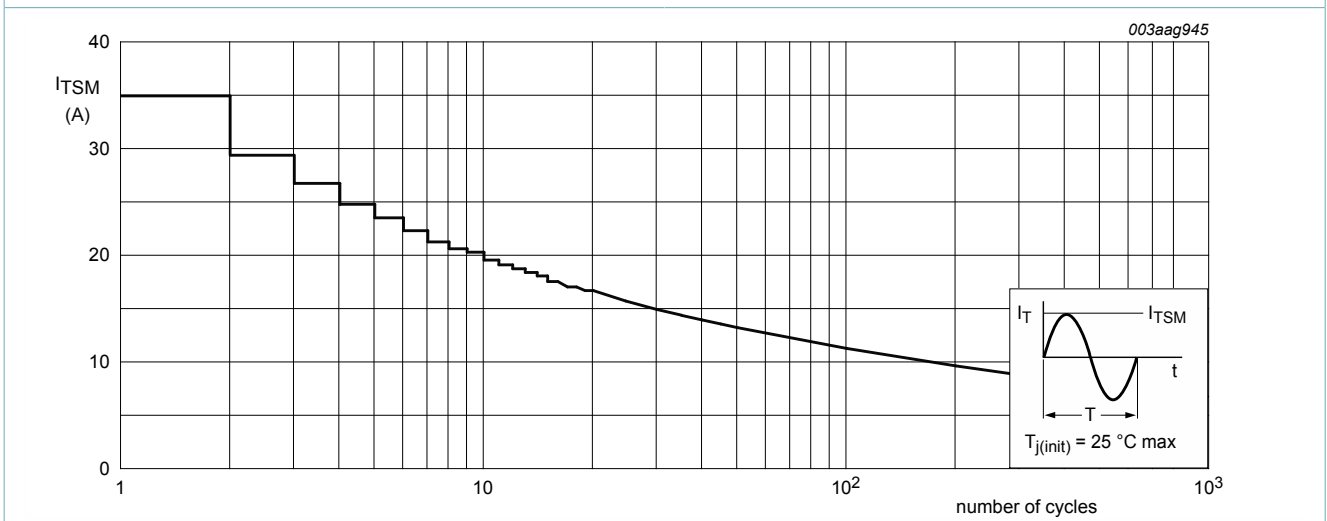


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

f = 50 Hz

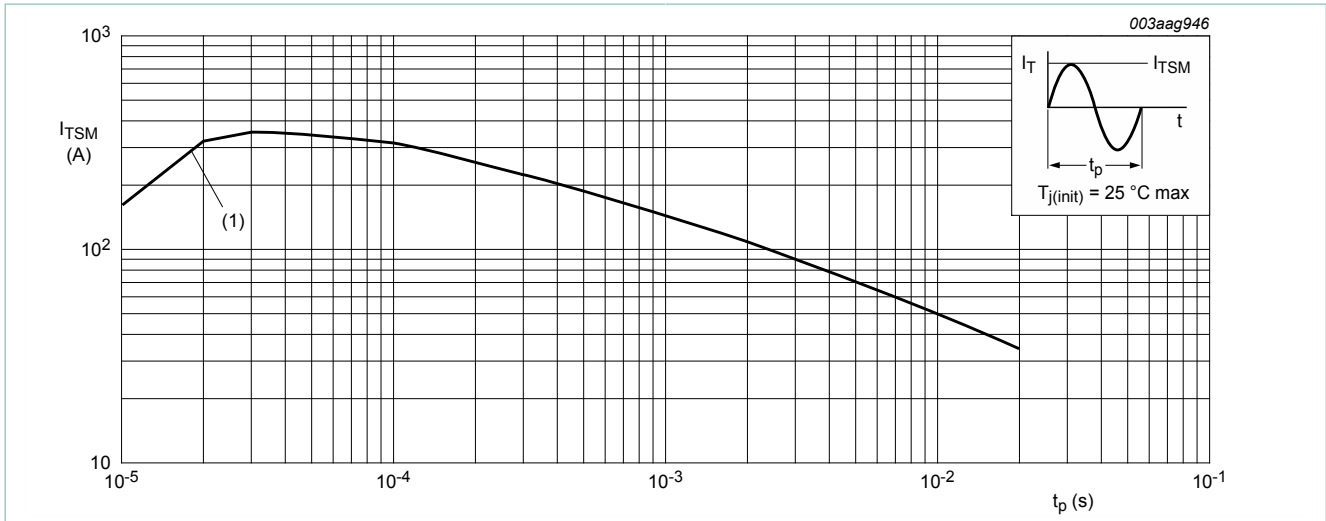


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

$t_p \leq 20 \text{ ms}$; (1) dI_T / dt limit

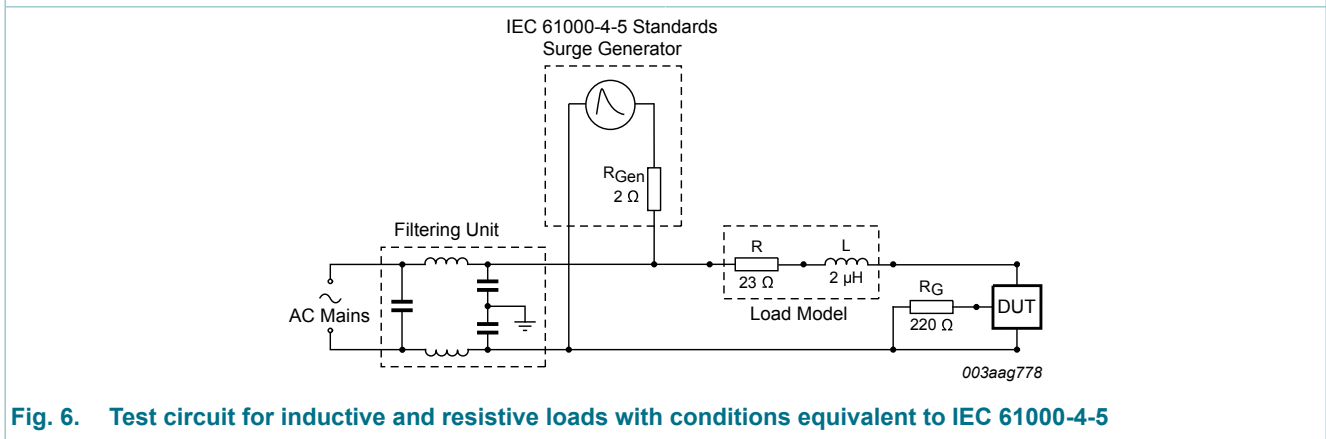
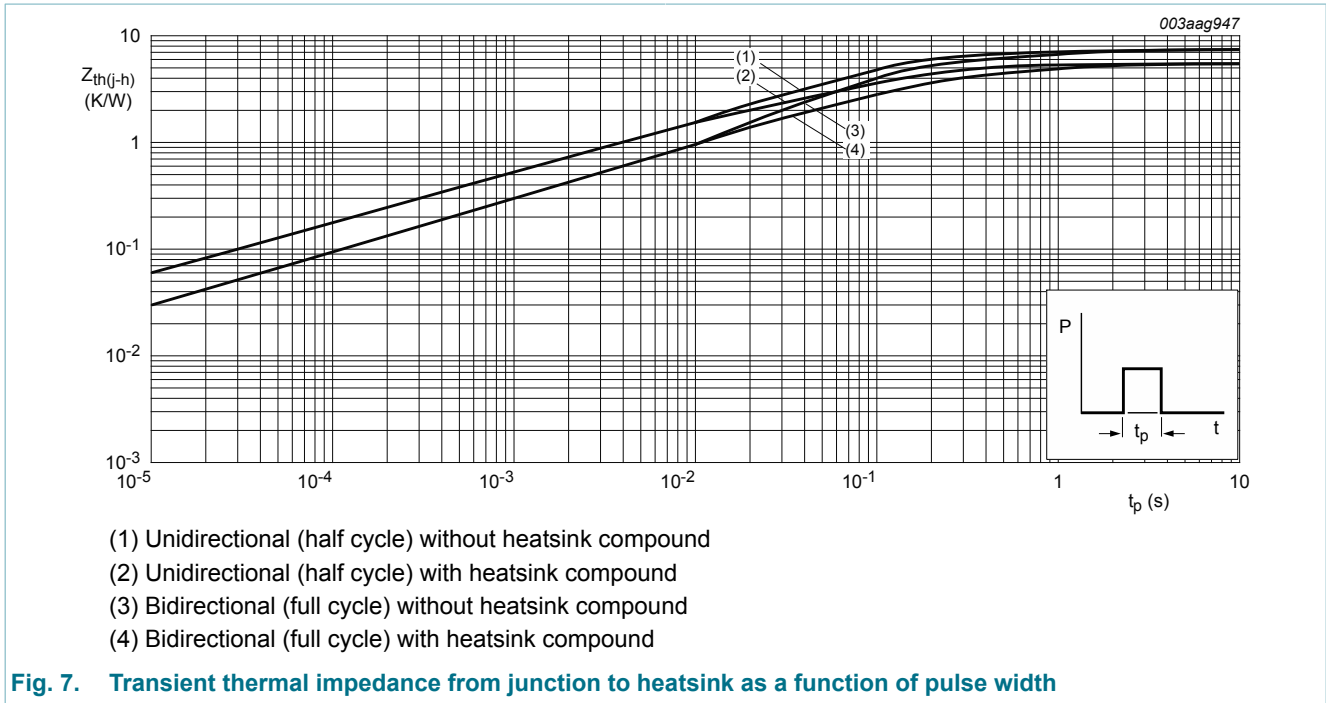


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 7	-	-	5.5	K/W
		full cycle or half cycle; without heatsink compound; Fig. 7	-	-	7.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; $T_h = 25\text{ °C}$; sinusoidal waveform; from all pins to external heatsink; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	$T_h = 25\text{ °C}$; from LD pin to external heatsink; f = 1 MHz	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _L	latching current	V _D = 12 V; I _G = 100 mA; LD+ G+; T _j = 25 °C; Fig. 9	-	-	30	mA
		V _D = 12 V; I _G = 100 mA; LD+ G-; T _j = 25 °C; Fig. 9	-	-	40	mA
		V _D = 12 V; I _G = 100 mA; LD- G-; T _j = 25 °C; Fig. 9	-	-	30	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 10	-	-	20	mA
V _T	on-state voltage	I _T = 6 A; T _j = 25 °C; Fig. 11	-	-	1.7	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 100 mA; T _j = 25 °C; Fig. 12	-	0.8	1	V
		V _D = 400 V; I _T = 100 mA; T _j = 125 °C; Fig. 12	0.2	0.45	-	V
I _D	off-state current	V _D = 800 V; T _j = 25 °C	-	-	10	µA
		V _D = 800 V; T _j = 125 °C	-	-	0.5	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 13	500	-	-	V/µs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14 ; Fig. 15	4	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 10 V/µs; gate open circuit; Fig. 14 ; Fig. 15	5	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 1 V/µs; gate open circuit; Fig. 14 ; Fig. 15	8	-	-	A/ms

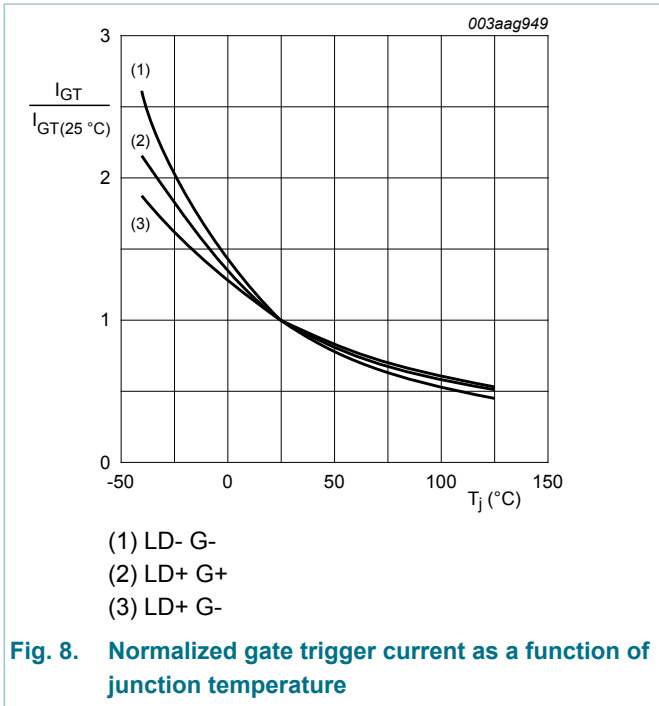


Fig. 8. Normalized gate trigger current as a function of junction temperature

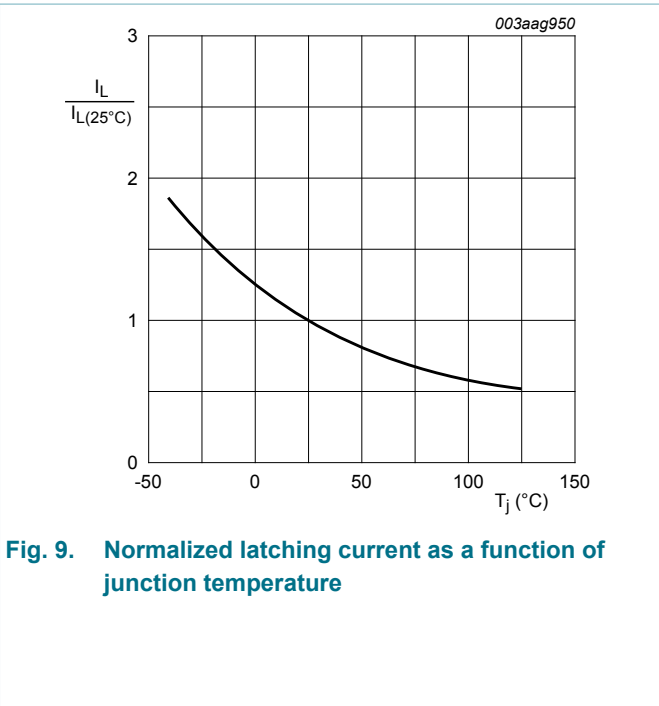


Fig. 9. Normalized latching current as a function of junction temperature

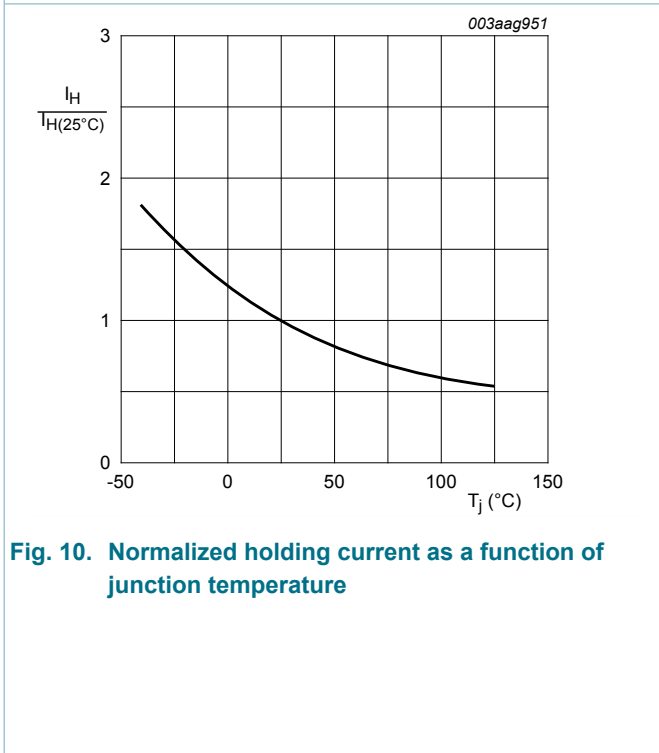


Fig. 10. Normalized holding current as a function of junction temperature

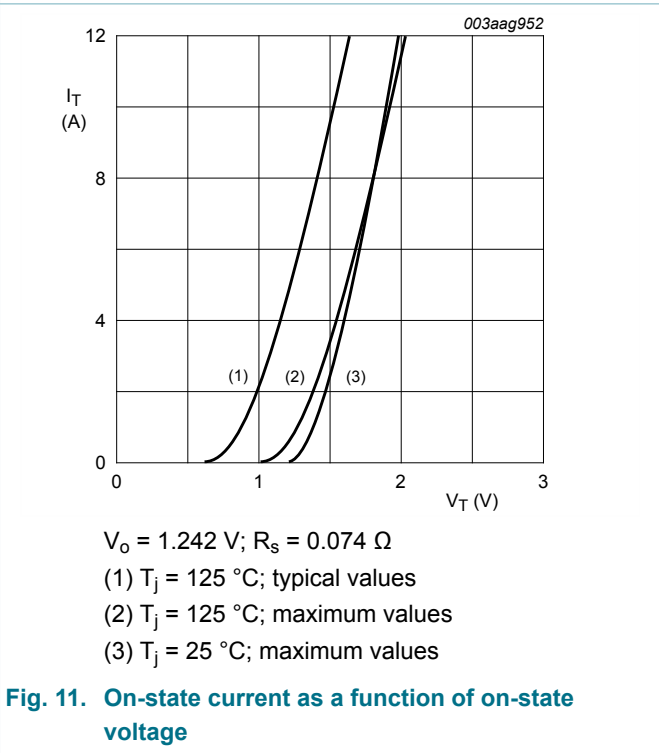


Fig. 11. On-state current as a function of on-state voltage

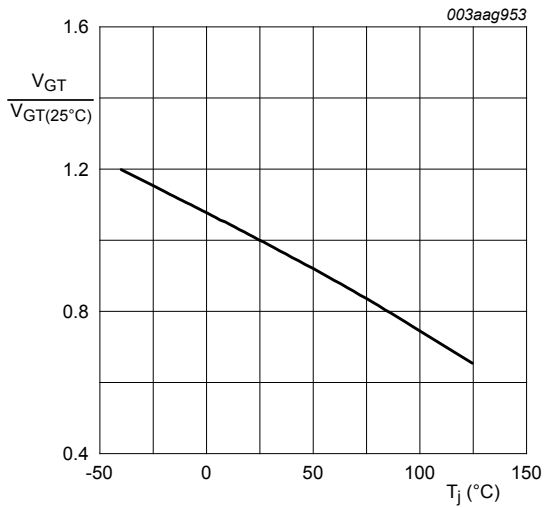
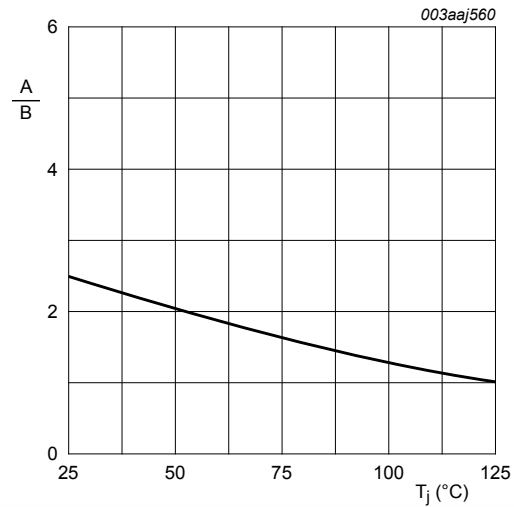
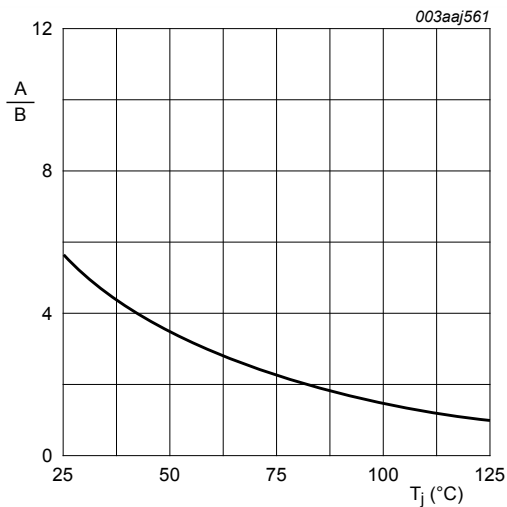


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



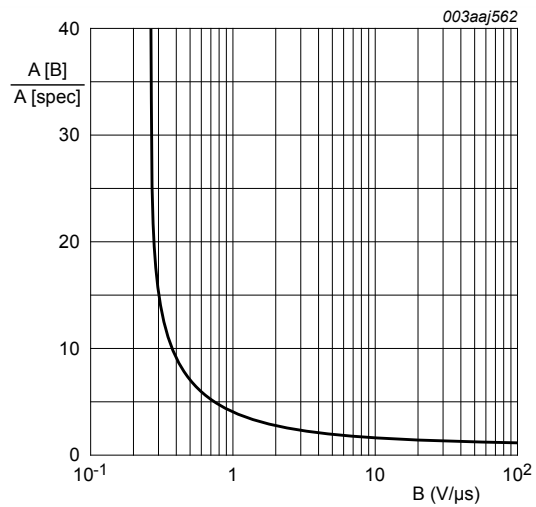
A is dV_D/dt at condition T_j °C
 B is dV_D/dt at condition T_j 125 °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A is di_{com}/dt at condition T_j °C
 B is di_{com}/dt at condition T_j 125 °C
 $V_D = 400$ V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A[B] is di_{com}/dt at condition B, dV_{com}/dt
 A[spec] is the specified data sheet value of di_{com}/dt
 turn-off time < 20 ms

Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

11. Package outline

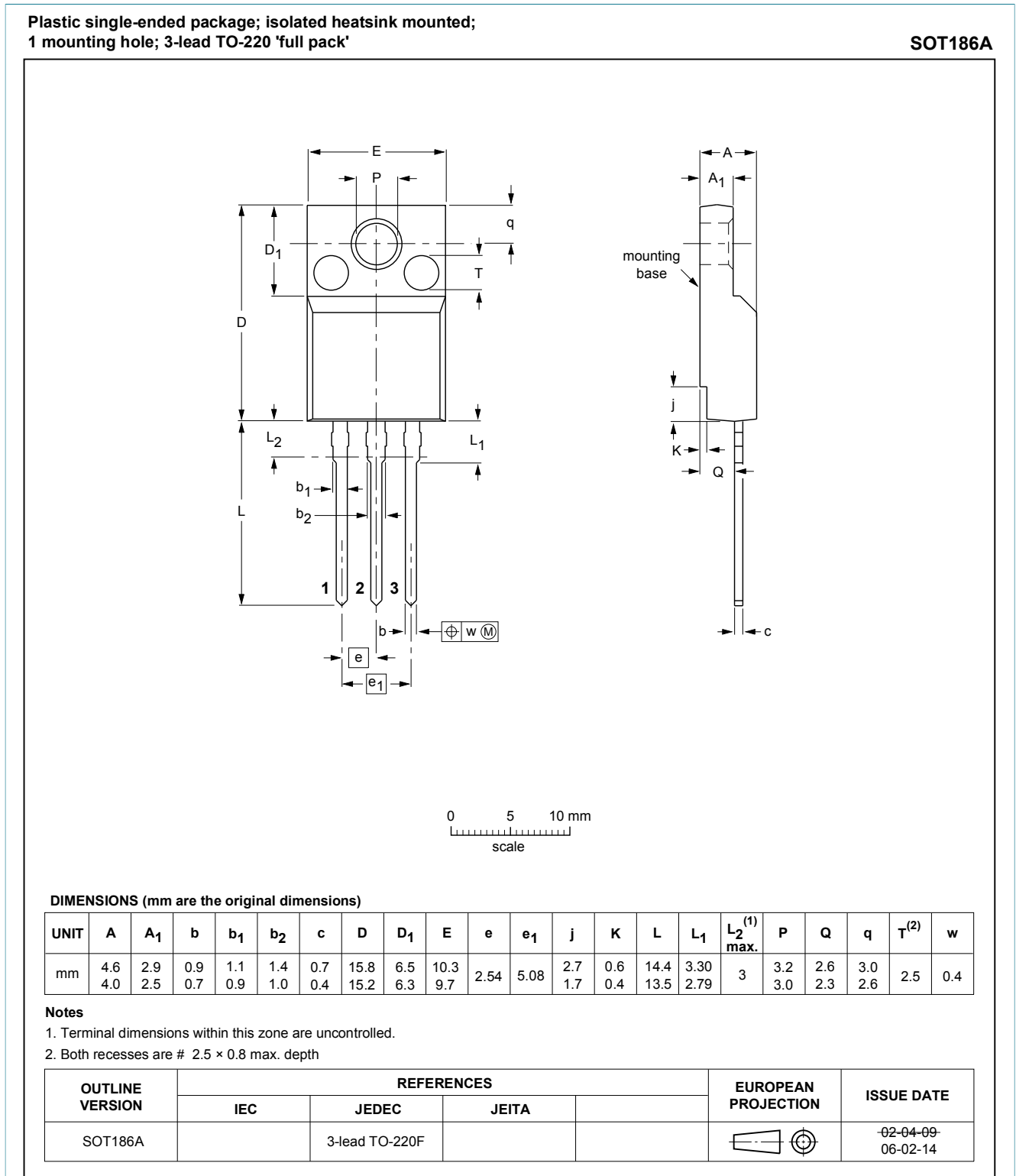


Fig. 16. Package outline TO-220F (SOT186A)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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