# NXP 74LV165 Counter datasheet

http://www.manuallib.com/nxp/74lv165-counter-datasheet.html

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and Q7) available from the last stage. When the parallel-load input (PL) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input PL is HIGH, data enters the register serially at the input DS. It shifts one place to the right (Q0 Q1 Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output Q7 to the input DS of the succeeding stage.

# 74LV165

## 8-bit parallel-in/serial-out shift register

**Rev. 6 — 19 February 2014** **Product data sheet**

## 1. General description

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and $\overline{Q7}$) available from the last stage. When the parallel-load input ($\overline{PL}$) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input $\overline{PL}$ is HIGH, data enters the register serially at the input DS. It shifts one place to the right (Q0 → Q1 → Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output Q7 to the input DS of the succeeding stage.

The clock input is a gate-$\overline{OR}$ structure which allows one input to be used as an active LOW clock enable input ($\overline{CE}$) input. The pin assignment for the inputs CP and $\overline{CE}$ is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when PL is activated.

## 2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- Synchronous parallel-to-serial applications
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- 5.5 V tolerant inputs/outputs
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
  - JESD8-1A (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114-A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LV165N | −40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74LV165D | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74LV165DB | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74LV165PW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

## 4. Functional diagram

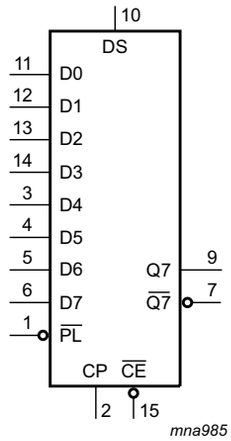



**Fig 1. Logic symbol**

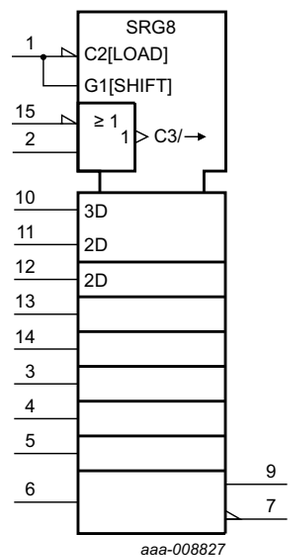



**Fig 2. IEC logic symbol**

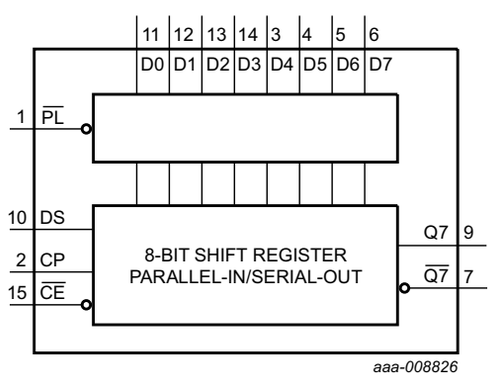



**Fig 3. Functional diagram**

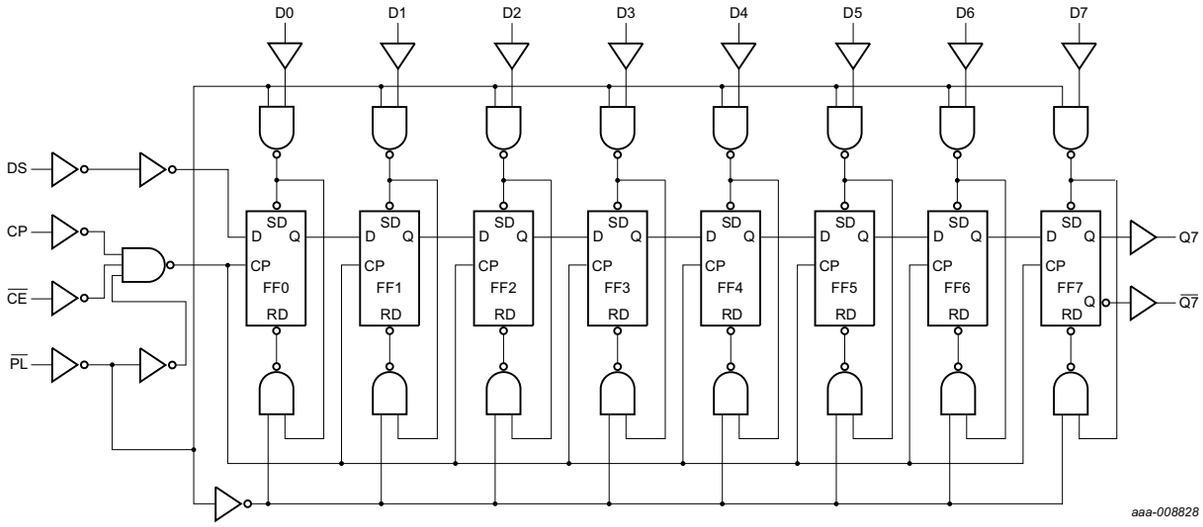



**Fig 4. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

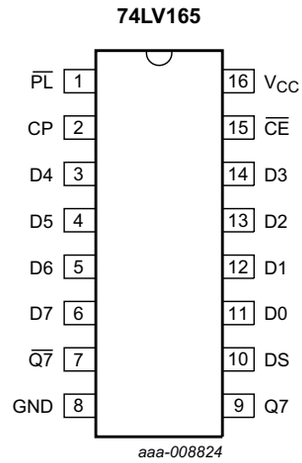



**Fig 5. Pin configuration (DIP16, SO16 and (T)SSOP16)**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{PL}$ | 1 | parallel enable input (active LOW) |
| CP | 2 | clock input (LOW-to-HIGH edge-triggered) |
| $\overline{Q7}$ | 7 | complementary serial output from the last stage |
| GND | 8 | ground (0 V) |
| Q7 | 9 | serial output from the last stage |
| DS | 10 | serial data input |
| D0 to D7 | 11, 12, 13, 14, 3, 4, 5, 6 | parallel data inputs |
| $\overline{CE}$ | 15 | clock enable input (active LOW) |
| $V_{CC}$ | 16 | positive supply voltage |

## 6. Functional description

**Table 3. Function table[1]**

| Operating modes | Inputs | | | | | Qn registers | | Output | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{PL}$ | $\overline{CE}$ | CP | DS | D0 to D7 | Q0 | Q1 to Q6 | Q7 | $\overline{Q7}$ |
| parallel load | L | X | X | X | L | L | L to L | L | H |
| | L | X | X | X | H | H | H to H | H | L |
| serial shift | H | L | ↑ | l | X | L | q0 to q5 | q6 | $\overline{q6}$ |
| | H | L | ↑ | h | X | H | q0 to q5 | q6 | $\overline{q6}$ |
| hold “do nothing” | H | H | X | X | X | q0 | q1 to q6 | q7 | q7 |

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don’t care;
↑ = LOW-to-HIGH clock transition.

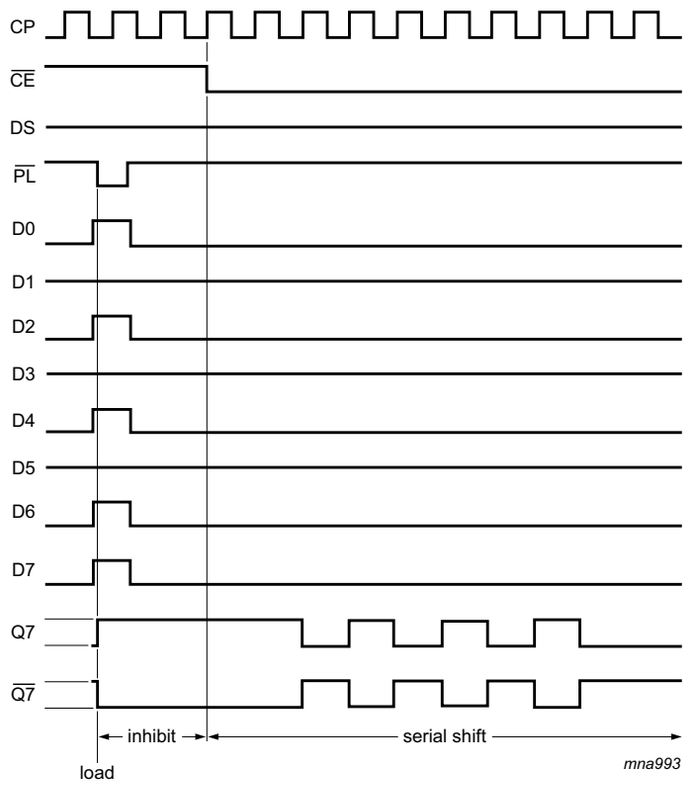



**Fig 6. Timing diagram**

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | 20 | mA |
| $V_I$ | input voltage | | | –0.5 | +7 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ | | - | ±50 | mA |
| $I_O$ | output current | $–0.5$ V $< V_O < V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | +50 | mA |
| $I_{GND}$ | ground current | | | –50 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | | | | |
| | | DIP16 package | [2] | - | 750 | mW |
| | | SO16 package | [3] | - | 500 | mW |
| | | (T)SSOP16 package | [4] | - | 400 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[3] $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[4] $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.0 | 3.3 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.0 V to 2.0 V | 0 | - | 500 | ns/V |
| | | $V_{CC}$ = 2.0 V to 2.7 V | 0 | - | 200 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 100 | ns/V |
| | | $V_{CC}$ = 3.6 V to 5.5 V | 0 | - | 50 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –100 μA | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 1.2 | | - | | |
| | | $V_{CC}$ = 2.0 V | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $V_{CC}$ = 2.7 V | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $V_{CC}$ = 4.5 V | 4.3 | 4.5 | - | 4.3 | - | V |
| | | standard outputs: $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $V_{CC}$ = 3.0 V; $I_O$ = –6 mA | 2.40 | 2.82 | - | 2.20 | - | V |
| | | $V_{CC}$ = 4.5 V; $I_O$ = –12 mA | 3.60 | 4.20 | - | 3.50 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100 μA | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 0 | - | - | - | |
| | | $V_{CC}$ = 2.0 V | - | 0 | 0.2 | 1.8 | 0.2 | V |
| | | $V_{CC}$ = 2.7 V | - | 0 | 0.2 | 2.5 | 0.2 | V |
| | | $V_{CC}$ = 3.0 V | - | 0 | 0.2 | 2.8 | 0.2 | V |
| | | $V_{CC}$ = 4.5 V | - | 0 | 0.2 | 4.3 | 0.2 | V |
| | | standard outputs: $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $V_{CC}$ = 3.0 V; $I_O$ = 6 mA | - | 0.25 | 0.40 | - | 0.50 | V |
| | | $V_{CC}$ = 4.5 V; $I_O$ = 12 mA | - | 0.35 | 0.55 | - | 0.65 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±1 | - | ±1 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 20 | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | VI = $V_{CC}$ – 0.6 V; $V_{CC}$ = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | | | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND (ground = 0 V); for test circuit, see Figure 12*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | $\overline{CE}$, CP to Q7, $\overline{Q7}$; see Figure 7 and Figure 8 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 115 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 38 | 61 | - | 76 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 27 | 43 | - | 54 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 22 | 36 | - | 45 | ns |
| | | $V_{CC}$ = 3.3 V; $C_L$ = 15 pF | | - | 18 | - | - | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | - | 15 | 24 | - | 30 | ns |
| | | $\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 8 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 110 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 35 | 56 | - | 70 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 24 | 39 | - | 49 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 20 | 33 | - | 41 | ns |
| | | $V_{CC}$ = 3.3 V; $C_L$ = 15 pF | | - | 18 | - | - | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | - | 14 | 22 | - | 27 | ns |
| | | D7 to Q7, $\overline{Q7}$; CL = 15 pF; see Figure 9 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 90 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 28 | 45 | - | 56 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 20 | 32 | - | 40 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 17 | 27 | - | 33 | ns |
| | | $V_{CC}$ = 3.3 V; $C_L$ = 15 pF | | - | 14 | - | - | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | - | 11 | 18 | - | 22 | ns |
| $t_W$ | pulse width | CP input HIGH to LOW; see Figure 7 | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 34 | 10 | - | 41 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 25 | 8 | - | 30 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 20 | 7 | - | 24 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 15 | 5 | - | 18 | - | ns |
| | | $\overline{PL}$ input LOW; see Figure 8 | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 34 | 10 | - | 41 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 25 | 8 | - | 30 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 20 | 7 | - | 24 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 15 | 5 | - | 18 | - | ns |

**Table 7. Dynamic characteristics** *…continued*

*GND (ground = 0 V); for test circuit, see Figure 12*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{rec}$ | recovery time | $\overline{PL}$ to CP, $\overline{CE}$; see Figure 8 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 40 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 24 | 15 | - | 30 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 18 | 11 | - | 23 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 17 | 10 | - | 21 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 12 | 7 | - | 15 | - | ns |
| $t_{su}$ | set-up time | DS to CP, $\overline{CE}$; see Figure 10 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | –8 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 22 | –2 | - | 26 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 16 | –1 | - | 19 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 13 | –1 | - | 15 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 9 | 0 | - | 10 | - | ns |
| | | $\overline{CE}$ to CP, CP to $\overline{CE}$; see Figure 10 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 20 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 22 | 7 | - | 26 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 16 | 5 | - | 19 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 13 | 4 | - | 15 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 9 | 3 | - | 10 | - | ns |
| | | Dn to $\overline{PL}$; see Figure 11 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 25 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 22 | 8 | - | 26 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 16 | 6 | - | 19 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 13 | 5 | - | 15 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 9 | 4 | - | 10 | - | ns |
| $t_h$ | hold time | DS to CP, $\overline{CE}$; Dn to $\overline{PL}$; see Figure 10 and Figure 11 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 20 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 22 | 7 | - | 26 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 16 | 5 | - | 19 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 13 | 4 | - | 15 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 9 | 3 | - | 10 | - | ns |
| | | $\overline{CE}$ to CP, CP to $\overline{CE}$; see Figure 10 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | –30 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 5 | –8 | - | 5 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 5 | –6 | - | 5 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 5 | –5 | - | 5 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 5 | –4 | - | 5 | - | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND (ground = 0 V); for test circuit, see Figure 12*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $f_{max}$ | maximum frequency | see Figure 7 | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 14 | 40 | - | 12 | - | MHz |
| | | $V_{CC}$ = 2.7 V | | 19 | 60 | - | 16 | - | MHz |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 24 | 65 | - | 20 | - | MHz |
| | | $V_{CC}$ = 3.3 V; $C_L$ = 15 pF | | - | 78 | - | - | - | MHz |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [4] | 36 | 75 | - | 30 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V | [5] | - | 35 | - | | | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

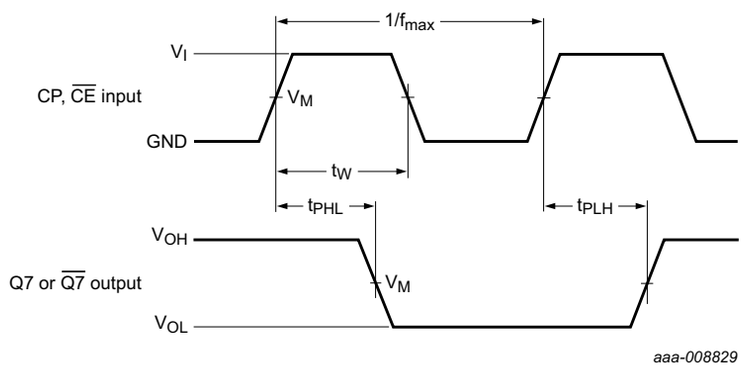
[2] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[3] Typical values are measured at $V_{CC}$ = 3.3 V.

[4] Typical values are measured at $V_{CC}$ = 5.0 V.

[5] $C_{PD}$ is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ ($P_D$ in µW), where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V.

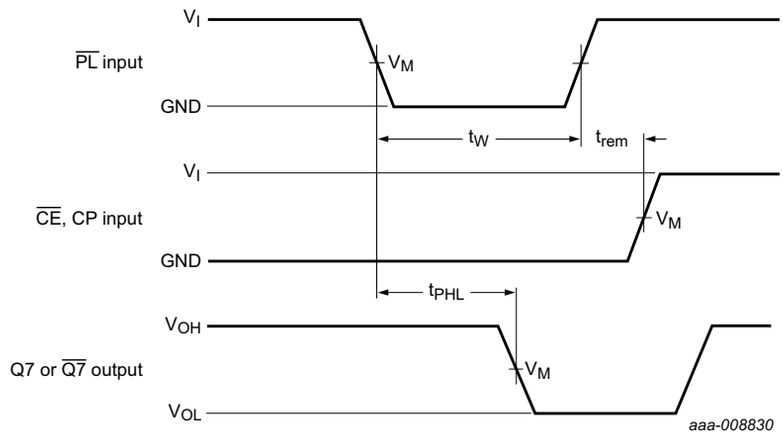
## 11. Waveforms




Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

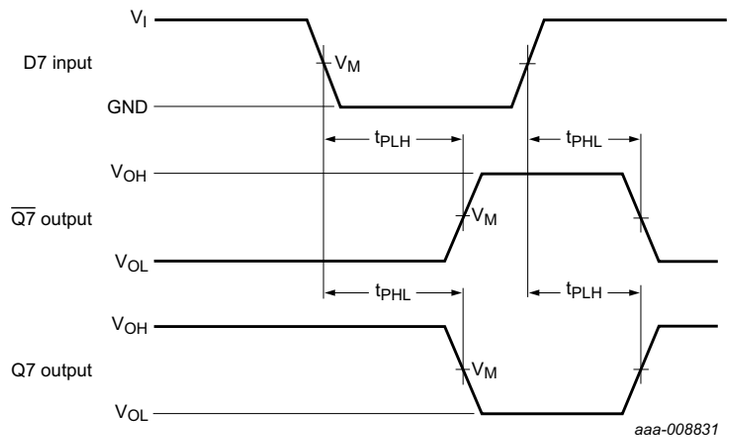
**Fig 7. Clock pulse (CP) and clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, clock pulse width and maximum clock frequency**




Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

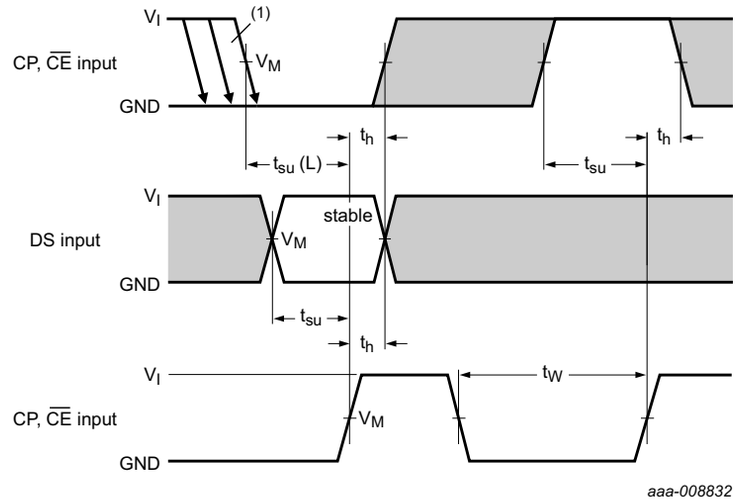
**Fig 8. Parallel load ($\overline{PL}$) pulse width, parallel load to output (Q7 or $\overline{Q7}$) propagation delays, parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time**




Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

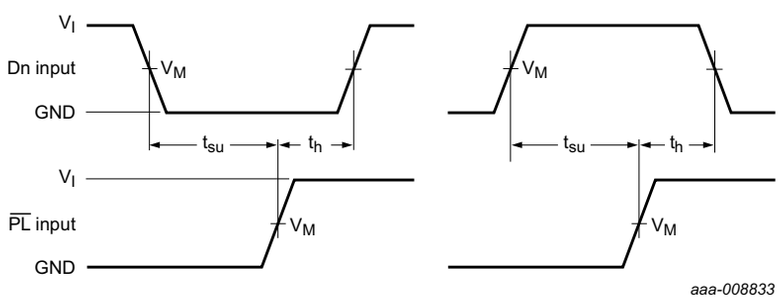
**Fig 9. Data input (Dn) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW**




Measurement points are given in Table 8.

(1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 10. Set-up and hold times**

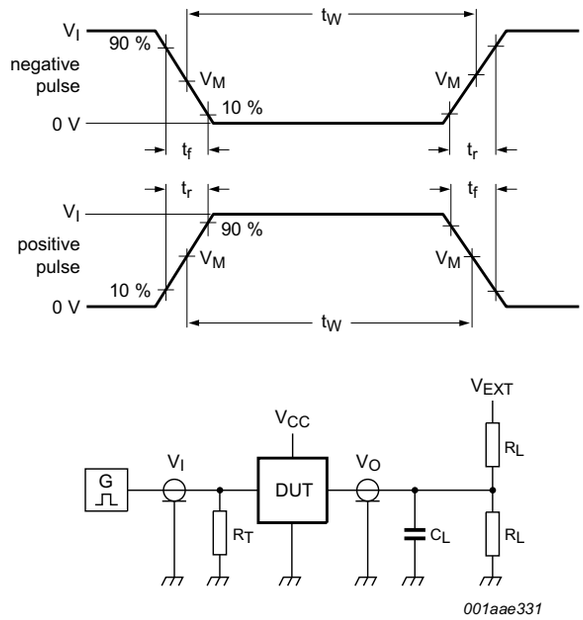



Measurement points are given in Table 8.

**Fig 11. Set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)**

**Table 8. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |




Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

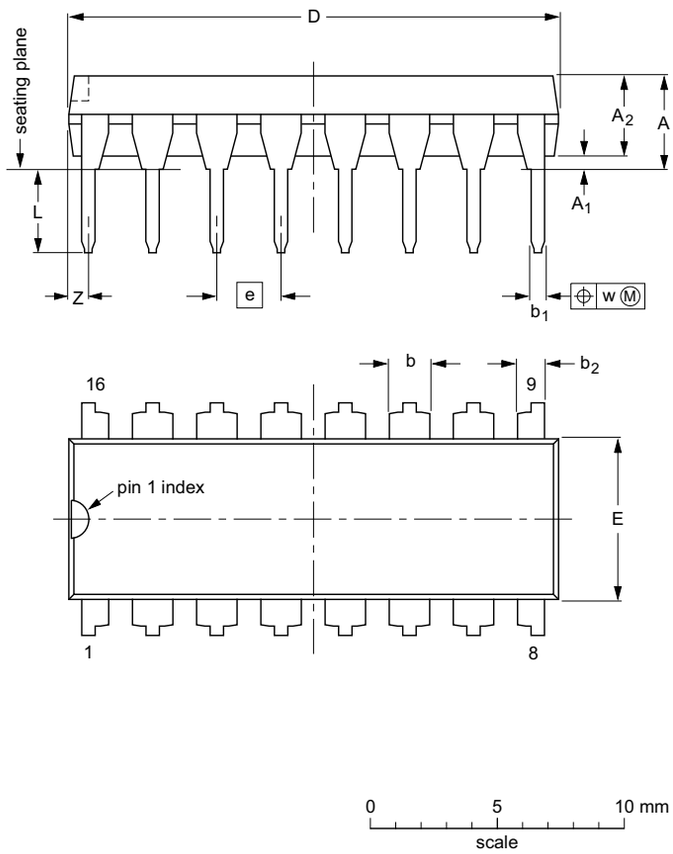
**Fig 12. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ |
| < 2.7 V | $V_{CC}$ | 2.5 ns | 50 pF | 1 kΩ | open |
| 2.7 V to 3.6 V | 2.7 V | 2.5 ns | 50 pF, 15 pF | 1 kΩ | open |
| ≥ 4.5 V | $V_{CC}$ | 2.5 ns | 50 pF | 1 kΩ | open |

## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | L | $M_E$ | $M_H$ | w | $Z^{(1)}$ max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

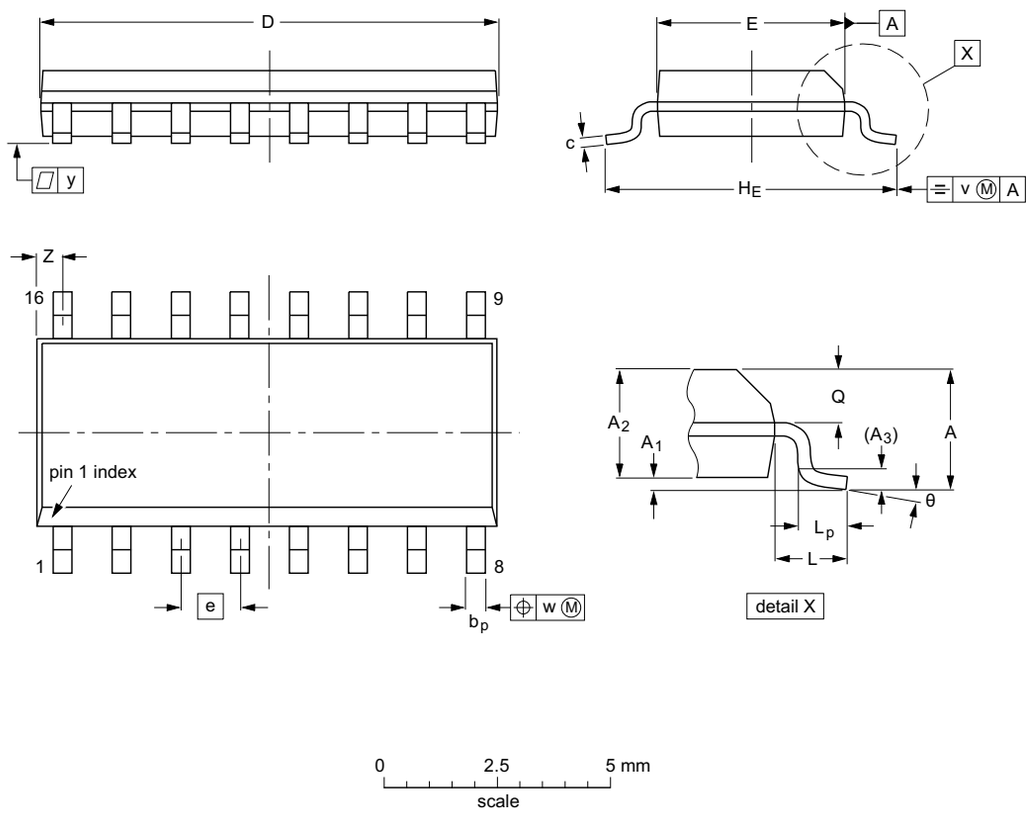
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 13. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

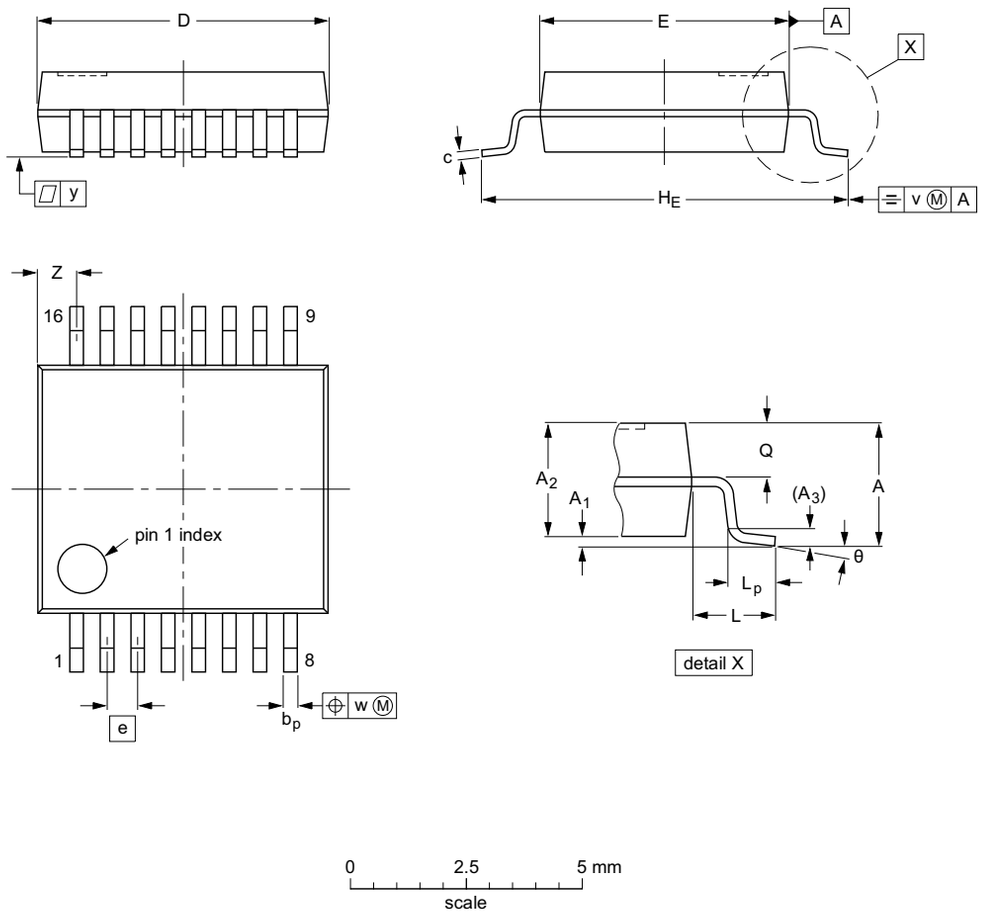
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 14. Package outline SOT109-1 (SO16)**

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | $8^o$<br>$0^o$ |

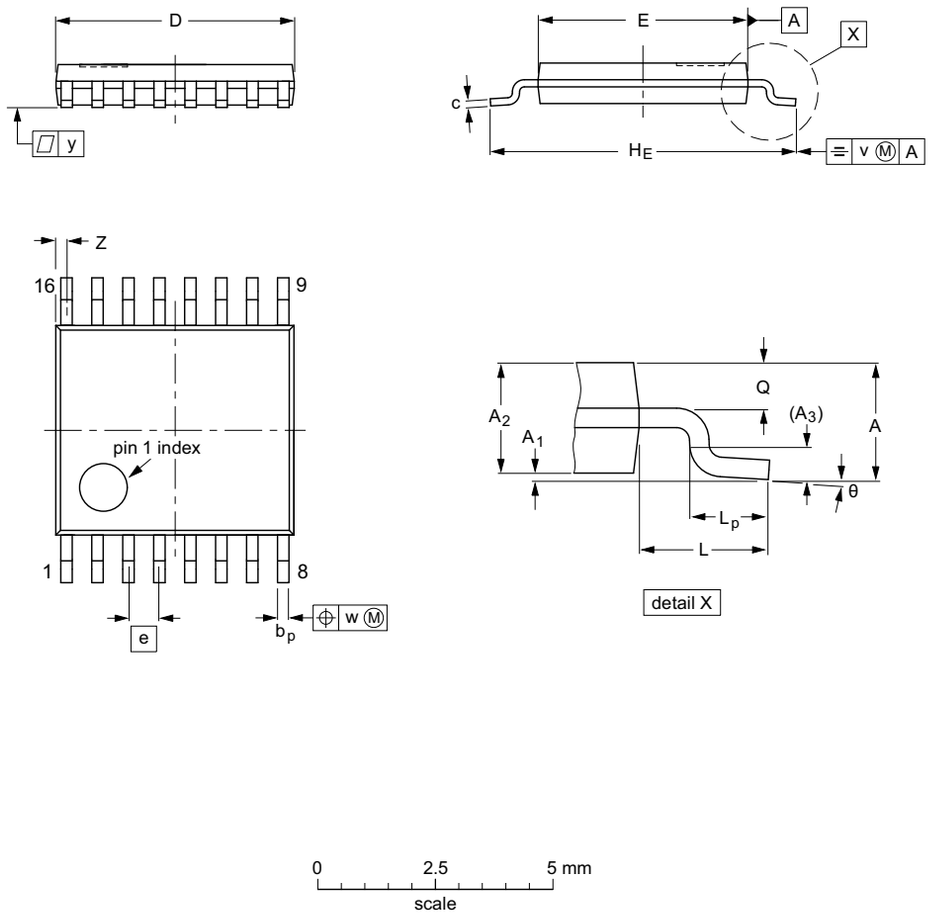
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 15. Package outline SOT338-1 (SSOP16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 16. Package outline SOT403-1 (TSSOP16)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LV165 v.6 | 20140219 | Product data sheet | - | 74LV165 v.5 |
| Modifications: | • Typo corrected in Table 2 “Pin description” | | | |
| 74LV165 v.5 | 20130909 | Product data sheet | - | 74LV165 v.4 |
| Modifications: | • Typo corrected in the header of Table 6 “Static characteristics” | | | |
| 74LV165 v.4 | 20130830 | Product data sheet | - | 74LV165_CNV_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Family data added, see Section 9 “Static characteristics” | | | |
| 74LV165_CNV_3 | December 1998 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 15.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 15.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 17. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 19 February 2014**
**Document identifier: 74LV165**