

NXP TDA6107AJF video output amplifier Datasheet

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The TDA6107AJF contains three video output amplifiers which are intended to drive the three cathodes of a color CRT. The device is contained in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package, and uses high-voltage DMOS technology.

To obtain maximum performance, the amplifier should be used with black-current control.

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TDA6107AJF

Triple video output amplifier

Rev. 02 — 28 April 2005

Product data sheet

1. General description

The TDA6107AJF contains three video output amplifiers which are intended to drive the three cathodes of a color CRT. The device is contained in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package, and uses high-voltage DMOS technology.

To obtain maximum performance, the amplifier should be used with black-current control.

2. Features

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (p-p)
- High slew rate of 900 V/ μ s
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 81
- Black-Current Stabilization (BCS) circuit with voltage window from 1.8 V to 6 V and current window from +100 μ A to -10 mA
- Thermal protection
- Internal protection against positive flashover discharges appearing on the CRT

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
TDA6107AJF	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

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4. Block diagram

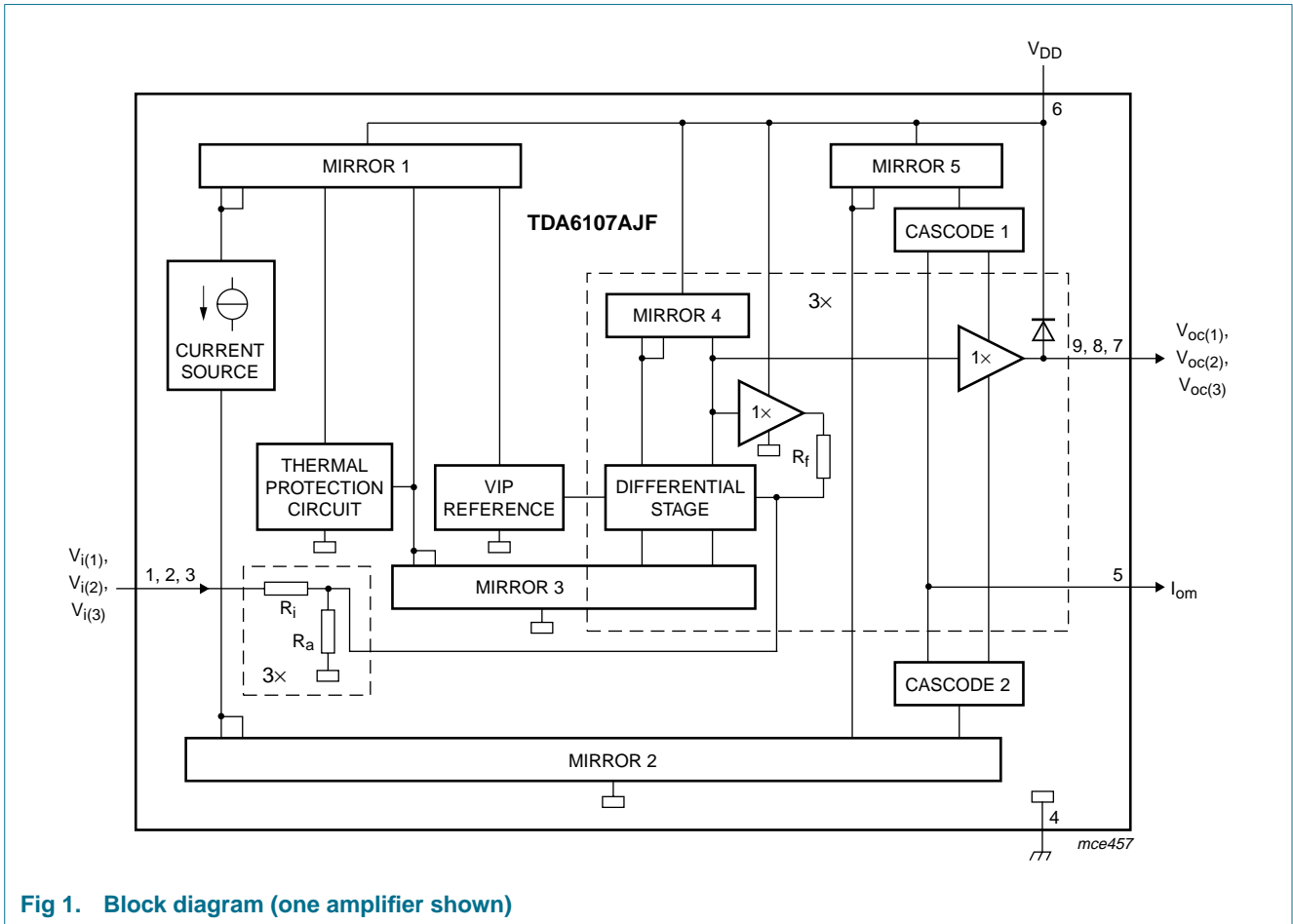


Fig 1. Block diagram (one amplifier shown)

5. Pinning information

5.1 Pinning

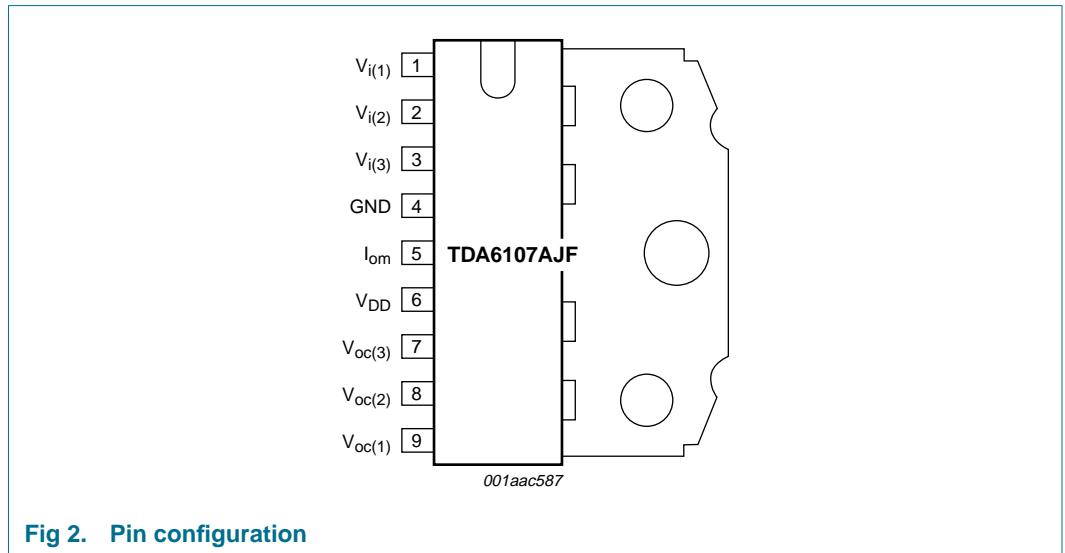


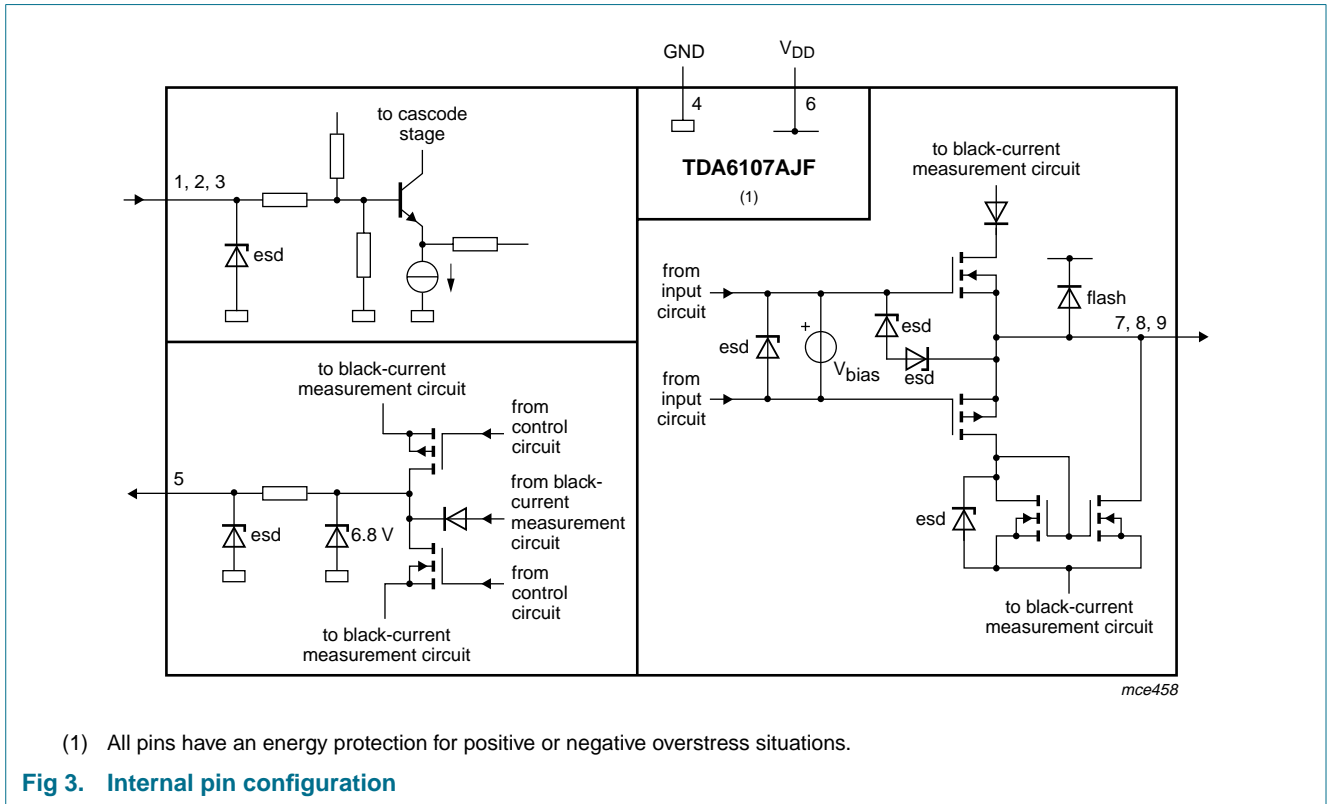
Fig 2. Pin configuration

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black-current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

6. Internal circuitry



7. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages measured with respect to ground; currents as specified in Figure 9; unless otherwise specified.

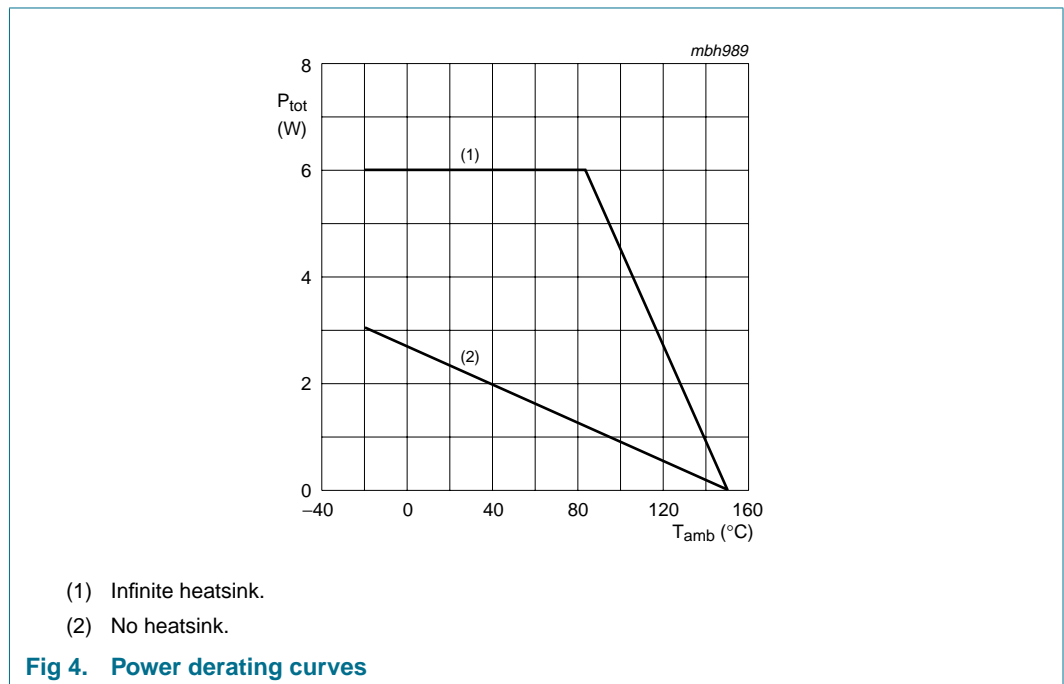
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		0	250	V
V_i	input voltage at pins $V_{i(1)}$, $V_{i(2)}$ and $V_{i(3)}$		0	12	V
V_{om}	measurement output voltage		0	6	V
$ I_{om(\text{mean})} $	absolute value of mean current of measurement output (for three channels)	$V_{oc} = 0 \text{ V to } V_{DD}$; $V_{om} = 1.8 \text{ V to } 6 \text{ V}$	-	5.6	mA
V_{oc}	cathode output voltage		0	V_{DD}	V
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-20	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM)	-	±3000	V
		Machine Model (MM)	-	±300	V

8. Thermal characteristics

Table 4: Thermal characteristics

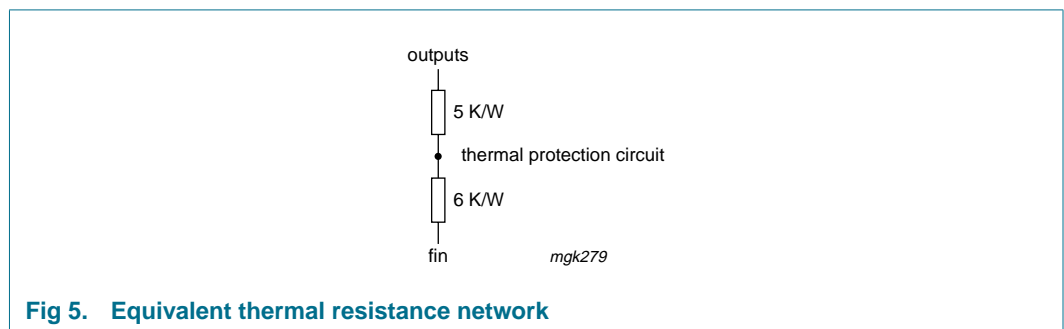
Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	56	K/W
$R_{th(j-fin)}$	thermal resistance from junction to fin		[1] 11	K/W

[1] An external heatsink is necessary; see *Application Note AN10227-01*.



8.1 Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10 % decrease at 130 °C and 30 % decrease at 145 °C (typical values on the spot of the thermal protection circuit).



9. Characteristics

Table 5: Characteristics

Operating range: $T_j = -20\text{ }^\circ\text{C}$ to $+150\text{ }^\circ\text{C}$; $V_{DD} = 180\text{ V}$ to 210 V ; test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{DD} = 200\text{ V}$; $V_{oc(1)} = V_{oc(2)} = V_{oc(3)} = \frac{1}{2}V_{DD}$; $C_L = 10\text{ pF}$ (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)} = 18\text{ K/W}$; measured in test circuit of [Figure 9](#); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_q	quiescent supply current		5.6	6	7.6	mA
$V_{ref(int)}$	internal reference voltage (input stage)		-	2.5	-	V
R_i	input resistance		-	2.1	-	k Ω
G	gain of amplifier		73	81	89	
ΔG	gain difference		-4.2	0	+4.2	
PSRR	power supply rejection ratio	$f < 50\text{ kHz}$	[1] -	55	-	dB
$\alpha_{ct(DC)}$	DC crosstalk between channels		-	-50	-	dB
Measurement output pin I_{om}; $V_{oc} = V_{oc(min)}$ to $V_{oc(max)}$						
$I_{om(offset)}$	offset current of measurement output (for three channels)	$I_{oc} = 0\text{ }\mu\text{A}$; $V_{om} = 1.8\text{ V}$ to 6 V	-50	-	+50	μA
$\Delta I_{om}/\Delta I_{oc}$	linearity of current transfer (for three channels)	$I_{oc} = -100\text{ }\mu\text{A}$ to $+100\text{ }\mu\text{A}$; $V_{om} = 1.8\text{ V}$ to 6 V	-0.9	-1.0	-1.1	
		$I_{oc} = -100\text{ }\mu\text{A}$ to $+10\text{ mA}$; $V_{om} = 1.8\text{ V}$ to 4 V	-0.9	-1.0	-1.1	
Output pins $V_{oc(1)}$, $V_{oc(2)}$, $V_{oc(3)}$						
$V_{oc(DC)}$	DC output voltage	$I_i = 0\text{ }\mu\text{A}$	76	87	97	V
$\Delta V_{oc(DC)(offset)}$	differential DC output offset voltage between two output pins	$I_i = 0\text{ }\mu\text{A}$	-5	0	+5	V
$\Delta V_{oc(T)}$	output voltage temperature drift		-	10	-	mV/K
$\Delta V_{oc(T)(offset)}$	differential output offset voltage temperature drift between two output pins		-	0	-	mV/K
$I_{oc(max)}$	maximum peak output current	$V_{oc} = 50\text{ V}$ to $V_{DD} - 50\text{ V}$	-	20	-	mA
$V_{oc(min)}$	minimum output voltage	$V_i = 4.5\text{ V}$; at $I_{oc} = 0\text{ mA}$	[2] -	-	10	V
$V_{oc(max)}$	maximum output voltage	$V_i = 0.5\text{ V}$; at $I_{oc} = 0\text{ mA}$	[2] $V_{DD} - 15$	-	-	V
B_S	small signal bandwidth	$V_{oc} = 60\text{ V}$ (p-p)	-	5.5	-	MHz
B_L	large signal bandwidth	$V_{oc} = 100\text{ V}$ (p-p)	-	4.5	-	MHz
$t_{co(p)}$	cathode output propagation time 50 % input to 50 % output	$V_{oc} = 100\text{ V}$ (p-p) square wave	[3] -	60	-	ns
$\Delta t_{co(p)}$	difference in cathode output propagation time 50 % input to 50 % output (between two output pins)	$V_{oc} = 100\text{ V}$ (p-p) square wave	[3] -10	0	+10	ns
$t_{oc(r)}$	cathode output rise time 10 % output to 90 % output	$V_{oc} = 50\text{ V}$ to 150 V square wave	[3] 67	91	113	ns
$t_{oc(f)}$	cathode output fall time 90 % output to 10 % output	$V_{oc} = 150\text{ V}$ to 50 V square wave	[3] 67	91	113	ns

Table 5: Characteristics ...continued

Operating range: $T_j = -20\text{ }^\circ\text{C}$ to $+150\text{ }^\circ\text{C}$; $V_{DD} = 180\text{ V}$ to 210 V ; test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{DD} = 200\text{ V}$; $V_{oc(1)} = V_{oc(2)} = V_{oc(3)} = \frac{1}{2}V_{DD}$; $C_L = 10\text{ pF}$ (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)} = 18\text{ K/W}$; measured in test circuit of [Figure 9](#); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{st}	settling time input (50 %) to output (99 % to 101 %)	$V_{oc} = 100\text{ V}$ (p-p) square wave	[3] -	-	350	ns
SR	slew rate between 50 V to $V_{DD} - 50\text{ V}$	$V_i = 2.5\text{ V}$ (p-p) square wave	[3] -	900	-	V/ μ s
O_v	cathode output voltage overshoot	$V_{oc} = 100\text{ V}$ (p-p) square wave	[3] -	2	-	%

- [1] The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.
- [2] See [Figure 6](#) for the typical DC-to-DC transfer of V_i to V_{oc} .
- [3] $f < 1\text{ MHz}$; $t_r = t_f = 40\text{ ns}$ [pins $V_{i(1)}$, $V_{i(2)}$ and $V_{i(3)}$]; see [Figure 7](#) and [Figure 8](#).

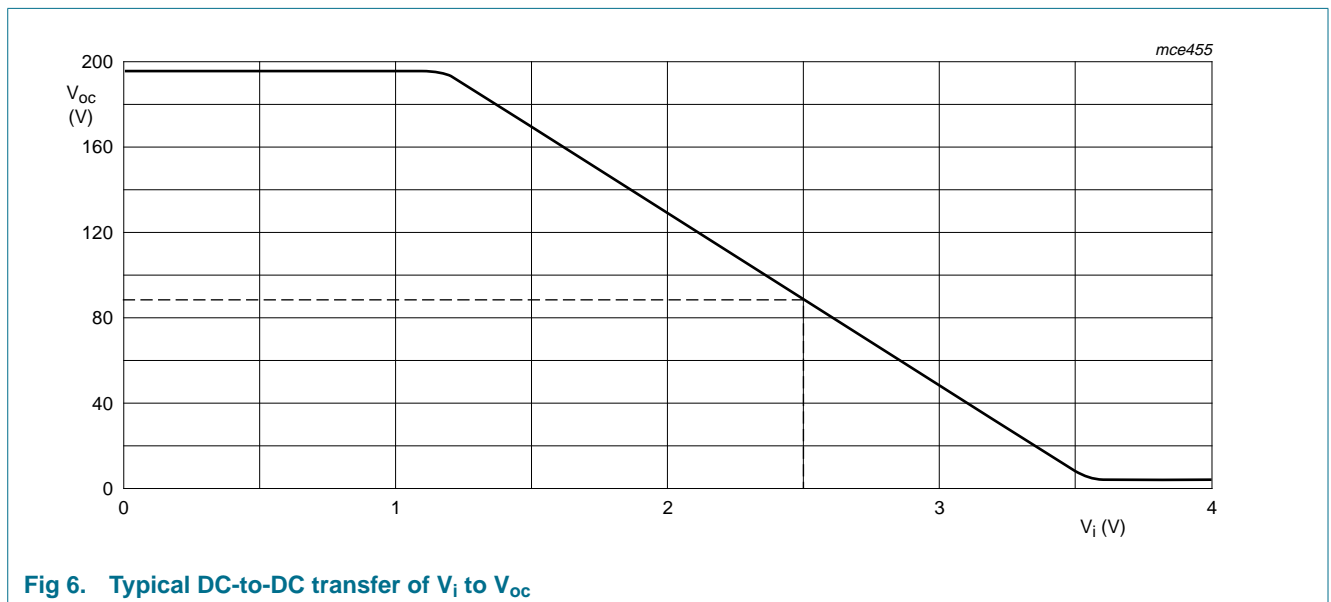


Fig 6. Typical DC-to-DC transfer of V_i to V_{oc}

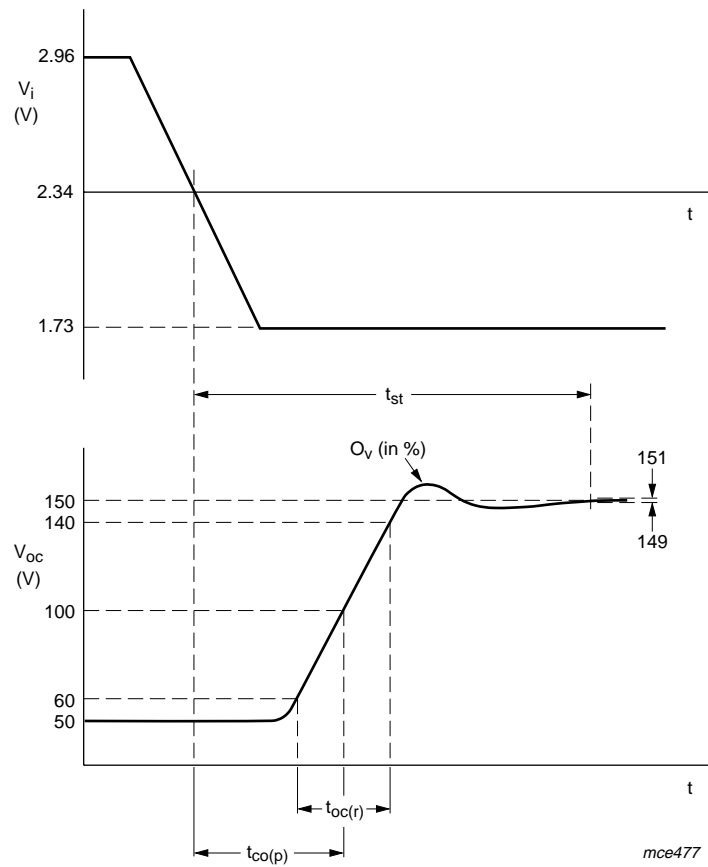


Fig 7. Output voltage [pins $V_{oc(1)}$, $V_{oc(2)}$ and $V_{oc(3)}$] rising edge as a function of the AC input signal

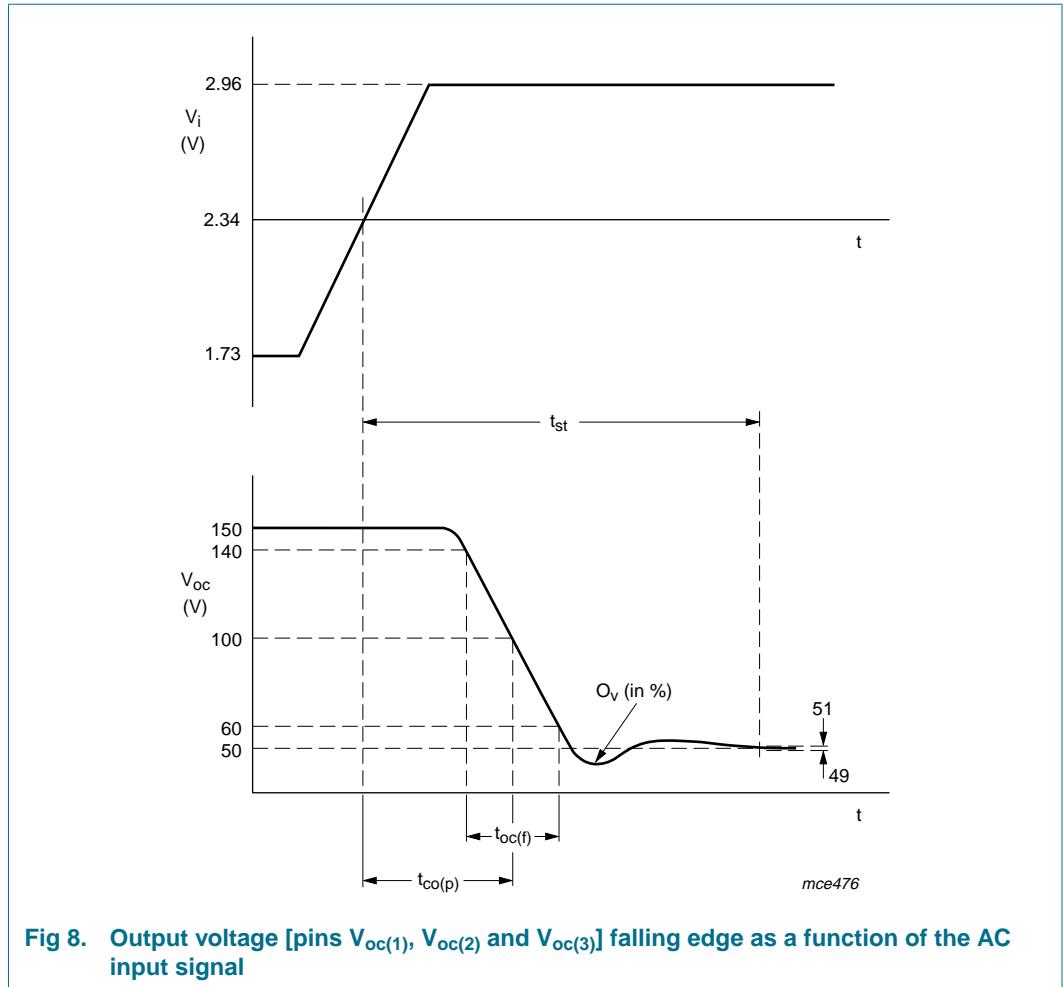


Fig 8. Output voltage [pins $V_{oc(1)}$, $V_{oc(2)}$ and $V_{oc(3)}$] falling edge as a function of the AC input signal

10. Application information

10.1 Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 3 A maximum with a charge content of 100 μC . External protection against higher currents is described in *Application note AN10227-01*.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 6 A maximum with a charge content of 100 nC. External protection against higher currents is described in *Application note AN10227-01*.

The DC voltage of pin V_{DD} must be within the operating range of 180 V to 210 V during the peak currents.

10.2 Flashover protection

The TDA6107AJF incorporates protection diodes against CRT flashover discharges that clamp the cathodes output voltage up to a maximum of $V_{DD} + V_d$.

To limit the diode current an external 1.5 k Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor value, the CRT has to be connected to the main PCB).

V_{DD} must be decoupled to GND:

1. With a capacitor > 20 nF with good HF behavior (e.g. foil); this capacitor must be placed as close as possible to pins V_{DD} and GND and must be within 5 mm.
2. With a capacitor > 3.3 μ F on the picture tube base print, depending on the CRT size.

10.3 Switch-off behavior

The switch-off behavior of the TDA6107AJF is controllable. This is because the output pins of the TDA6107AJF are still under control of the input pins for low power supply voltages (approximately 30 V and higher).

10.4 Bandwidth

The addition of the flash resistor produces a decreased bandwidth and increases the rise and fall times.

10.5 Dissipation

A distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6107AJF is due to voltage supply currents and load currents in the feedback network and CRT.

The static dissipation P_{stat} equals: $P_{stat} = V_{DD} \times I_{DD} + 3 \times V_{oc} \times I_{oc}$

Where:

V_{DD} = supply voltage

I_{DD} = supply current

V_{oc} = DC value of cathode output voltage

I_{oc} = DC value of cathode output current

The dynamic dissipation P_{dyn} equals: $P_{dyn} = 3 \times V_{DD} \times (C_L + C_{int}) \times f_i \times V_{oc(p-p)} \times \delta$

Where:

C_L = load capacitance

C_{int} = internal load capacitance (≈ 4 pF)

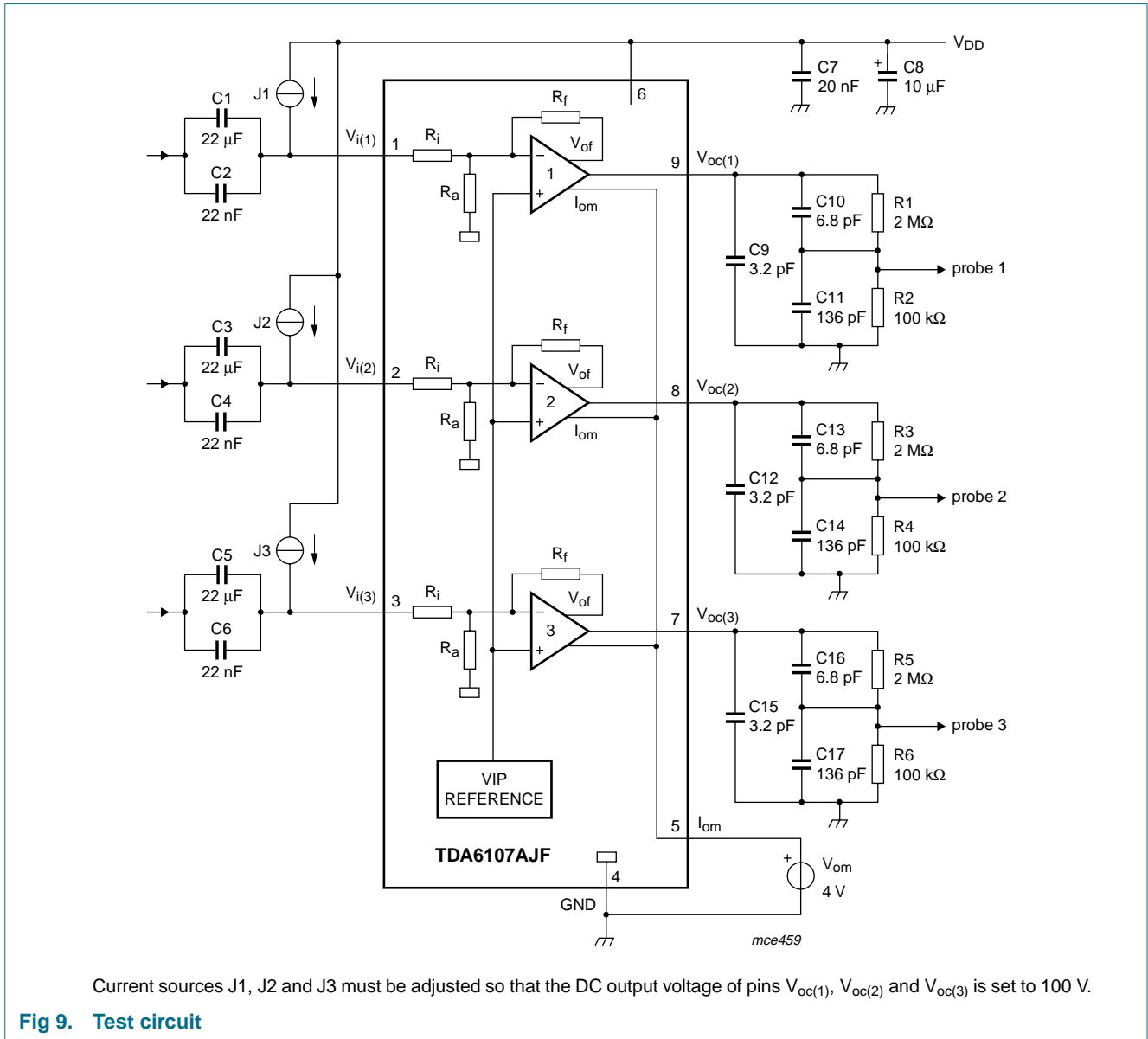
f_i = input frequency

$V_{oc(p-p)}$ = cathode output voltage (peak-to-peak value)

δ = non-blanking duty cycle

The TDA6107AJF must be mounted on the picture tube base print to minimize the load capacitance.

11. Test information



11.1 Quality information

The General Quality Specification for Integrated Circuits, SNW-FQ-611 is applicable.

12. Package outline

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads

SOT111-1

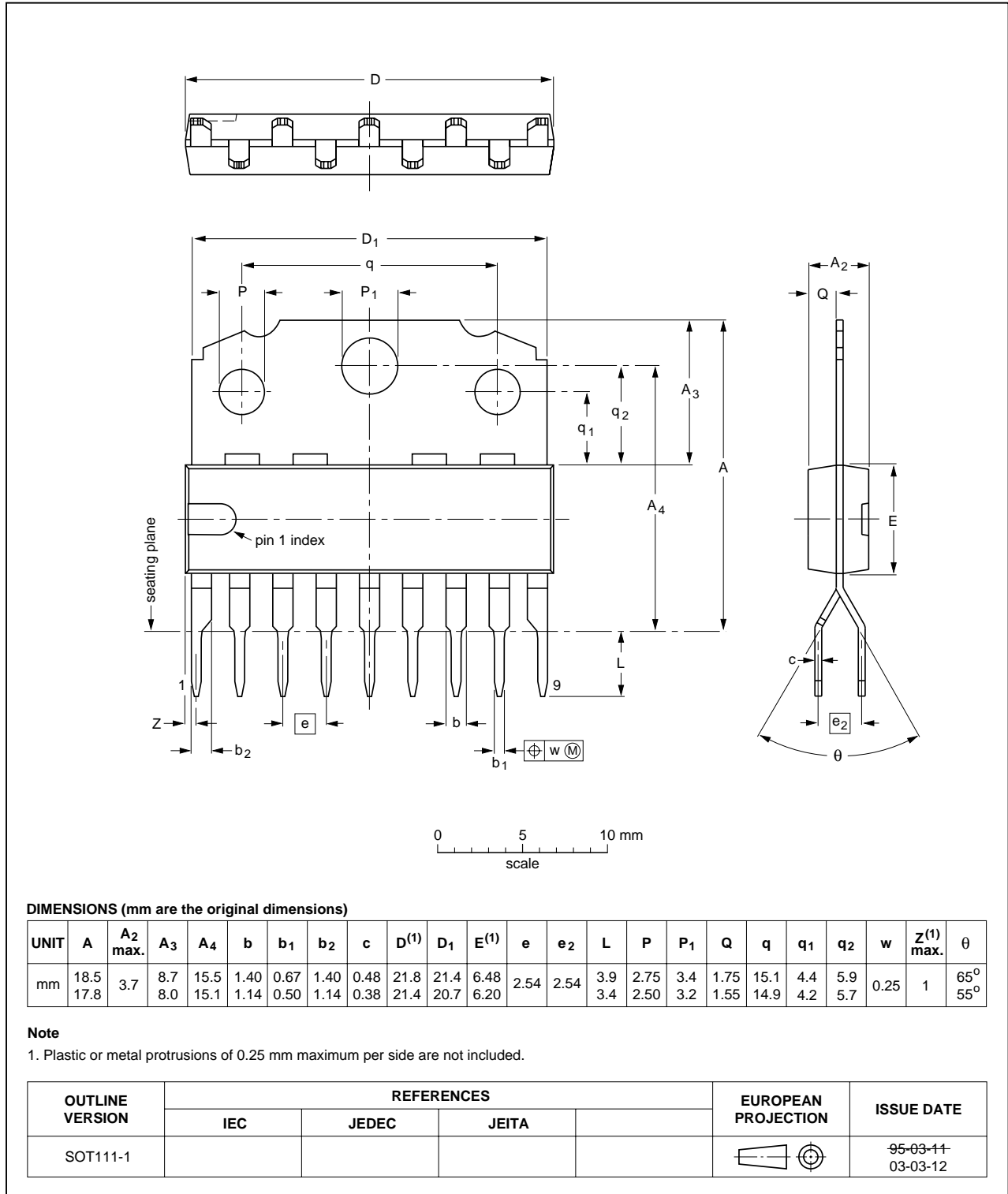


Fig 10. Package outline SOT 111-1 (DBS9MPF)

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13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

14. Soldering

14.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 6: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable [1]
PMFP [2]	–	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Revision history

Table 7: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA6107AJF_2	20050428	Product data sheet	-	9397 750 14728	TDA6107AJF_1
Modifications:		<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.• Changed data sheet status to product data sheet			
TDA6107AJF_1	20030919	Preliminary specification	-	9397 750 11632	-

16. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 28 April 2005
Document number: 9397 750 14728

Published in The Netherlands