Analog Power AM20N10-180D MOSFET Datasheet

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These miniature surface mount MOSFETs utilize a high cell density trench process to provide low rDS(on) and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and cordless telephones.

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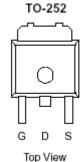
N-Channel 100-V (D-S) MOSFET

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PRODUCT SUMMARY			
$V_{DS}(V)$	$\mathbf{r}_{\mathrm{DS(on)}} \mathbf{m}(\Omega) \qquad \mathbf{I}_{\mathrm{D}} (A)$		
100	$180 @ V_{GS} = 10V$	14	
	190 @ V _{GS} = 4.5V	13	

- $\hbox{ Low $r_{DS(on)}$ provides higher efficiency and} \\ \hbox{ extends battery life}$
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current ^a	$T_C=25^{\circ}C$	I_D	14	A	
Pulsed Drain Current ^b		I_{DM}	36	A	
Continuous Source Current (Diode Conduction) ^a		I_S	30	A	
Power Dissipation ^a	$T_C=25^{\circ}C$	P_{D}	50	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	$R_{ heta JA}$	50	°C/W	
Maximum Junction-to-Case	$R_{ heta JC}$	3.0	°C/W	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
D		T C W.	Limits			TT .4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{\mathrm{DS}} = V_{\mathrm{GS}}, I_{\mathrm{D}} = 250\mathrm{uA}$	1			V	
Gate-Body Leakage	Igss	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			±100	nA	
Zara Cata Valtaga Drain Current	T	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25		
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	34			A	
D : G	rds(on)	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$			180	mΩ	
Drain-Source On-Resistance ^A		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			190		
Forward Tranconductance ^A	gfs	$V_{DS} = 40 \text{ V}, I_{D} = 2 \text{ A}$		4.4		S	
Diode Forward Voltage	V_{SD}	$I_S = 2 A, V_{GS} = 0 V$		1.1		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = 25 \text{ V}, V_{GS} = 5 \text{ V},$ $I_{D} = 2 \text{ A}$		10			
Gate-Source Charge	Q_{gs}			4		nC	
Gate-Drain Charge	Qgd	ID = 2 A		3			
Turn-On Delay Time	t _{d(on)}			5			
Rise Time	$t_{\rm r}$	$V_{\rm DD} = 100 \text{ V}, R_{\rm L} = 25 \Omega, I_{\rm D} = 2 \text{ A},$		3		nS	
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 \text{ V}$		30		113	
Fall-Time	tf			6			

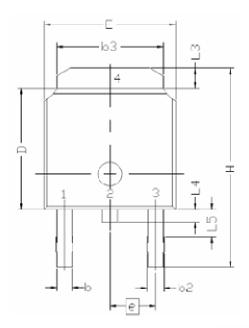
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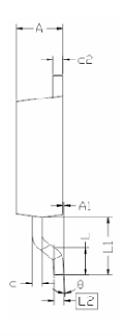
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Package Information





SYMBOL	DIMENS:		REQMTS
O IT IDEC	MIN	NDM	MAX
Ŀ	6.40	6.60	6.731
L	1.40	1.52	1.77
1			EF
L2	Û.	508 BS	C
L3	0.89		1.27
4	0.64		1.01
L5			
D	6.00	6.10	6.223
Н	9.40	10.00	10.40
b	0.64	0.76	0.88
p2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e A	2.	286 BS	C
Α	2.20	2.30	2.38
A1	0		0.127
	0.45	0.50	0.60
<5	0.45	0.50	0.58
D1	5.30		
E1	4.40		
ΘÎ	0*		10*

