National Semiconductor

December 2003

LP3999
Low Noise 150mA Voltage Regulator for RF/Analog Applications

General Description

The LP3999 regulator is designed to meet the requirements of portable wireless battery-powered applications and will provide an accurate output voltage with low noise and low quiescent current. Ideally suited for powering RF/Analog devices this device will also be used to meet more general circuit requirements.

For battery powered applications the low dropout and low ground current provided by the device allows the lifetime of the battery to be maximized.The inclusion of an Enable(disable) control can be used by the system to further extend the battery lifetime by reducing the power consumption to virtually zero. Should the application require a device with an active disable function please refer to device LP3995.

The LP3999 also features internal protection against short-circuit currents and over-temperature conditions.

The LP3999 is designed to be stable with small 1.0 µF ceramic capacitors. The small outline of the LP3999 micro SMD package with the required ceramic capacitors can realize a system application within minimal board area.

Performance is specified for a −40˚C to +125˚C temperature range.

The device is available in micro SMD package and LLP package. For other package options contact your local NSC sales office.

The device is available in fixed output voltages in the ranges of 1.5V to 3.3V. For availability, please contact your local NSC sales office.

Key Specifications

- 2.5V to 6.0V Input Range
- Accurate Output Voltage; ±75mV / 2%
- 60 mV Typical Dropout with 150 mA Load. V_{out} > 2.5V
- Virtually Zero Quiescent Current when Disabled
- 10 µVrms output noise over 10Hz to 100kHz
- Stable with a 1 µF Output Capacitor
- Guaranteed 150 mA Output Current
- Fast Turn-on Time; 140 µs (Typ.)

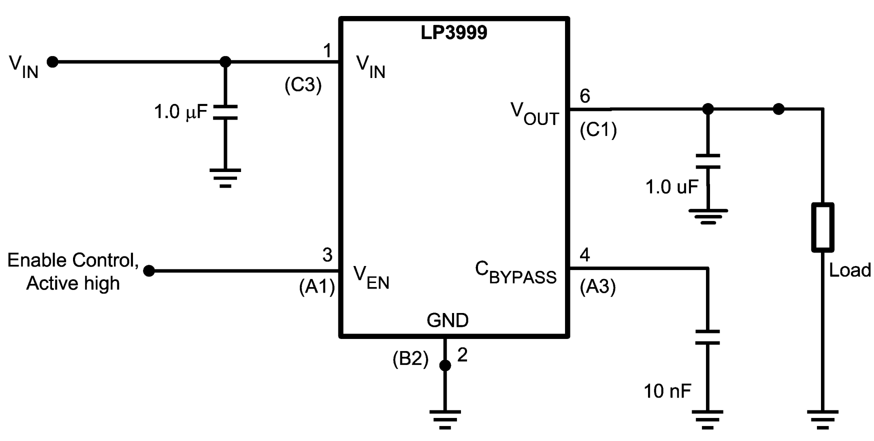
Features

- 5 pin micro SMD Package
- 6 pin LLP Package
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- Fast Turn-on
- Thermal-overload and short-circuit protection
- −40 to +125˚C junction temperature range for operation

Applications

- GSM Portable Phones
- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- Bluetooth Devices
- Portable Information Appliances
- Handheld MP3 Devices

Typical Application Circuit



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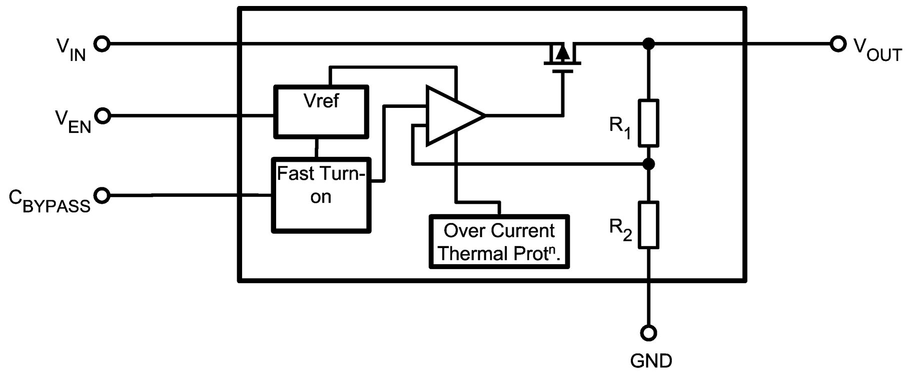
Block Diagram



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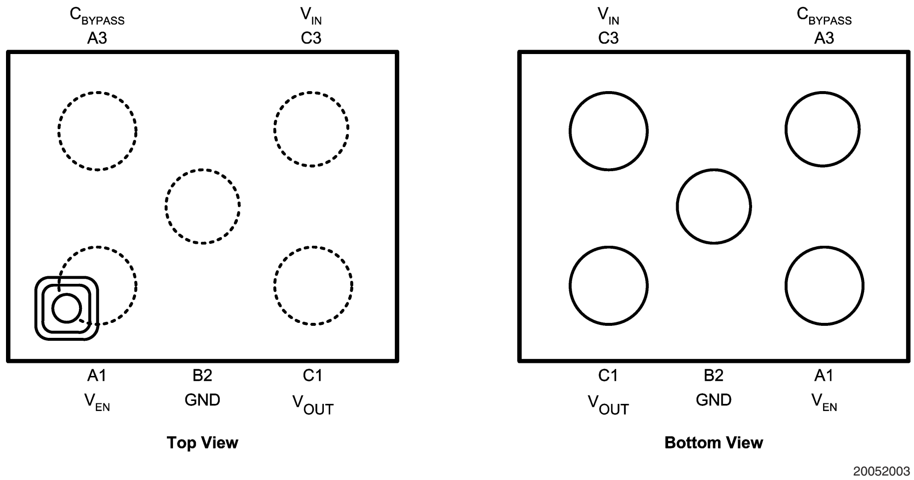
Pin Description

Package 5 pin micro SMD

Pin No.		Symbol	Name and Function
micro SMD	LLP		
A1	3	V_{EN}	Enable Input; Disables the Regulator when ≤ 0.4V. Enables the regulator when ≥ 0.9V
B2	2	GND	Common Ground
C1	6	V_{OUT}	Voltage output. Connect this output to the load circuit.
C3	1	V_{IN}	Voltage Supply Input
A3	4	C_{BYPASS}	Bypass Capacitor connection. Connect a 0.01 µF capacitor for noise reduction.
	5	N/C	No internal connection. There should not be any board connection to this pin.
	Pad	GND	Ground connection. Connect to ground plane for best thermal conduction.

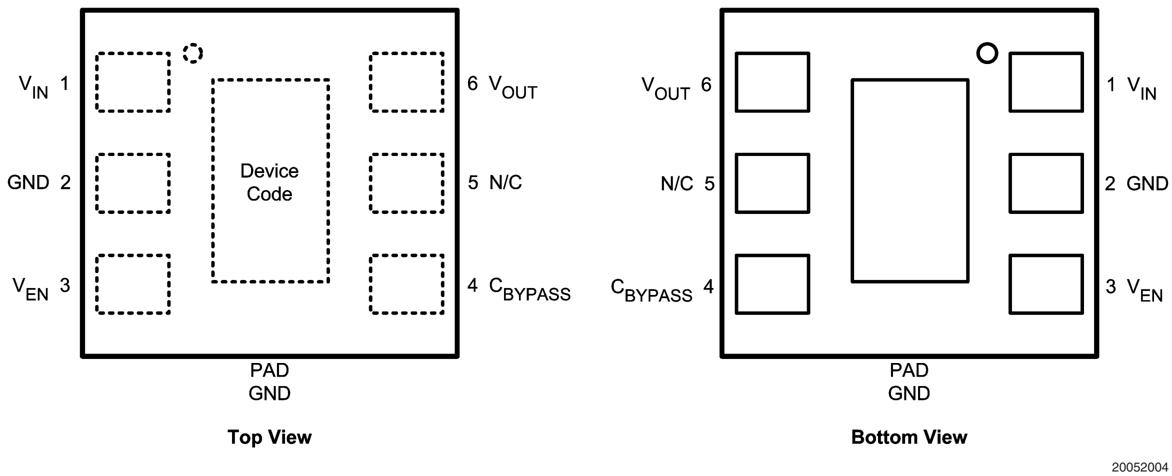
Connection Diagrams

micro SMD, 5 Bump Package



See NS Package Number TLA05

LLP-6 Package (SOT23 footprint)



See NS Package Number LDE06A

Ordering Information

For micro SMD Package

Output Voltage (V)	Grade	LP3999 Supplied as 250 Units, Tape and Reel	LP3999 Supplied as 3000 Units, Tape and Reel	Package Marking
1.5	STD	LP3999ITL-1.5	LP3999ITLX-1.5	
1.6 (Note 2)	STD	LP3999ITL-1.6	LP3999ITLX-1.6	
1.7(Note 2)	STD	LP3999ITL-1.7	LP3999ITLX-1.7	
1.8	STD	LP3999ITL-1.8	LP3999ITLX-1.8	
1.875	STD	LP3999ITL-1.875	LP3999ITLX-1.875	
1.9 (Note 2)	STD	LP3999ITL-1.9	LP3999ITLX-1.9	
2.0(Note 2)	STD	LP3999ITL-2.0	LP3999ITLX-2.0	
2.1 (Note 2)	STD	LP3999ITL-2.1	LP3999ITLX-2.1	
2.2(Note 2)	STD	LP3999ITL-2.2	LP3999ITLX-2.2	
2.4	STD	LP3999ITL-2.4	LP3999ITLX-2.4	
2.5	STD	LP3999ITL-2.5	LP3999ITLX-2.5	
2.6(Note 2)	STD	LP3999ITL-2.6	LP3999ITLX-2.6	
2.8	STD	LP3999ITL-2.8	LP3999ITLX-2.8	
3.0(Note 2)	STD	LP3999ITL-3.0	LP3999ITLX-3.0	
3.3	STD	LP3999ITL-3.3	LP3999ITLX-3.3	

For micro SMD Package UNLEADED

Output Voltage (V)	Grade	LP3999 Supplied as 250 Units, Tape and Reel	LP3999 Supplied as 3000 Units, Tape and Reel	Package Marking
1.5 (Note 2)	STD	LP3999ITL-1.5 NOPB	LP3999ITLX-1.5 NOPB	
1.6 (Note 2)	STD	LP3999ITL-1.6 NOPB	LP3999ITLX-1.6 NOPB	
1.7 (Note 2)	STD	LP3999ITL-1.7 NOPB	LP3999ITLX-1.7 NOPB	
1.8 (Note 2)	STD	LP3999ITL-1.8 NOPB	LP3999ITLX-1.8 NOPB	
1.875 (Note 2)	STD	LP3999ITL-1.875 NOPB	LP3999ITLX-1.875 NOPB	
1.9 (Note 2)	STD	LP3999ITL-1.9 NOPB	LP3999ITLX-1.9 NOPB	
2.0(Note 2)	STD	LP3999ITL-2.0 NOPB	LP3999ITLX-2.0 NOPB	
2.1 (Note 2)	STD	LP3999ITL-2.1 NOPB	LP3999ITLX-2.1 NOPB	
2.2(Note 2)	STD	LP3999ITL-2.2 NOPB	LP3999ITLX-2.2 NOPB	
2.4 (Note 2)	STD	LP3999ITL-2.4 NOPB	LP3999ITLX-2.4 NOPB	
2.5 (Note 2)	STD	LP3999ITL-2.5 NOPB	LP3999ITLX-2.5 NOPB	
2.6(Note 2)	STD	LP3999ITL-2.6 NOPB	LP3999ITLX-2.6 NOPB	
2.8 (Note 2)	STD	LP3999ITL-2.8 NOPB	LP3999ITLX-2.8 NOPB	
3.0(Note 2)	STD	LP3999ITL-3.0 NOPB	LP3999ITLX-3.0 NOPB	
3.3(Note 2)	STD	LP3999ITL-3.3 NOPB	LP3999ITLX-3.3 NOPB	

Ordering Information (Continued)

For LLP-6 Package

Output Voltage (V)	Grade	LP3999 Supplied as 1000 Units, Tape and Reel	LP3999 Supplied as 4500 Units, Tape and Reel	Package Marking
1.5 (Note 2)	STD	LP3999ILD-1.5	LP3999ILDX-1.5	L032B
1.6(Note 2)	STD	LP3999ILD-1.6	LP3999ILDX-1.6	L033B
1.8 (Note 2)	STD	LP3999ILD-1.8	LP3999ILDX-1.8	L034B
1.875(Note 2)	STD	LP3999ILD-1.875	LP3999ILDX-1.875	
1.9 (Note 2)	STD	LP3999ILD-1.9	LP3999ILDX-1.9	L035B
2..0 (Note 2)	STD	LP3999ILD-2.0	LP3999ILDX-2.0	
2.1 (Note 2)	STD	LP3999ILD-2.1	LP3999ILDX-2.1	L036B
2.2 (Note 2)	STD	LP3999ILD-2.2	LP3999ILDX-2.2	
2.4 (Note 2)	STD	LP3999ILD-2.4	LP3999ILDX-2.4	
2.5 (Note 2)	STD	LP3999ILD-2.5	LP3999ILDX-2.5	L037B
2.6 (Note 2)	STD	LP3999ILD-2.6	LP3999ILDX-2.6	
2.8 (Note 2)	STD	LP3999ILD-2.8	LP3999ILDX-2.8	L038B
3.0 (Note 2)	STD	LP3999ILD-3.0	LP3999ILDX-3.0	L039B
3.3 (Note 2)	STD	LP3999ILD-3.3	LP3999ILDX-3.3	L040B

Note 1: Available in sample quantities only

Note 2: For availability contact your local sales office

Absolute Maximum Ratings

(Notes 3, 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage (V_{IN})	–0.3 to 6.5V
Output Voltage	–0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Enable Input Voltage	–0.3 to 6.5V
Junction Temperature	150˚C
Lead/Pad Temperature (Note 5)	
LLP	235˚C
microSMD	260˚C
Storage Temperature	–65 to +150˚C
Continuous Power Dissipation (Note 6)	Internally limited
ESD (Note 9)	
Human Body Model	2 kV
Machine Model	200V

Operating Ratings (Note 3)

Input Voltage (V_{IN})	2.5 to 6.0V
Enable Input Voltage	0 to 6.0V
Junction Temperature	–40 to +125˚C
Ambient Temperature Range (Note 7)	-40 to 85˚C

Thermal Properties(Note 8)

Junction to Ambient Thermal Resistance	
θ_{JA} (LLP pkg.)	88˚C/W
θ_{JA} (micro SMD pkg.)	255˚C/W

Electrical Characteristics

Unless otherwise noted, V_{EN} = 1.5, V_{IN} = $V_{OUT(NOM)}$ + 1.0V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF, c_{BP} = 0.01 µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the full temperature range for operation, –40 to +125˚C. (Note 13)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{IN}	Input Voltage			2.5	6.0	V
DEVICE OUTPUT: 1.5 ≤ V_{OUT} < 1.8V						
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1 mA		–50	50	mV
				-75	**75**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$+1.0V) to 6.0V, I_{OUT} = 1 mA		**–3.5**	**3.5**	mV/V
	micro SMD Load Regulation Error	I_{OUT} = 1 mA to 150 mA	10		**75**	µV/mA
	LLP Load Regulation Error	I_{OUT} = 1 mA to 150 mA	70		**125**	µV/mA
PSRR	Power Supply Rejection Ratio (Note 11)	f = 1 kHz, I_{OUT} = 1 mA	58			dB
		f = 10 kHz, I_{OUT} = 1 mA	58			
DEVICE OUTPUT: 1.8 ≤ V_{OUT} < 2.5V						
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1 mA		-50	50	mV
				–75	**75**	
	microSMD Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$+1.0V) to 6.0V, I_{OUT} = 1 mA		**–2.5**	**2.5**	mV/V
	LLP Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$+1.0V) to 6.0V, I_{OUT} = 1 mA		**–3.5**	**3.5**	mV/V
	micro SMD Load Regulation Error	I_{OUT} = 1 mA to 150 mA	10		**75**	µV/mA
	LLP Load Regulation Error	I_{OUT} = 1 mA to 150 mA	80		**125**	µV/mA
PSRR	Power Supply Rejection Ratio (Note 11)	f = 1 kHz, I_{OUT} = 1 mA	60			dB
		f = 10 kHz, I_{OUT} = 1 mA	60			

Electrical Characteristics (Continued)

Unless otherwise noted, V_{EN} = 1.5, V_{IN} = $V_{OUT(NOM)}$ + 1.0V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF, c_{BP} = 0.01 µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125˚C. (Note 13)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
DEVICE OUTPUT: 2.5 ≤ V_{OUT} ≤ 3.3V						
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1 mA		-2	2	% of $V_{OUT(NOM)}$
				−3	**3**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$+1.0V) to 6.0V, I_{OUT} = 1 mA		**−0.1**	**0.1**	%/V
	micro SMD Load Regulation Error	I_{OUT} = 1 mA to 150 mA	0.0004		**0.002**	%/mA
	LLP Load Regulation Error	I_{OUT} = 1 mA to 150 mA	0.003			%/mA
	Dropout Voltage	I_{OUT} = 1 mA	0.4		**2**	mV
		I_{OUT} = 150 mA	60		**100**	
PSRR	Power Supply Rejection Ratio (Note 11)	f = 1 kHz, I_{OUT} = 1 mA	60			dB
		f = 10 kHz, I_{OUT} = 1 mA	50			
FULL V_{OUT} RANGE						
I_{LOAD}	Load Current	(Notes 10, 11)		0		µA
I_Q	Quiescent Current	V_{EN} = 1.5V, I_{OUT} = 0 mA	85		**150**	µA
		V_{EN} = 1.5V, I_{OUT} = 150 mA	140		**200**	
		V_{EN} = 0.4V	0.003		**1.5**	
I_{SC}	Short Circuit Current Limit		450			mA
E_N	Output Noise Voltage ((Note 11))	BW = 10 Hz to 100 kHz, V_{IN} = 4.2V, No Load	10			µVrms
		BW = 10 Hz to 100 kHz, V_{IN} = 4.2V, 1mA Load	30			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature	160			˚C
		Hysteresis	20			
ENABLE CONTROL CHARACTERISTICS						
I_{EN}	Maximum Input Current at V_{EN} Input	V_{EN} = 0.0V and V_{IN} = 6.0V	0.001			µA
V_{IL}	Low Input Threshold				**0.4**	V
V_{IH}	High Input Threshold			**0.9**		V
TIMING CHARACTERISTICS						
T_{ON}	Turn On Time (Note 11)	To 95% Level (Note 12)	140			µs

Note 3: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 4: All voltages are with respect to the potential at the GND pin.

Note 5: For further information on these packages please refer to the following application notes;

AN-1112 Micro SMD Package Wafer Level Chip Scale Package,

AN-1187. Leadless Leadframe Package.

Note 6: Internal Thermal shutdown circuitry protects the device from permanent damage.

Note 7: In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$), the maximum power dissipation ($P_{D(max)}$), and the junction to ambient thermal resistance in the application (θ_{JA}). This relationship is given by :-

$$T_{A(max)} = T_{J(max-op)} - (P_{D(max)} \times \theta_{JA})$$

Note 8: Junction to ambient thermal resistance is highly dependant on the application and board layout. In applications where high thermal dissipation is possible, special care must be paid to thermal issues in the board design.

Note 9: The human body is 100 pF discharge through 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 10: The device maintains the regulated output voltage without load.

Note 11: This electrical specification is guaranteed by design.

Note 12: Time from V_{EN} = 0.9V to V_{OUT} = 95% ($V_{OUT(NOM)}$)

Electrical Characteristics (Continued)

Note 13: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25˚C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 14: $V_{OUT(NOM)}$ is the stated output voltage option for the device.

Recommended Output Capacitor

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitor	Capacitance (Note 15)	1.0	0.75		µF
		ESR		5	500	mΩ

Note 15: The capacitor tolerance should be 30% or better over temperature. Recommended capacitor type is X7R however dependant on application X5R,Y5V and Z5U can also be used.

Input Test Signals

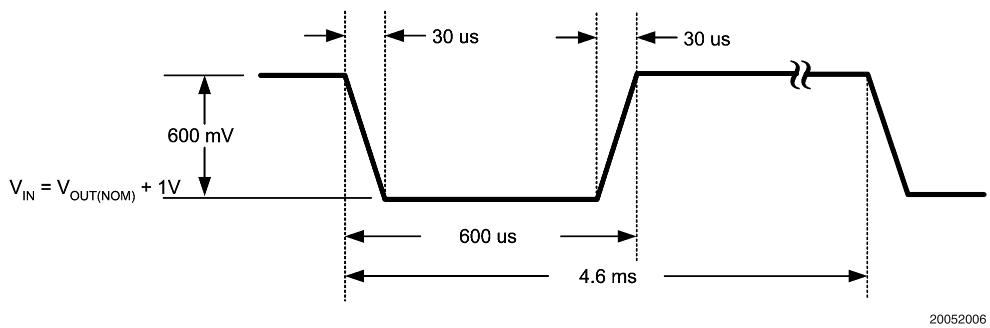


FIGURE 1. Line Transient Response Input Test Signal

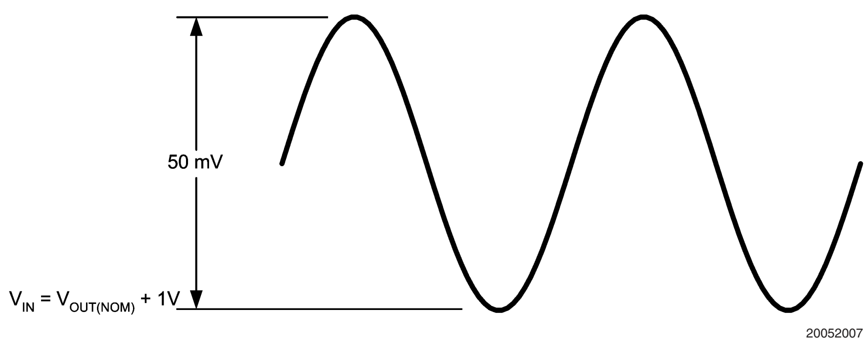
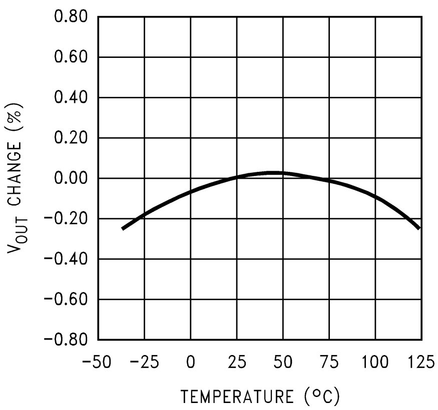


FIGURE 2. PSRR Input Test Signal

Typical Performance Characteristics

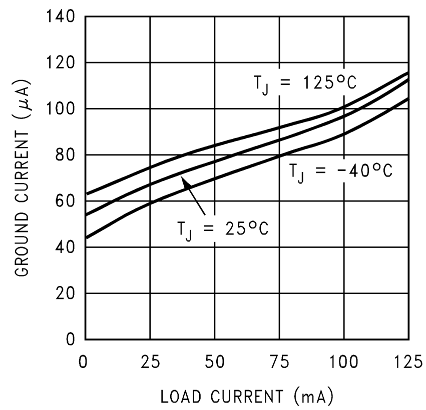
Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\ \mu F$ Ceramic, $V_{IN} = V_{OUT} + 1.0V$, $T_A = 25^\circ C$, Enable pin is tied to V_{IN}.

Output Voltage Change vs Temperature



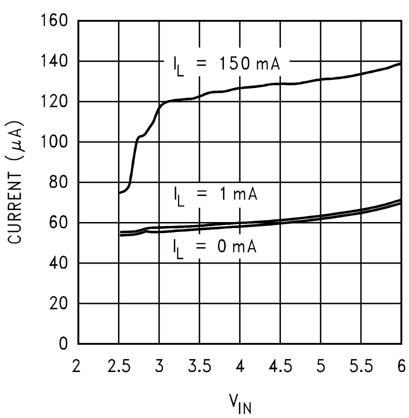
20052010

Ground Current vs Load Current (1.8V V_{OUT})



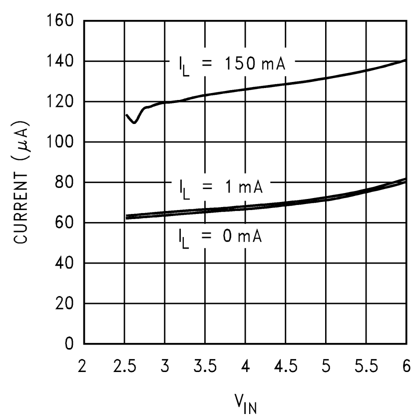
20052011

Ground Current vs V_{IN} @ 25˚C



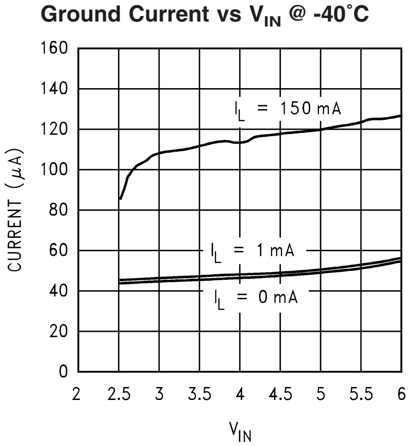
20052014

Ground Current vs V_{IN} @125˚C



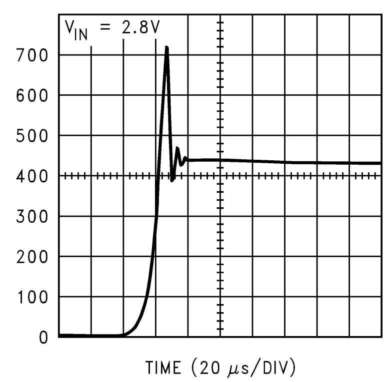
20052015

Ground Current vs V_{IN} @ -40˚C



20052013

Short Circuit Current

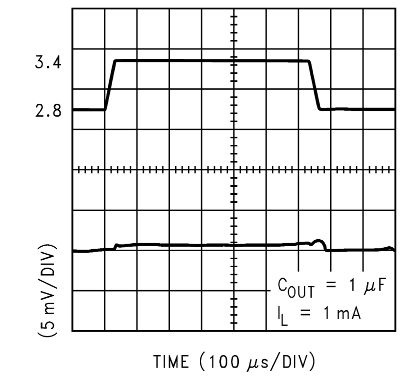


20052016

Typical Performance Characteristics

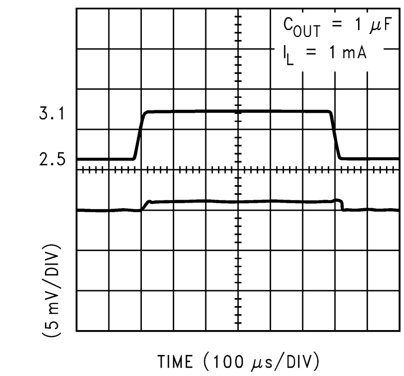
Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\ \mu F$ Ceramic, $V_{IN} = V_{OUT} + 1.0V$, $T_A = 25^\circ C$, Enable pin is tied to V_{IN}. (Continued)

Line Transient Response (1.8V V_{OUT})



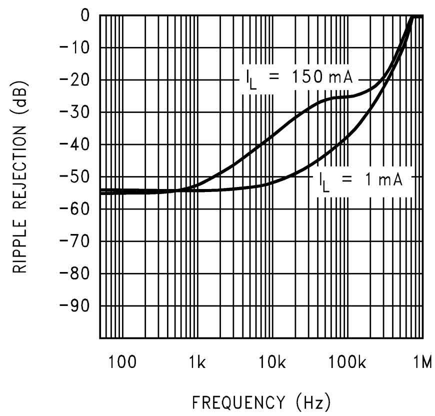
20052018

Line Transient Response (1.5V V_{OUT})



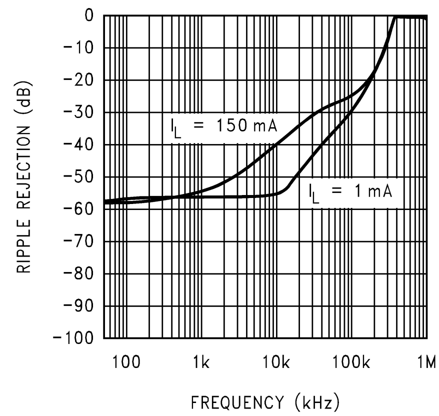
20052017

Ripple Rejection (1.8V V_{OUT})



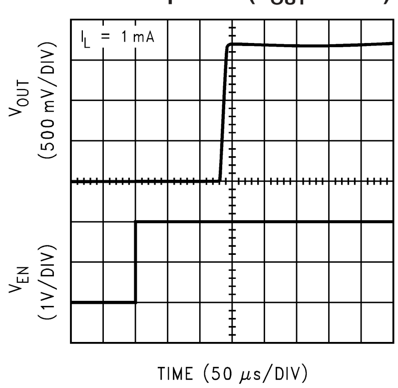
20052019

Ripple Rejection (1.5V V_{OUT})



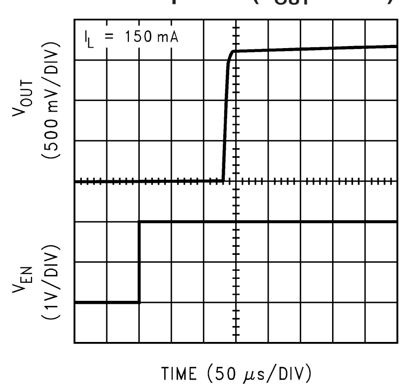
20052020

Enable Start-Up Time (V_{OUT} = 1.8V)



20052030

Enable Start-Up Time (V_{OUT} = 1.8V)

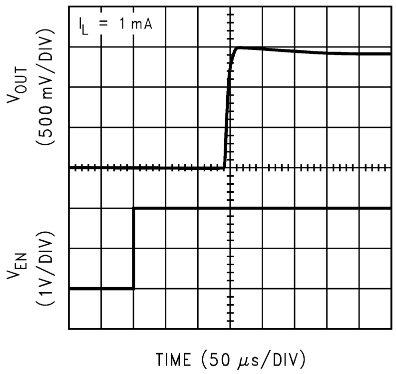


20052031

Typical Performance Characteristics

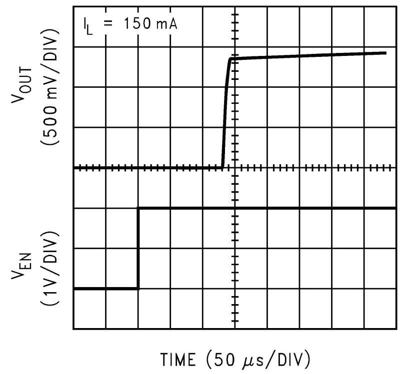
Unless otherwise specified, C_{IN} = C_{OUT} = 1.0 µF Ceramic, V_{IN} = V_{OUT} + 1.0V, T_A = 25˚C, Enable pin is tied to V_{IN}. (Continued)

Enable Start-Up Time (V_{OUT} = 1.5V)



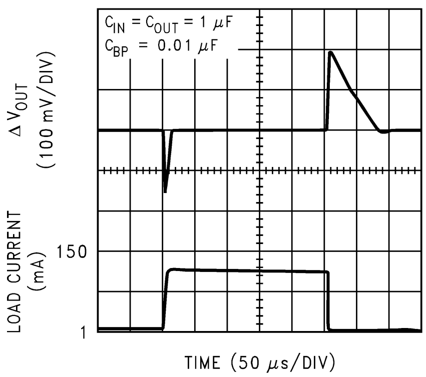
20052032

Enable Start-Up Time (V_{OUT} = 1.5V)



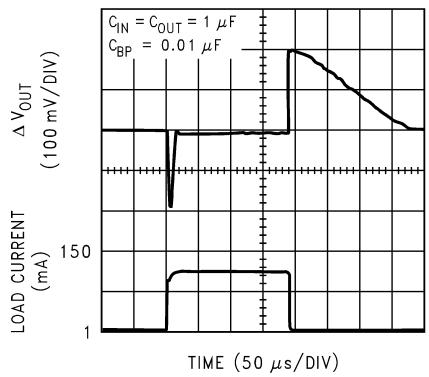
20052033

Load Transient Response (V_{OUT} = 1.8V)



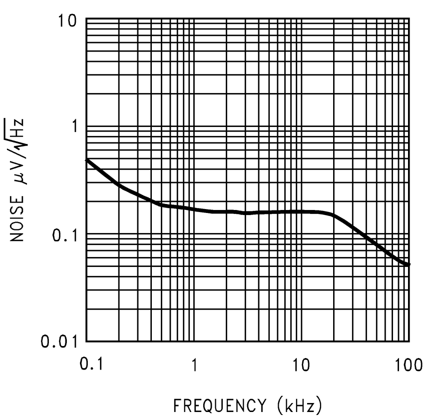
20052022

Load Transient Response (V_{OUT} = 1.5V)



20052021

Output Noise Density V_{IN} = 4.2V V_{OUT} = 2.5V)



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Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in (Note 7) in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

With a θ_{JA} = 255˚C/W, the device in the micro SMD package returns a value of 392 mW with a maximum junction temperature of 125˚C.

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}.$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

In common with most regulators, the LP3999 requires external capacitors to ensure stable operation. The LP3999 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0 µF capacitor be connected between the LP3999 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the **ESR** (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0 µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3999 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 1.0 [to 10 µF] range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP3999 application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

NO-LOAD STABILITY

The LP3999 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3999 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3999.

The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25˚C to 85˚C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to −40˚C, so some guard band must be allowed.

NOISE BYPASS CAPACITOR

A bypass capacitor should be connected between the C_{BYPASS} pin and ground to significantly reduce the noise at the regulator output. This device pin connects directly to a high impedance node within the bandgap reference circuitry. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The use of a 0.01µF bypass capacitor is strongly recommended to prevent overshoot on the output during start-up.

Application Hints (Continued)

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High quality ceramic capacitors with NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO's, the addition of a noise reduction capacitor does not effect the transient response of the device.

ENABLE OPERATION

The LP3999 may be switched ON or OFF by a logic input at the ENABLE pin, V_{EN}. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. If the application does not require the shutdown feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST TURN ON

Fast turn-on is guaranteed by control circuitry within the reference block allowing a very fast ramp of the output voltage to reach the target voltage. There is no active turn-off on this device. Refer to LP3995 for a similar device with active turn-off.

micro SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note AN-1112.

Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

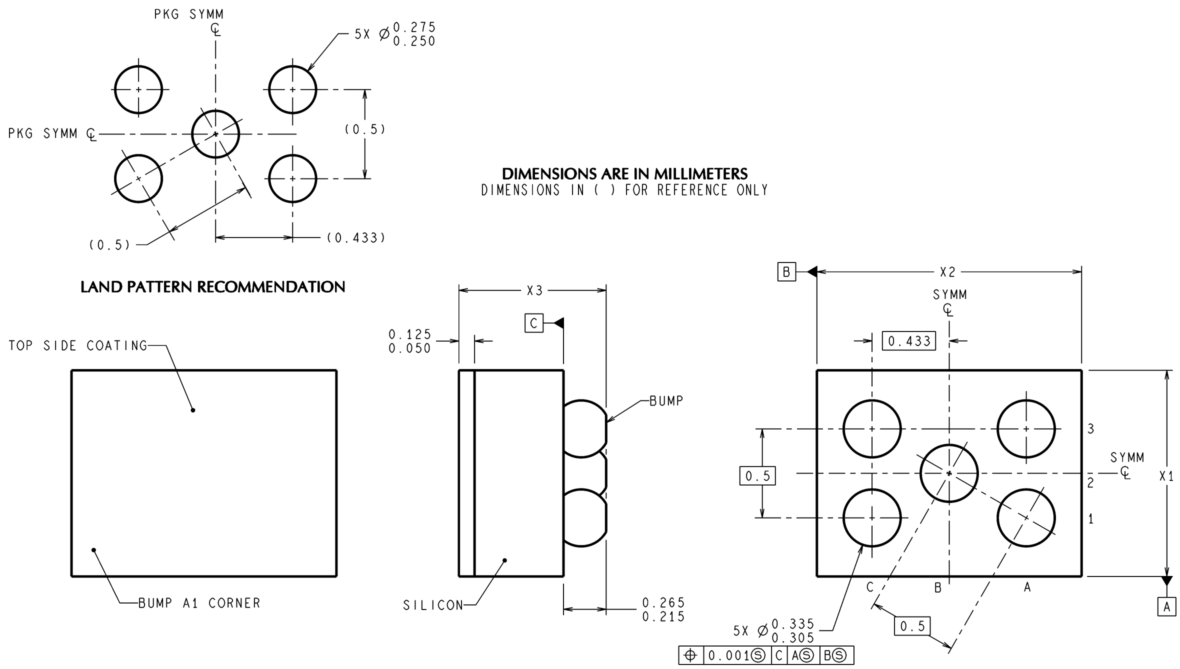
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

micro SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight will cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum have the most detrimental effect thus the fluorescent lighting used inside most buildings has very little effect on performance. Tests carried out on a micro SMD test board showed a negligible effect on the regulated output voltage when brought within 1 cm of a fluorescent lamp. A deviation of less than 0.1% from nominal output voltage was observed.

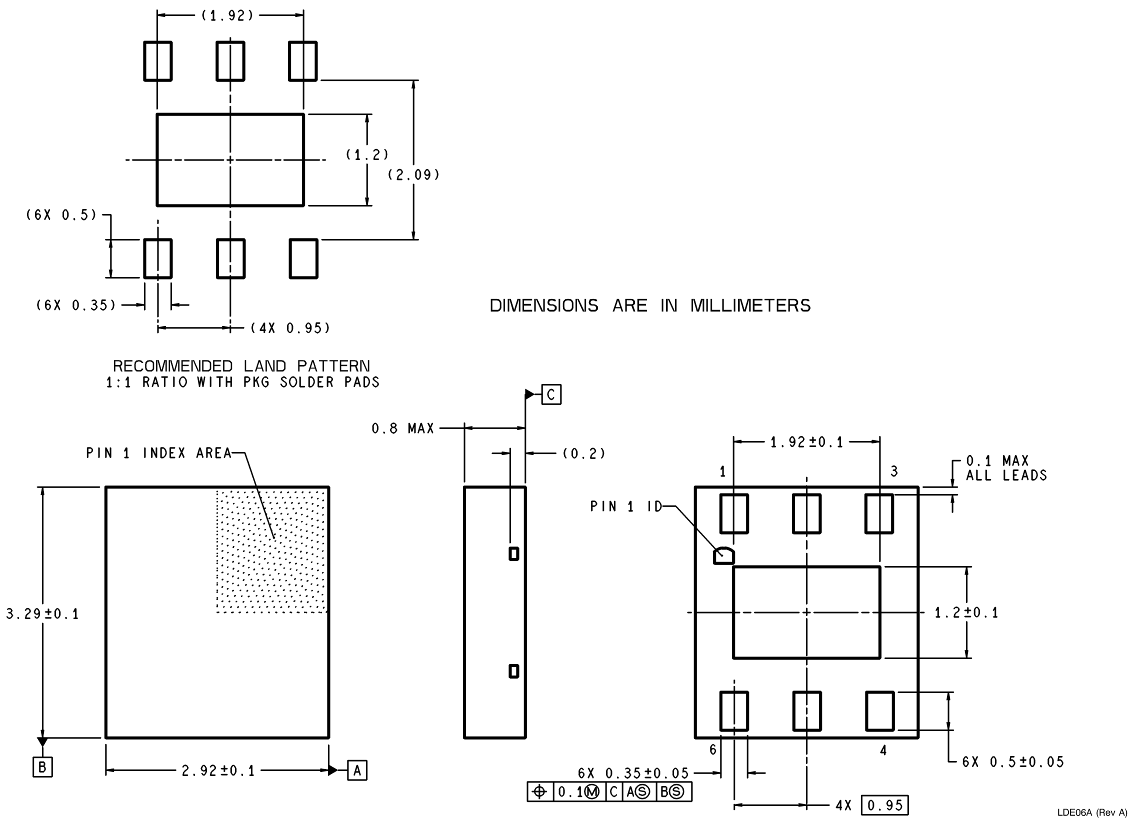
Physical Dimensions inches (millimeters) unless otherwise noted



TLA05XXX (Rev B)

micro SMD, 5 Bump, Package (TLA05)
NS Package Number TLA05ADA
The dimensions for X1, X2 and X3 are given as:
X1 = 1.006 +/– 0.03mm
X2 = 1.438 +/– 0.03mm
X3 = 0.600 +/– 0.075mm

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LLP, 6 Lead, Package (SOT23 Land)
NS Package Number LDE06A

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