19-5303; Rev 0; 6/10

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

概述

MAX2063高线性度、双通道数字调节可变增益放大器(VGA)工作在50MHz至1000MHz频率范围。可通过SPI™兼容接口控制作为从机外设的每路数字衰减器；也允许以1dB步长通过5位并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择，可直接设置在4种增益选项的一种，用户可通过SPI接口预先设置四种增益选项。2个独立的控制引脚允许用户快速选择4种定制衰减状态的任何一个，无需对SPI总线重新编程。

因为每一级电路都具有外部RF输入和RF输出，通过适当配置可以优化噪声系数(放大器配置为第一级)或OIP3（放大器配置为最后一级)。该器件还包含增益为24dB的放大器(放大器本身)，增益最大时噪声系数(NF)为5.6dB（包括衰减器的插入损耗)，并提供+41dBm的高OIP3。这些特性使得该器件成为多通道接收器和发射器应用理想的VGA选择。

此外，器件采用+5V单电源供电时具有最优的性能；工作在+3.3V单电源时，具有先进的省电模式，但性能指标略有降低。器件采用紧凑、带裸焊盘的48引脚、薄型QFN封装(7mm x 7mm)，在扩展级温度范围(T_C = -40°C至+85°C)内确保电气特性。

应用

IF和RF增益级设计

温度补偿电路

蜂窝频段WCDMA和cdma2000®基站

GSM 850/GSM 900 EDGE基站

WiMAX™和LTE基站及用户端企业设备

固定宽带无线接入

无线本地环路

军用系统

特性

- ♦ 两个通道可独立控制
- ♦ 50MHz至1000MHz RF频率范围
- ♦ 引脚兼容系列器件包括
  - MAX2062 (模拟/数字VGA)
  - MAX2064 (模拟VGA)
- ♦ 21.3dB (典型值)最大增益
- ♦ 100MHz带宽内保持0.25dB的增益平坦度
- ♦ 31dB增益范围
- ♦ 200MHz频率下具有58dB通道隔离
- ♦ 支持4种“速射”预编程衰减设置选项
  - 快速设置4种定制衰减状态之一，无需对SPI总线重新编程
  - 理想用于快速响应和大信号阻塞保护
  - 避免ADC过驱动
- ♦ 200MHz时具有优异的线性特性
  - +41dBm OIP3
  - +56dBm OIP2
  - 输出1dB压缩点为+19dBm
- ♦ 5.6dB典型噪声系数
- ♦ 25ns数字切换时间
- ♦ 超低失真VGA摆幅具有0.05dB的过冲/下冲
- ♦ +5V单电源供电(可选择+3.3V供电)
- ♦ 放大器关断模式支持TDD应用

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2063ETM+	-40°C to +85°C	48 Thin QFN-EP*
MAX2063ETM+T	-40°C to +85°C	48 Thin QFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
T = 卷带包装。

SPI是Motorola, Inc.的商标。
cdma2000是电信工业协会的注册商标。
WiMAX是WiMAX论坛的商标。

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_AMP\_1}$, $V_{CC\_AMP\_2}$, V_{CC_RG} to GND .....-0.3V to +5.5V
STA_A_1, STA_A_2, STA_B_1, STA_B_2, PD_1, PD_2, AMPSET to GND .....-0.3V to +3.6V
DAT, $\overline{CS}$, CLK, DA_SP to GND .....-0.3V to +3.6V
D0_1, D1_1, D2_1, D3_1, D4_1, D0_2, D1_2, D2_2, D3_2, D4_2 to GND.....-0.3V to +3.6V
AMP_IN_1, AMP_IN_2 to GND.....+0.95V to +1.2V
AMP_OUT_1, AMP_OUT_2 to GND .....-0.3V to +5.5V
D_ATT_IN_1, D_ATT_IN_2, D_ATT_OUT_1, D_ATT_OUT_2 to GND.....0V to +3.6V
REG_OUT to GND.....-0.3V to +3.6V
RF Input Power (D_ATT_IN_1, D_ATT_IN_2) ..... +20dBm
RF Input Power (AMP_IN_1, AMP_IN_2)..... +18dBm
θ_{JC} (Notes 1, 2)..... +12.3°C/W
θ_{JA} (Notes 2, 3)..... +38°C/W
Continuous Power Dissipation (Note 1) 5.3W
Operating Case Temperature Range (Note 4) .. -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = +4.75V to +5.25V, AMPSET = 0, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = +5.0V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{DC}			148	205	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		5.2	8	mA
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		1.7		3.465	V
Input Logic Current	I_{IH}, I_{IL}		-1		+1	µA

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = +3.135V to +3.465V, AMPSET = 1, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.135	3.3	3.465	V
Supply Current	I_{DC}			88	145	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		4.3	8	mA
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		1.7		3.465	V

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 5)	50		1000	MHz

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G	f_{RF} = 50MHz		22.0		dB
		f_{RF} = 100MHz		21.7		
		f_{RF} = 200MHz		21.3		
		f_{RF} = 350MHz, T_C = +25°C	18	21.0	23	
		f_{RF} = 450MHz		20.8		
		f_{RF} = 750MHz		19.9		
		f_{RF} = 900MHz		18.3		
Gain vs. Temperature				-0.006		dB/°C
Gain Flatness vs. Frequency		From 100MHz to 200MHz		0.35		dB
		Any 100MHz frequency band from 200MHz to 500MHz		0.25		
Noise Figure	NF	f_{RF} = 50MHz		5.2		dB
		f_{RF} = 100MHz		5.4		
		f_{RF} = 200MHz		5.6		
		f_{RF} = 350MHz		5.8		
		f_{RF} = 450MHz		5.9		
		f_{RF} = 750MHz		6.4		
		f_{RF} = 900MHz		6.7		
Total Attenuation Range				30.8		dB
Output Second-Order Intercept Point (Minimum Attenuation)	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$		51.6		dBm
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.8		dB
		RF input 2 amplified power measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		49.4		

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 50MHz			47.1		dBm
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 100MHz			43.9		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 200MHz			41.0		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 350MHz			37.0		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 450MHz			35.2		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 750MHz			28.7		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 900MHz			26.5		
Output -1dB Compression Point	P_{1dB}	(Note 7)			18.8		dBm
Second Harmonic	HD2	P_{OUT} = +3dBm			-54.8		dBc
Third Harmonic	HD3	P_{OUT} = +3dBm			-72.9		dBc
Group Delay		Includes EV kit PCB delays			0.87		ns
Amplifier Power-Down Time		PD_1 or PD_2 from 0 to 1, amplifier DC supply current settles to within 0.1mA			0.5		µs
Amplifier Power-Up Time		PD_1 or PD_2 from 1 to 0, amplifier DC supply current settles to within 1%			0.5		µs
Input Return Loss	RL_{IN}	50Ω source			23.3		dB
Output Return Loss	RL_{OUT}	50Ω load			24.4		dB
DIGITAL ATTENUATOR (each path, unless otherwise noted)							
Insertion Loss	IL				3.0		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$			53.1		dBm
Input Third-Order Intercept Point	IIP3	P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz			43.2		dBm
Attenuation Range					30.8		dB
Step Size					1		dB
Relative Attenuation Accuracy					0.11		dB
Absolute Attenuation Accuracy					0.23		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		-0.4		Degrees
			0dB to 24dB		0.6		
			0dB to 31dB		0.9		

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Amplitude Overshoot/ Undershoot		Between any two states	Elapsed time = 15ns		1.0		dB
			Elapsed time = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss	RL_{IN}	50Ω source			21.6		dB
Output Return Loss	RL_{OUT}	50Ω load			21.2		dB
SERIAL PERIPHERAL INTERFACE (SPI)							
Maximum Clock Speed	f_{CLK}				20		MHz
Data-to-Clock Setup Time	t_{CS}				2		ns
Data-to-Clock Hold Time	t_{CH}				2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}				3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}				7		ns
$\overline{CS}$ Setup Time	t_{EWS}				3.5		ns
Clock Pulse Width	t_{CW}				5		ns

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +3.3V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = +3.3V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G			20.9		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone		29.6		dBm
Noise Figure	NF			5.9		dB
Total Attenuation Range				30.8		dB
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.8		dB
		RF input 2 amplified power measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		49.1		
Output -1dB Compression Point	P_{1dB}	(Note 7)		13.4		dBm

Note 5: Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*.

Note 6: All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

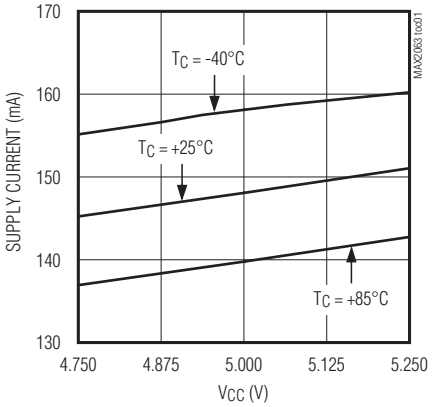
Note 7: It is advisable not to continuously operate RF input 1 or RF input 2 above +15dBm.

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

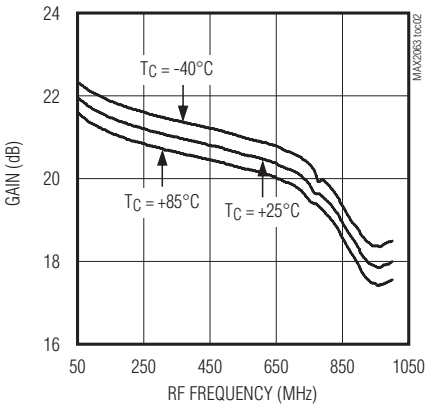
典型工作特性

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

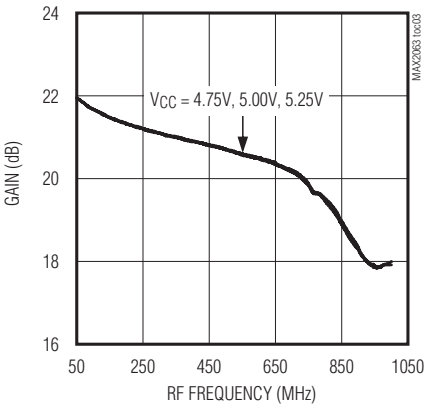
SUPPLY CURRENT vs. V_{CC}



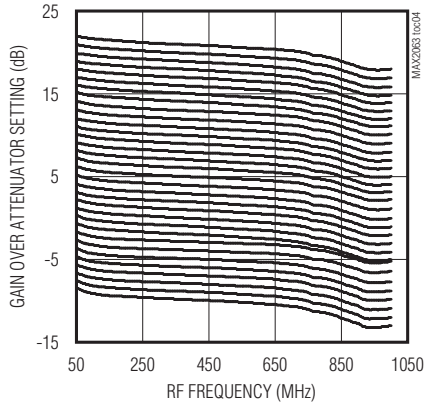
GAIN vs. RF FREQUENCY



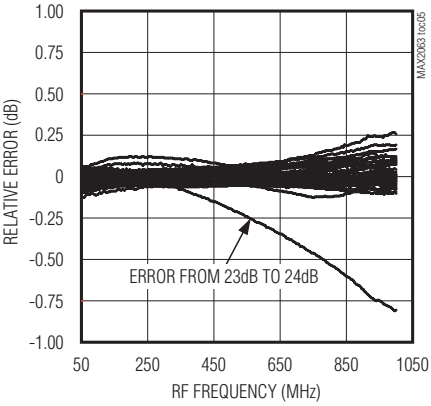
GAIN vs. RF FREQUENCY



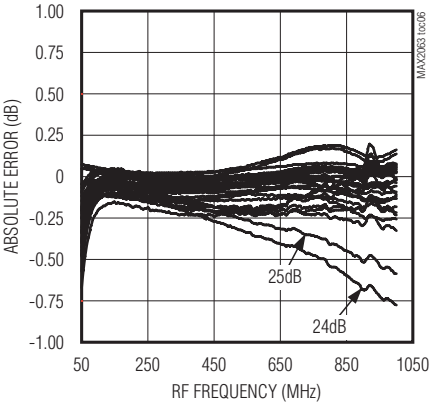
GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



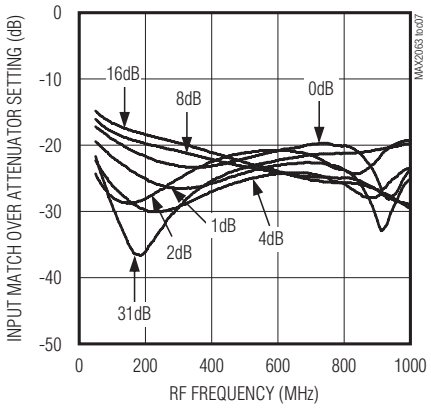
ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



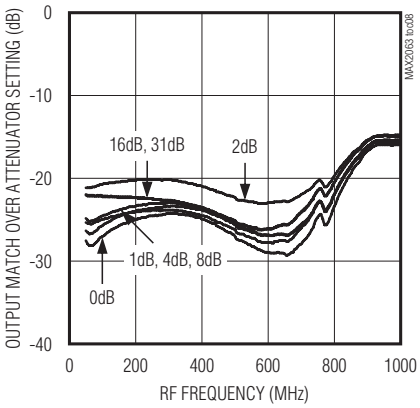
ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



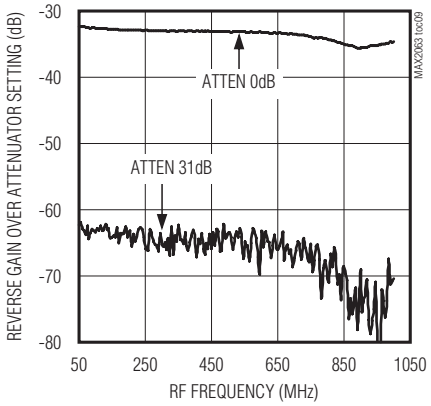
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



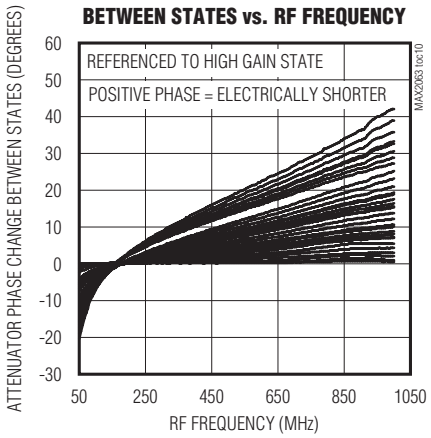
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

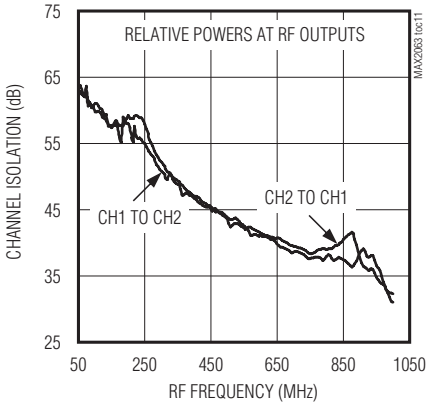
REVERSE GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



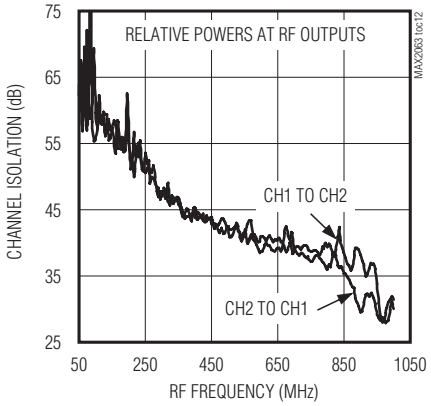
ATTENUATOR PHASE CHANGE BETWEEN STATES vs. RF FREQUENCY



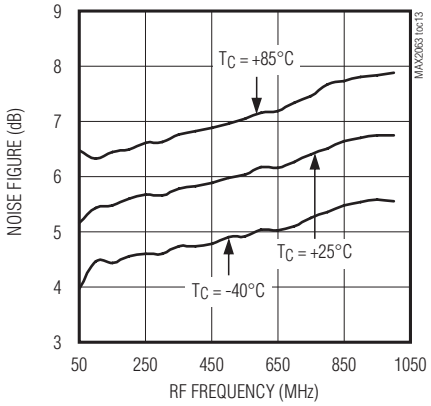
CHANNEL ISOLATION vs. RF FREQUENCY (MAXIMUM GAIN)



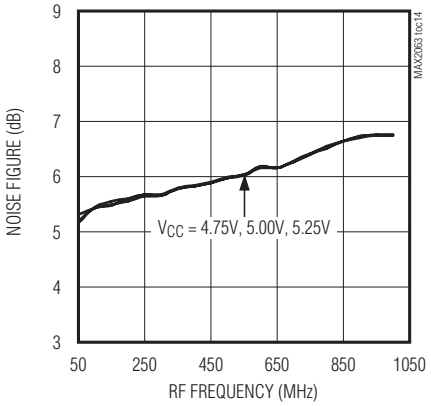
CHANNEL ISOLATION vs. RF FREQUENCY (MINIMUM GAIN)



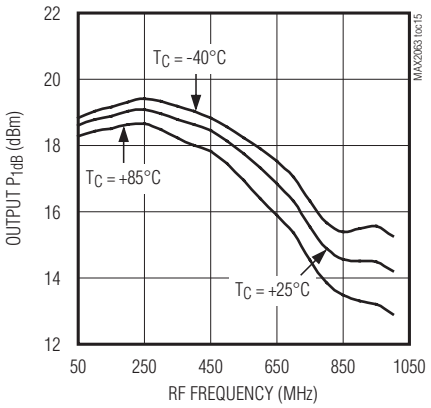
NOISE FIGURE vs. RF FREQUENCY



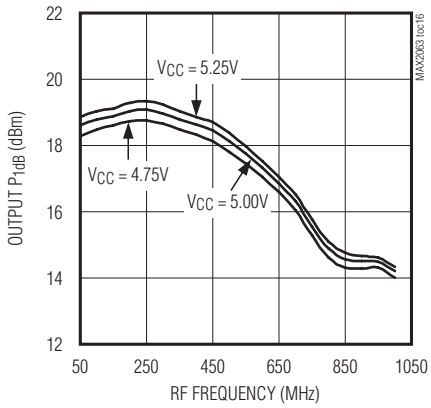
NOISE FIGURE vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY

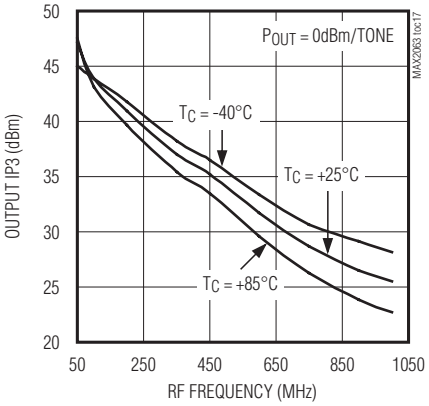


50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

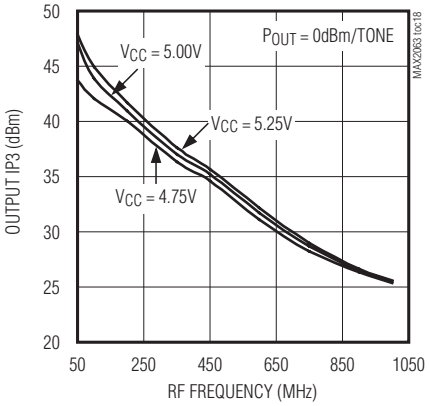
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

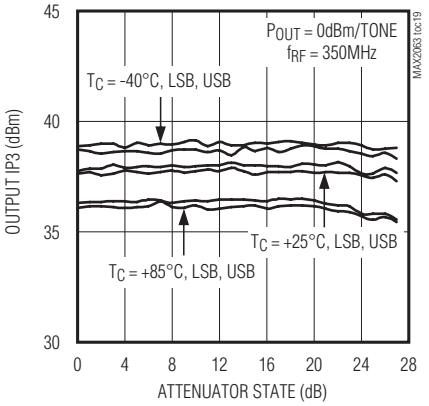
OUTPUT IP3 vs. RF FREQUENCY



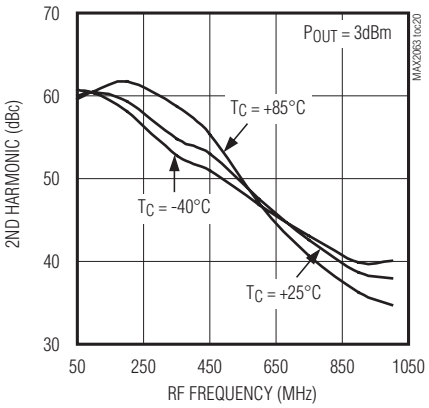
OUTPUT IP3 vs. RF FREQUENCY



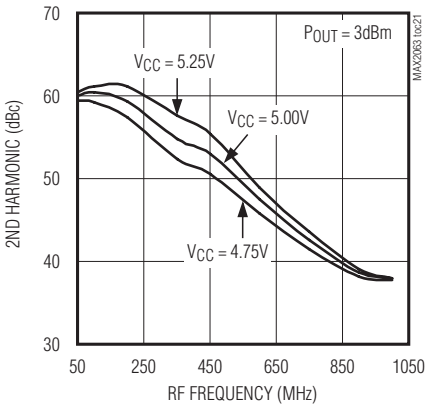
OUTPUT IP3 vs. ATTENUATOR STATE



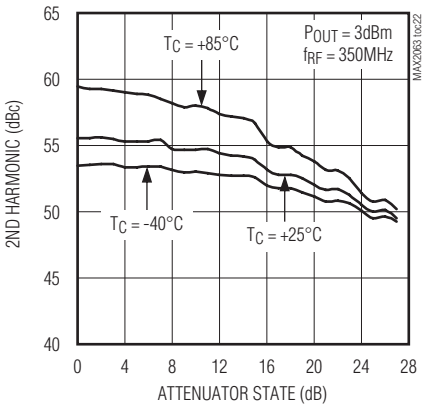
2ND HARMONIC vs. RF FREQUENCY



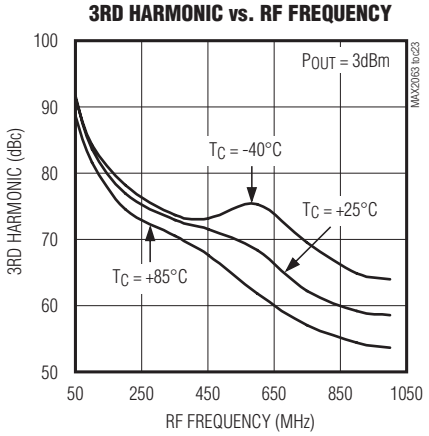
2ND HARMONIC vs. RF FREQUENCY



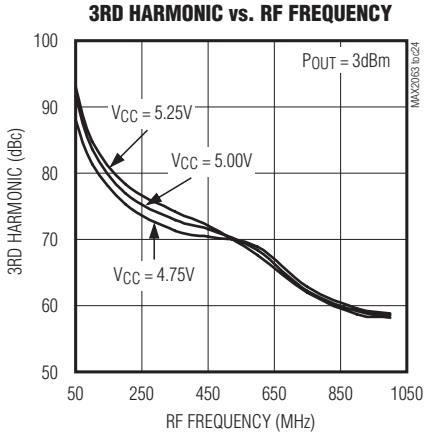
2ND HARMONIC vs. ATTENUATOR STATE



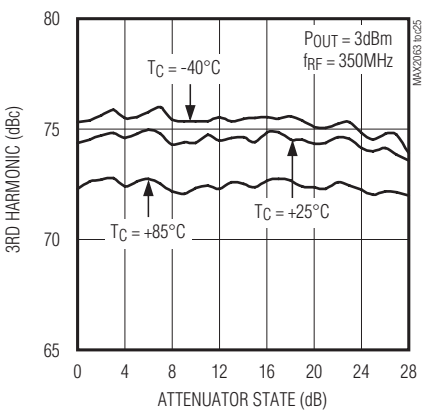
3RD HARMONIC vs. RF FREQUENCY



3RD HARMONIC vs. RF FREQUENCY



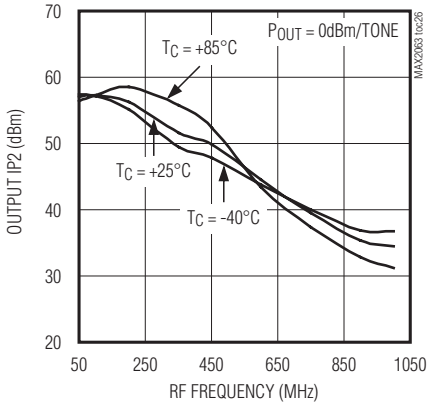
3RD HARMONIC vs. ATTENUATOR STATE



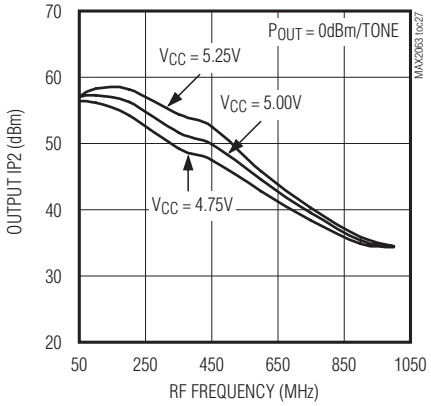
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

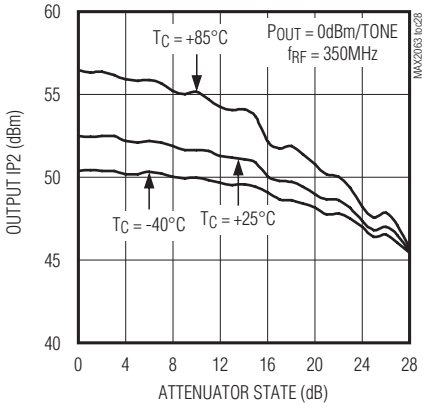
OUTPUT IP2 vs. RF FREQUENCY



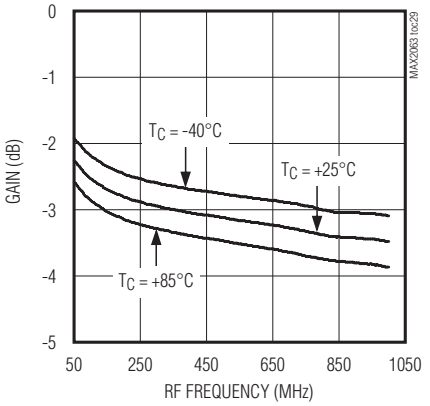
OUTPUT IP2 vs. RF FREQUENCY



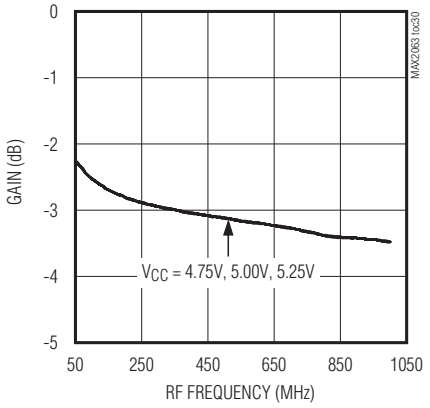
OUTPUT IP2 vs. ATTENUATOR STATE



GAIN vs. RF FREQUENCY (ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ATTENUATOR ONLY)

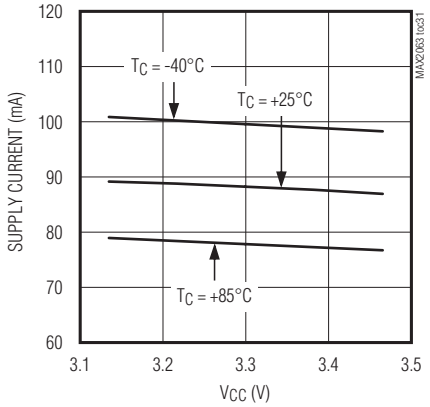


50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

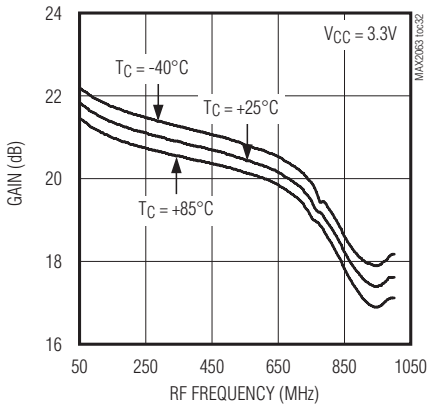
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

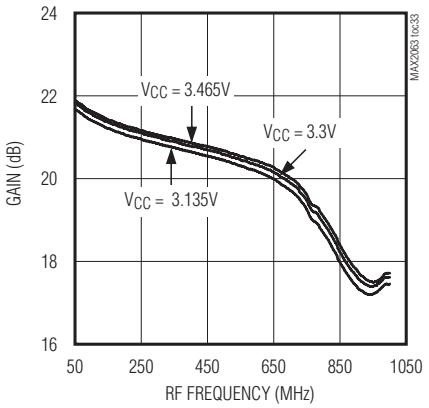
SUPPLY CURRENT vs. V_{CC}



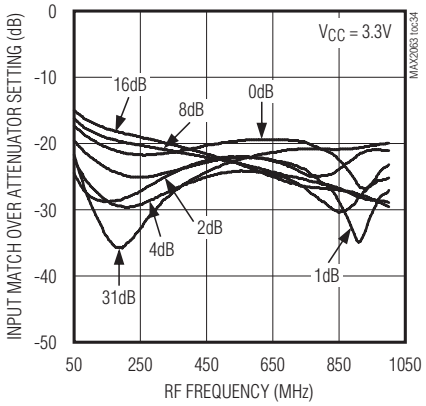
GAIN vs. RF FREQUENCY



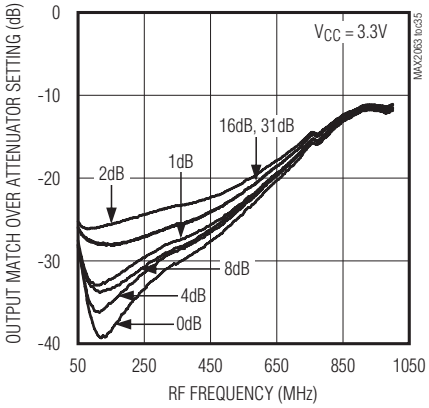
GAIN vs. RF FREQUENCY



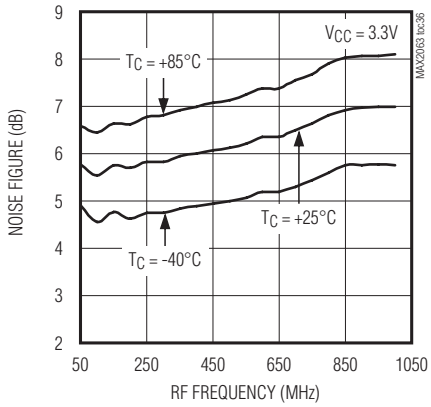
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



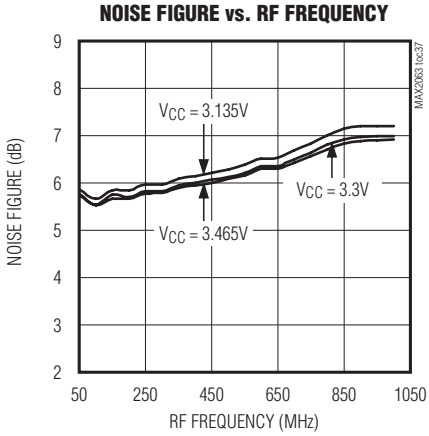
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



典型工作特性(续)

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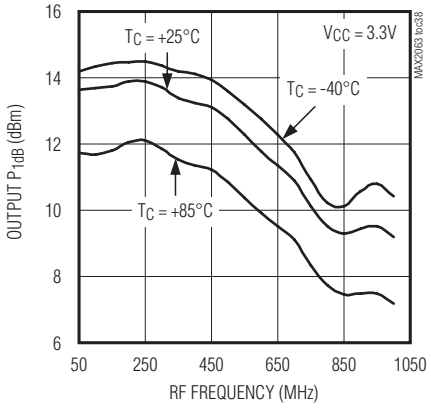
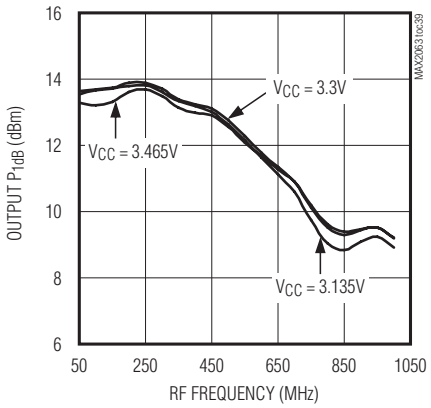
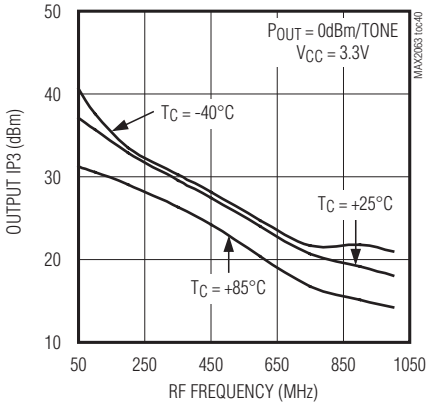
OUTPUT P_{1dB} vs. RF FREQUENCY



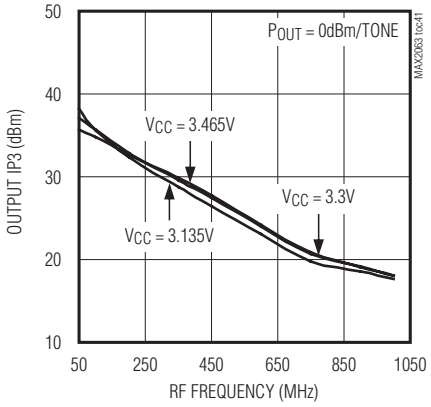
OUTPUT P_{1dB} vs. RF FREQUENCY



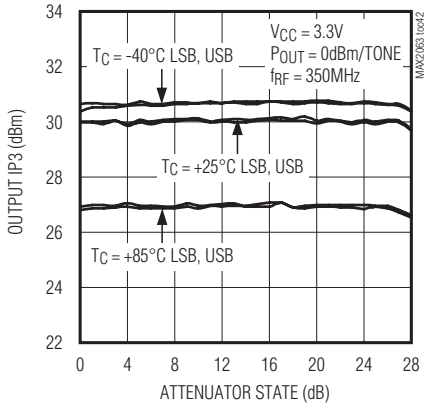
OUTPUT IP3 vs. RF FREQUENCY



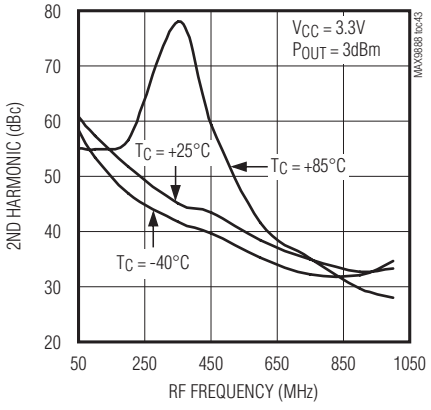
OUTPUT IP3 vs. RF FREQUENCY



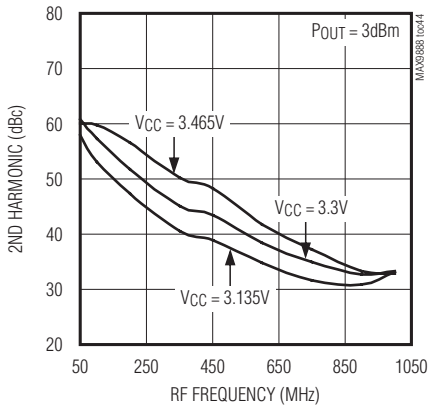
OUTPUT IP3 vs. ATTENUATOR STATE



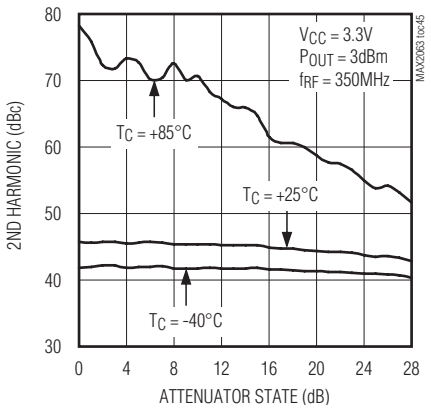
2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. ATTENUATOR STATE

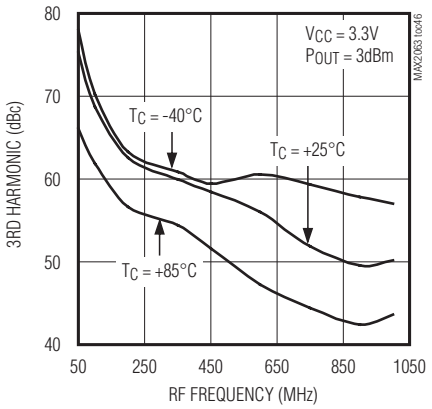


50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

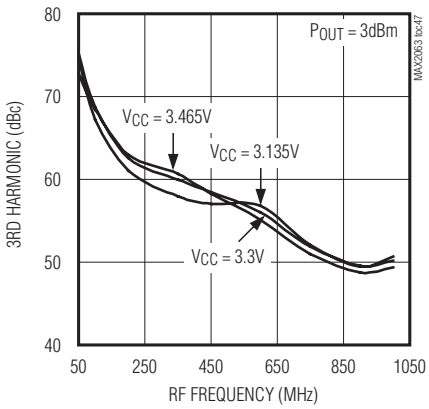
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

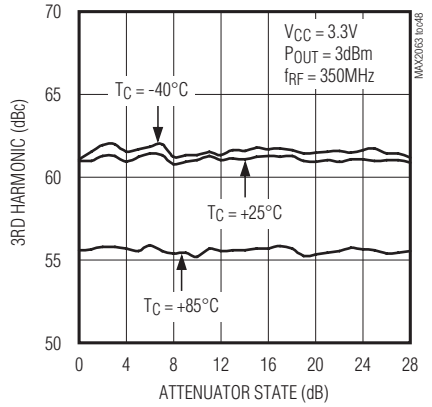
3RD HARMONIC vs. RF FREQUENCY



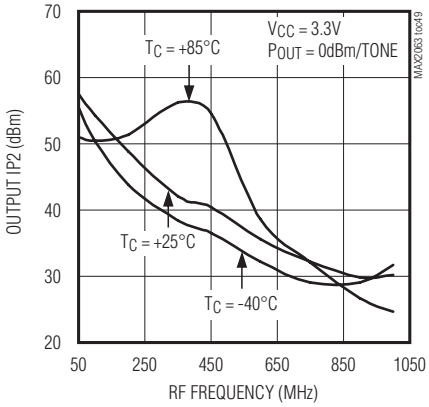
3RD HARMONIC vs. RF FREQUENCY



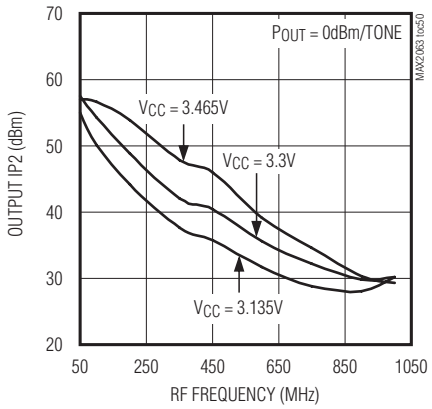
3RD HARMONIC vs. ATTENUATOR STATE



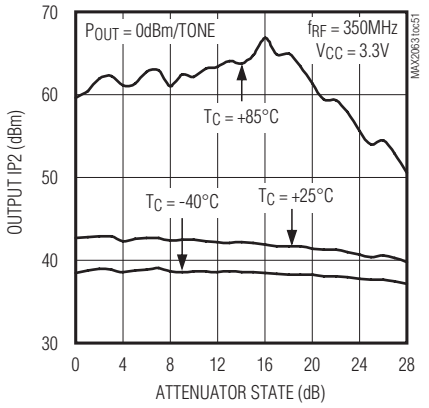
OUTPUT IP2 vs. RF FREQUENCY



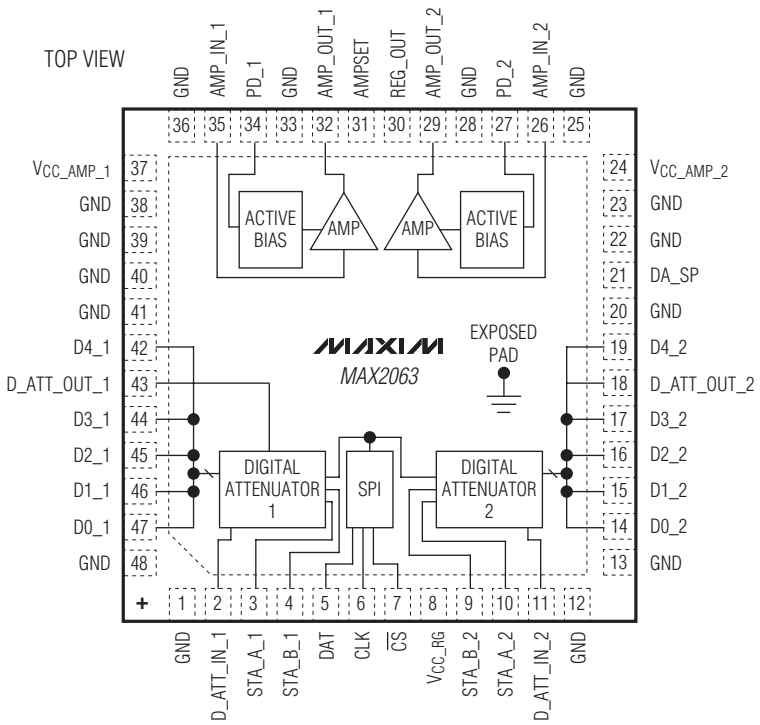
OUTPUT IP2 vs. RF FREQUENCY



OUTPUT IP2 vs. ATTENUATOR STATE



引脚配置



THIN QFN
(7mm x 7mm)

引脚说明

引脚	名称	功能
1, 12, 13, 20, 22, 23, 25, 28, 33, 36, 38–41, 48	GND	地。
2	D_ATT_IN_1	5位数字衰减器RF输入(50Ω)，通道1。需要外接隔直流电容。
3	STA_A_1	数字衰减器预编程衰减状态逻辑输入，通道1。 **状态A　状态B　数字衰减器1** 逻辑电平 = 0　逻辑电平 = 0　预编程状态1 逻辑电平 = 1　逻辑电平 = 0　预编程状态2 逻辑电平 = 0　逻辑电平 = 1　预编程状态3 逻辑电平 = 1　逻辑电平 = 1　预编程状态4
4	STA_B_1	
5	DAT	SPI数据输入。
6	CLK	SPI时钟输入。
7	$\overline{CS}$	SPI片选输入。

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

引脚说明(续)

引脚	名称	功能
8	V_{CC_RG}	稳压电源输入，连接到3.3V或5V外部电源。V_{CC_RG}为驱动放大器以外的所有电路供电，利用10nF电容旁路该引脚，电容应尽可能靠近该引脚放置。
9	STA_B_2	数字衰减器预编程衰减状态逻辑输入，通道2。 状态A / 状态B / 数字衰减器2 逻辑电平 = 0 / 逻辑电平 = 0 / 预编程状态1 逻辑电平 = 1 / 逻辑电平 = 0 / 预编程状态2 逻辑电平 = 0 / 逻辑电平 = 1 / 预编程状态3 逻辑电平 = 1 / 逻辑电平 = 1 / 预编程状态4
10	STA_A_2	
11	D_ATT_IN_2	5位数字衰减器RF输入(50Ω)，通道2。需要外接隔直流电容。
14	D0_2	1dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。
15	D1_2	2dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。
16	D2_2	4dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。
17	D3_2	8dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。
18	D_ATT_OUT_2	5位数字衰减器输出(50Ω)，通道2。需要外接隔直流电容，通过1000pF电容连接到AMP_IN_2。
19	D4_2	16dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。
21	DA_SP	数字衰减器串行/并行控制选择输入。将DA_SP设置为逻辑1，选择串行控制；将DA_SP设置为逻辑0，选择并行控制。
24	$V_{CC\_AMP\_2}$	驱动放大器电源输入，通道2。在尽可能靠近该引脚的位置安装10nF旁路电容。
26	AMP_IN_2	驱动放大器输入(50Ω) ，通道2。通过1000pF电容连接到D_ATT_OUT_2。
27	PD_2	关断控制，通道2。详细操作请参考表2。
29	AMP_OUT_2	驱动放大器输出(50Ω)，通道2。在AMP_OUT_2与$V_{CC_}$之间连接上拉电感。
30	REG_OUT	稳压器输出，通过1µF电容旁路。
31	AMPSET	3.3V供电时，驱动放大器的偏置设置。V_{CC_AMP1}和V_{CC_AMP2}采用3.3V供电时，该引脚置为逻辑1；5V供电时，置为逻辑0。
32	AMP_OUT_1	驱动放大器输出(50Ω)，通道1。在AMP_OUT_1与$V_{CC_}$之间连接上拉电感。
34	PD_1	关断控制，通道1。详细操作请参考表2。
35	AMP_IN_1	驱动放大器输入(50Ω) ，通道1。通过1000pF电容连接到D_ATT_OUT_1。
37	$V_{CC\_AMP\_1}$	驱动放大器电源输入，通道1。在尽可能靠近该引脚的位置安装10nF旁路电容。
42	D4_1	16dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。
43	D_ATT_OUT_1	5位数字衰减器输出(50Ω)，通道1。需要外接隔直流电容，通过1000pF电容连接到AMP_IN_1。
44	D3_1	8dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。
45	D2_1	4dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。
46	D1_1	2dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。
47	D0_1	1dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。
—	EP	裸焊盘，内部连接到GND。将其连接到大面积的PCB接地区域有利于改善RF性能，增强散热。

详细说明

MAX2063高线性度数字VGA是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω接口的应用而设计。器件的每个通道集成了一个数字衰减器，可提供31dB的增益控制，同时可优化放大器驱动设计来提供高增益、高输出IP3、低NF和低功耗指标。

可通过SPI兼容接口控制作为从机外设的每个数字衰减器；也允许以1dB步长通过5位并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择，可直接设置在4种增益选项的一种，用户可通过SPI接口预先设置四种增益选项。2个独立的控制引脚允许用户快速选择4种定制衰减状态的任何一个，无需对SPI总线重新编程。

因为每通道中两级放大电路的每一级都具有RF输入和RF输出，通过适当配置可以优化NF（放大器配置为第一级）或OIP3（放大器配置为最后一级）。该器件还提供增益为24dB的放大器（放大器本身），增益最大时NF为5.6dB（包括衰减器的插入损耗），并提供+41dBm的高OIP3。这些特性使得该器件成为多通道接收器和发射器应用理想的VGA选择。

5位数字衰减器控制

器件集成了两个5位数字衰减器，用于实现高动态范围控制。每个数字衰减器具有31dB控制范围、1dB步长，可通过专用的5位并行总线或3线SPI接口设置。请参考*应用信息*部分和表1所示的衰减器设置，获得更多信息。这些衰减器可用于静态和动态功率控制。

驱动放大器

器件包括两个24dB固定增益的高性能驱动器。每个驱动放大器优化于50MHz至1000MHz频率范围的高线性度指标。

表1. 控制逻辑

DA_SP	DIGITAL ATTENUATOR
0	Parallel controlled
1	SPI controlled (control voltages show up on the parallel control pins)

表2. 工作模式

RESULT	$V_{CC\_}$ (V)	AMPSET	PD_1	PD_2
All on	5	0	0	0
	3.3	1	0	0
AMP1 off AMP2 on	5	0	1	0
	3.3	1	1	0
AMP1 on AMP2 off	5	0	0	1
	3.3	1	0	1
All off	5	0	1	1
	3.3	1	1	1

应用信息

工作模式

器件可以工作在+3.3V电源电压，但会降低线性指标。AMPSET引脚需要在不同模式下进行适当偏置，如表2所示。此外，还可以独立控制驱动放大器关断，以降低直流电源的功耗，详细信息请参考表2所示的偏置配置。

SPI接口和衰减器设置

数字衰减器可采用5位字长通过3线SPI/MICROWIRE™兼容串行接口进行控制。移入56位数据，MSB在前，并通过$\overline{CS}$打包成帧。前28位数据用于设置第一路衰减器，后续28位数据用于设置第二路衰减器。当$\overline{CS}$为低电平时，时钟有效，数据在时钟的上升沿移入。当$\overline{CS}$跳变到高电平时，数据被锁存，改变衰减器设置（图1）。表3给出了SPI数据格式的详细信息。

MICROWIRE是National Semiconductor Corp.的商标。

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

第1路数字衰减器编程

D0:D7　保留位，置于逻辑0

D8:D12　预编程衰减状态1

D8 = 1dB位，D9 = 2dB位，D10 = 4dB位，D11 = 8dB位，D12 = 16dB位

D13:D17　预编程衰减状态2

D13 = 1dB位，D14 = 2dB位，D15 = 4dB位，D16 = 8dB位，D17 = 16dB位

D18:D22　预编程衰减状态3

D18 = 1dB位，D19 = 2dB位，D20 = 4dB位，D21 = 8dB位，D22 = 16dB位

D23:D27　预编程衰减状态4

D23 = 1dB位，D24 = 2dB位，D25 = 4dB位，D26 = 8dB位，D27 = 16dB位

第2路数字衰减器编程

D28:D35　保留位，置于逻辑0

D36:D40　预编程衰减状态1

D36 = 1dB位，D37 = 2dB位，D38 = 4dB位，D39 = 8dB位，D40 = 16dB位

D41:D45　预编程衰减状态2

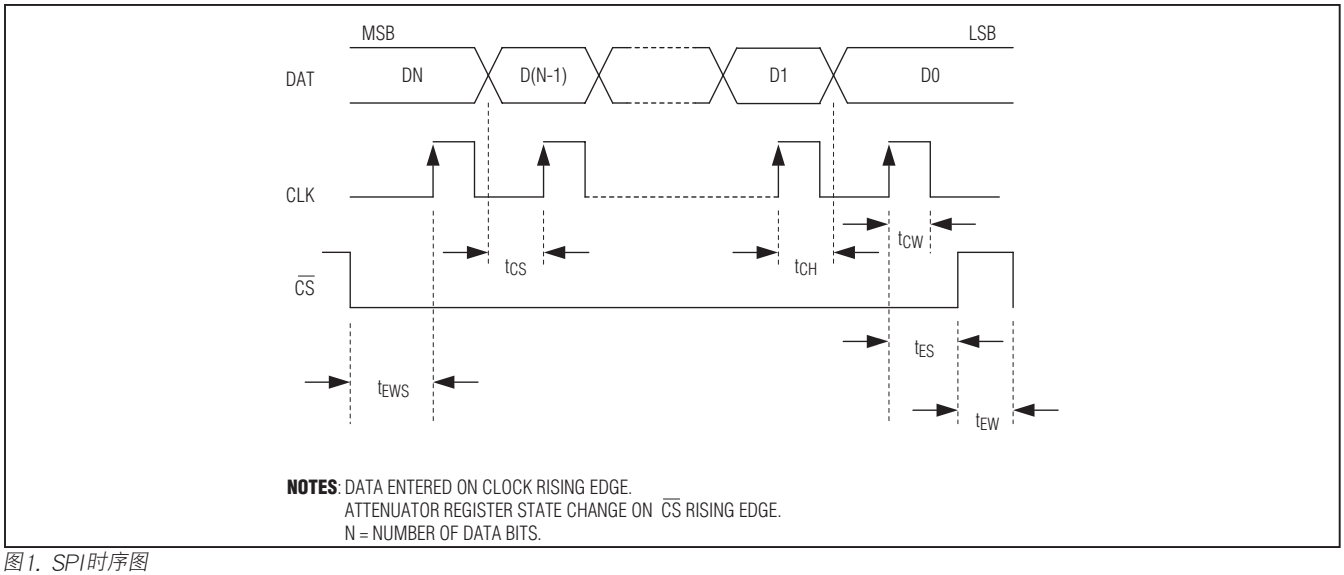
D41 = 1dB位，D42 = 2dB位，D43 = 4dB位，D44 = 8dB位，D45 = 16dB位

D46:D50　预编程衰减状态3

D46 = 1dB位，D47 = 2dB位，D48 = 4dB位，D49 = 8dB位，D50 = 16dB位

D51:D55　预编程衰减状态4

D51 = 1dB位，D52 = 2dB位，D53 = 4dB位，D54 = 8dB位，D55 = 16dB位



NOTES: DATA ENTERED ON CLOCK RISING EDGE.
ATTENUATOR REGISTER STATE CHANGE ON $\overline{CS}$ RISING EDGE.
N = NUMBER OF DATA BITS.

图1. SPI时序图

表3. SPI数据格式

FUNCTION	BIT	DESCRIPTION
2nd Digital Attenuator State 4	D55 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D54	8dB step
	D53	4dB step
	D52	2dB step
	D51	1dB step
2nd Digital Attenuator State 3	D50	16dB step (MSB of the 5-bit word used to program the digital attenuator state 3)
	D49	8dB step
	D48	4dB step
	D47	2dB step
	D46	1dB step
2nd Digital Attenuator State 2	D45	16dB step (MSB of the 5-bit word used to program the digital attenuator state 2)
	D44	8dB step
	D43	4dB step
	D42	2dB step
	D41	1dB step
2nd Digital Attenuator State 1	D40	16dB step (MSB of the 5-bit word used to program the digital attenuator state 1)
	D39	8dB step
	D38	4dB step
	D37	2dB step
	D36	1dB step
Reserved	D35	Bits D[35:28] are reserved. Set to logic 0.
	D34	
	D33	
	D32	
	D31	
	D30	
	D29	
	D28	
1st Digital Attenuator State 4	D27	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step
1st Digital Attenuator State 3	D22	16dB step (MSB of the 5-bit word used to program the digital attenuator state 3)
	D21	8dB step
	D20	4dB step
	D19	2dB step
	D18	1dB step
1st Digital Attenuator State 2	D17	16dB step (MSB of the 5-bit word used to program the digital attenuator state 2)
	D16	8dB step
	D15	4dB step
	D14	2dB step
	D13	1dB step

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

表3. SPI数据格式(续)

FUNCTION	BIT	DESCRIPTION
1st Digital Attenuator State 1	D12	16dB step (MSB of the 5-bit word used to program the digital attenuator state 1)
	D11	8dB step
	D10	4dB step
	D9	2dB step
	D8	1dB step
Reserved	D7	Bits D[7:0] are reserved. Set to logic 0.
	D6	
	D5	
	D4	
	D3	
	D2	
	D1	
	D0 (LSB)	

利用并行控制总线设置数字衰减器

为了达到25ns的快速切换能力，器件为每路衰减器提供一个辅助的5位并行控制接口。这两组数字逻辑衰减器控制引脚总线(D0_ _至D4_ _)用于设置衰减器的工作状态(表4)。

直接访问5位总线可以使用户省去SPI接口的编程延时。任何SPI总线的速率都受限于指令逐位传递到外围器件的时间。通过直接访问5位并行接口，用户可以在“快速建立”自动增益控制(AGC)应用中实现数字衰减状态的迅速切换。

注意，当数字衰减器由SPI总线控制时，每个数字衰减器的控制电压由五个并行控制引脚设置(引脚14-17和引脚19控制数字衰减器2，引脚42和引脚44-47控制数字衰减器1)。当数字衰减器处于SPI控制模式时，并行控制引脚必须开路。

“速射”预编程衰减状态

器件能够在4个预置衰减等级之间提供“速射”增益选择。与上述辅助5位总线类似，“速射”增益选择使用户能够快速进入4个预先设定的数字衰减状态的任意一个，消除了通过SPI总线重新编程的相关延时。

这种方式的切换速度与采用辅助5位并行总线的速度相当。但这一特殊功能可以使数字衰减器的I/O降低5倍或2.5倍(5个控制位与1个或2个控制位)，具体取决于所要求的状态数。

用户可通过STA_A_1和STA_B_1 (衰减器2对应于STA_A_2和STA_B_2)逻辑输入引脚设置所要求的各级状态(参考表5和表6)。利用STA_A_1引脚(1个控制位)可以得到2个预先设定的衰减状态，同时使用STA_A_1和STA_B_1引脚(2个控制位)，可以得到4个预先设定的衰减状态。

例如，假设AGC应用需要静态调节衰减器，以解决接收器增益不一致的问题。该AGC电路还需要对可能引起接收器灵敏度下降以及ADC过驱动的干扰信号进行动态衰减。该实例中，器件可以预先设置(通过SPI总线) 2种衰减状态：一个状态用于处理静态增益调节，另一个状态用于处理干扰信号。

用户只需要对一个I/O引脚(即STA_A_1控制位)进行控制，即可在静态和动态衰减控制之间快速切换。

需要时，用户还可以使用第二个I/O引脚(即STA_B_1控制位)设置另外两个衰减状态。这两个附加的衰减设置非常适合软件定义的无线通信装置，这些装置往往需要多个静态增益设置，以满足不同工作频率的要求；也适合需要多个动态衰减设置以处理不同阻塞电平(按照多个无线通信标准的定义)的应用。

供电顺序

所采用的供电顺序为:

1) 电源上电

2) 施加控制信号

布局考虑

器件经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。器件采用48引脚薄型QFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装器件的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP**必须**直接或通过一系列电镀过孔焊接到PCB的地层。

表7给出了典型应用电路的元件值。

表4. 数字衰减器设置(并行控制，DA_SP = 0)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0_ _	Disable 1dB attenuator	Enable 1dB attenuator
D1_ _	Disable 2dB attenuator	Enable 2dB attenuator
D2_ _	Disable 4dB attenuator	Enable 4dB attenuator
D3_ _	Disable 8dB attenuator	Enable 8dB attenuator
D4_ _	Disable 16dB attenuator	Enable 16dB attenuator

表5. 衰减器1的可编程衰减状态设置(DA_SP = 1)

STA_A_1	STA_B_1	SETTING FOR DIGITAL ATTENUATOR 1*
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

**由SPI编程位D8:D27定义(详细信息请参考表3)。*

表6. 衰减器2的可编程衰减状态设置(DA_SP = 1)

STA_A_2	STA_B_2	SETTING FOR DIGITAL ATTENUATOR 2*
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

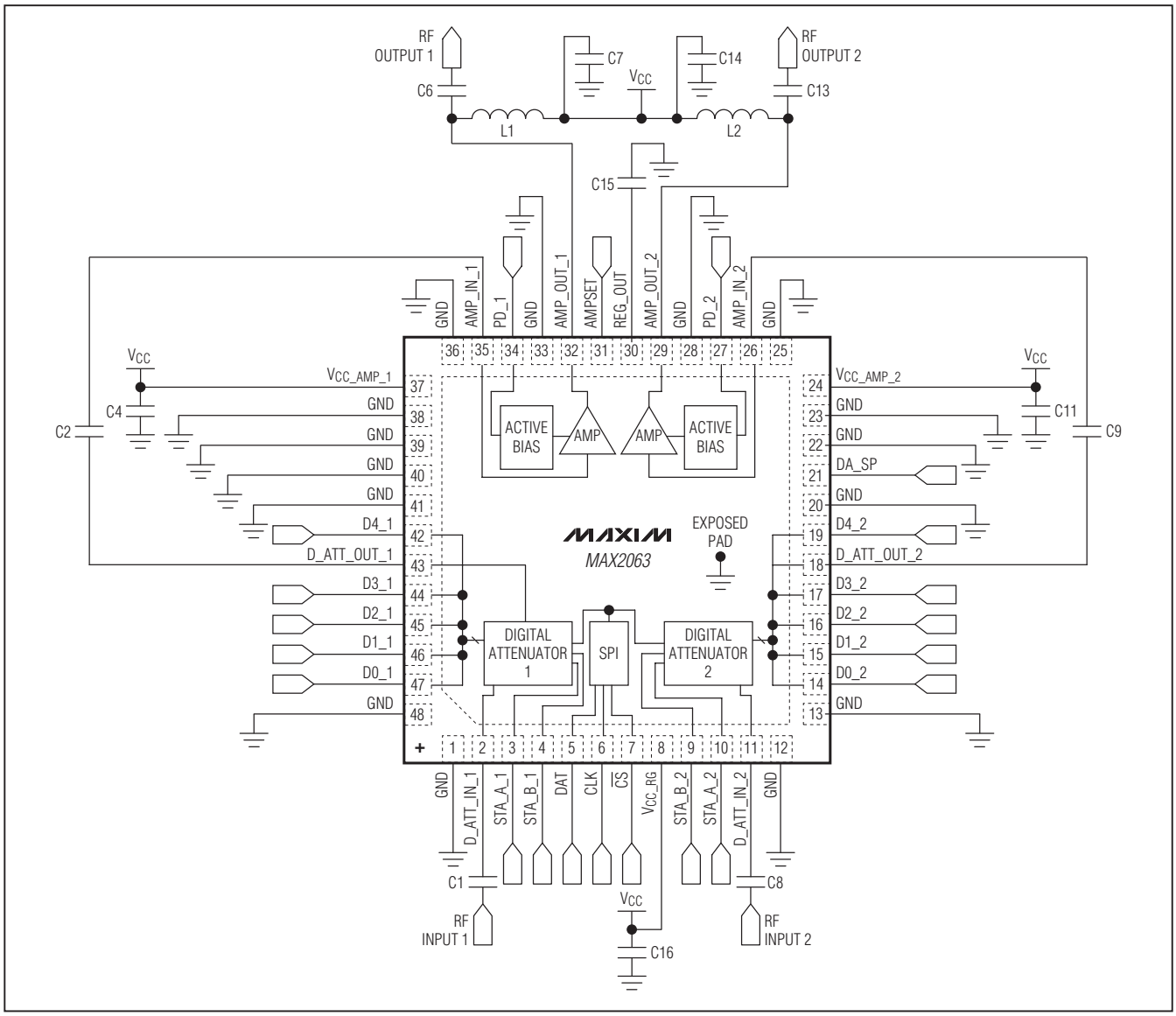
**由SPI编程位D36:D55定义(详细信息请参考表3)。*

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

表7. 典型应用电路的元件值

DESIGNATION	QTY	DECRIPTION	COMPONENT SUPPLIER
C1, C2, C6, C8, C9, C13	6	1000pF capacitors (0402) Murata GRM1555C1H102J	Murata North America Electronics, Inc.
C4, C7, C11, C14, C16	5	10nF capacitors (0402) Murata GRM155R71E103K	Murata North America Electronics, Inc.
C15	1	1µF capacitor (0603) Murata GRM188R71C105K	Murata North America Electronics, Inc.
L1, L2	2	820nH inductors (1008) Coilcraft 1008CS-821XJLC	Coilcraft, Inc.
U1	1	VGA (48-pin thin QFN-EP, 7mm x 7mm) Maxim MAX2063ETM+	Maxim Integrated Products, Inc.

典型应用电路



芯片信息

PROCESS: SiGe BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
48引脚薄型QFN-EP	T4877+7	21-0144	90-0133

50MHz至1000MHz、高线性度、串行/并行控制的双通道数字VGA

修订历史

修订号	修订日期	说明	修改页
0	6/10	最初版本。	—

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