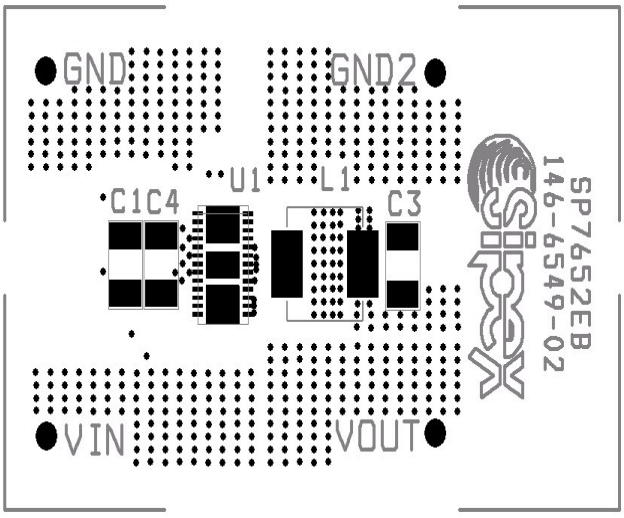
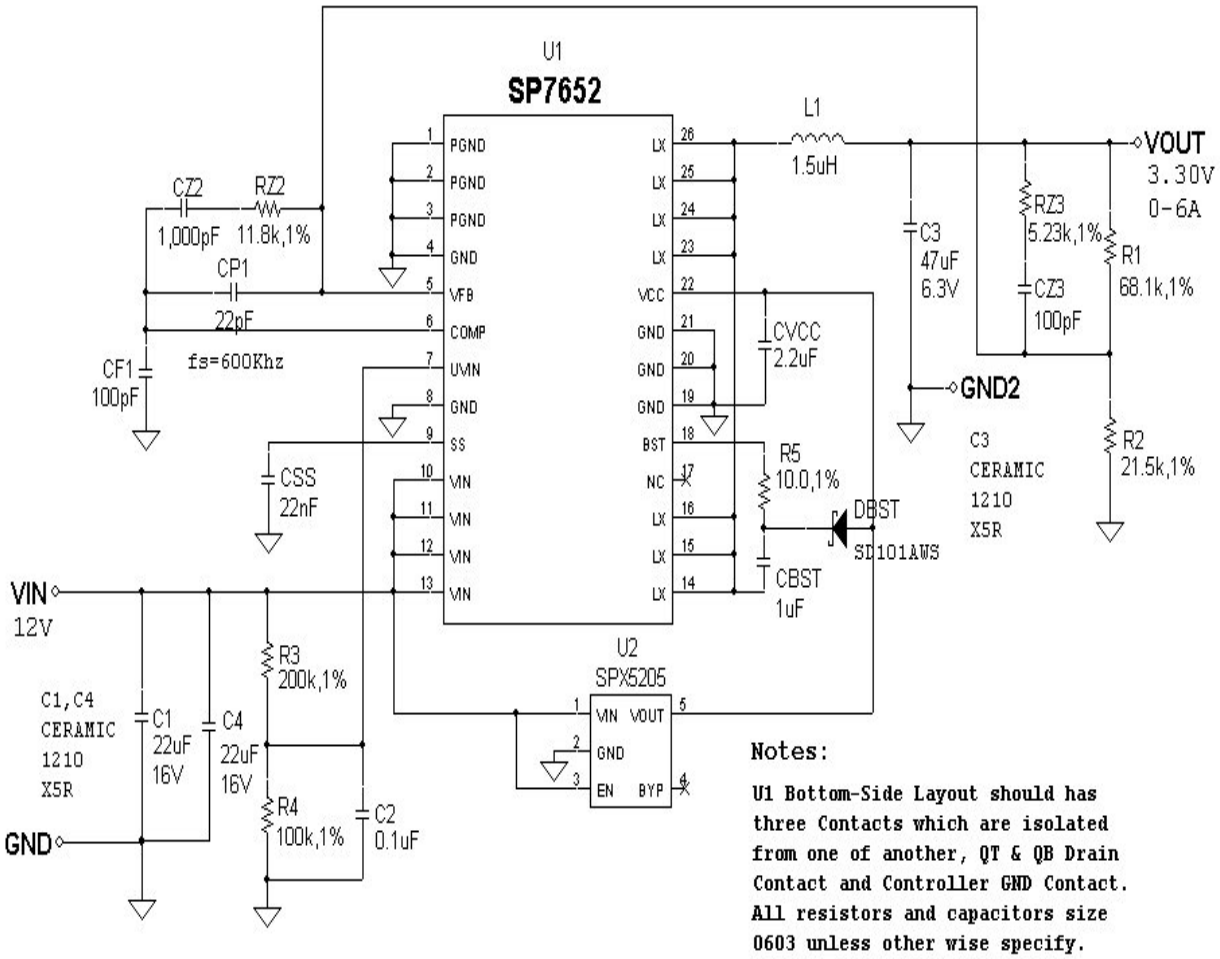
SP7652
Evaluation Board Manual

- Easy Evaluation for the SP7652ER 0 to 28V Input, 0 to 6A Output Synchronous Buck Converter
- Built in Low Rds(on) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 90%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown



SP7652EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP7652EB Circuit

Connect the SP7652 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It’s best to GND reference scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen touching probe tip to the pad for C3 and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7652 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7652 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V \left(R1 / R2 + 1 \right) \Rightarrow R2 = R1 / \left[\left(Vout / 0.80V \right) - 1 \right]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP7652 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7652ER provides short circuit protection by sensing Vout at GND.

POWER SUPPLY DATA

The SP7652ER is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7652 Evaluation Board Efficiency plot, with efficiencies to 90% and output currents to 6A. SP7652ER Load Regulation is shown in Figure 2 of only 0.3% change in output voltage from no load to 6A load. Figures 3 and 4 illustrate a 3A to 6A and 0A to 6A Load Step. Start-up Response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP7652ER is configured for hiccup mode in response to an output dead short circuit condition and will Softstart until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 30mV at no load to 6A load.

While data on individual power supply boards may vary, the capability of the SP7652ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

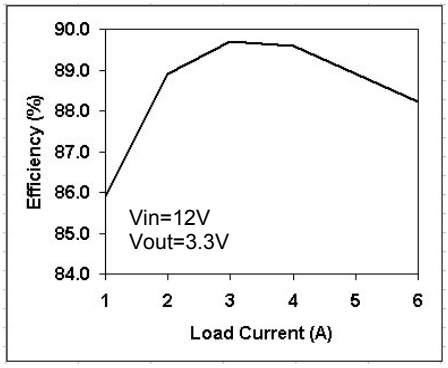


Figure 1. Efficiency vs Load

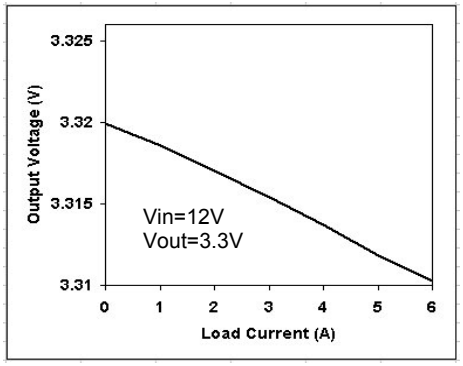


Figure 2. Load Regulation

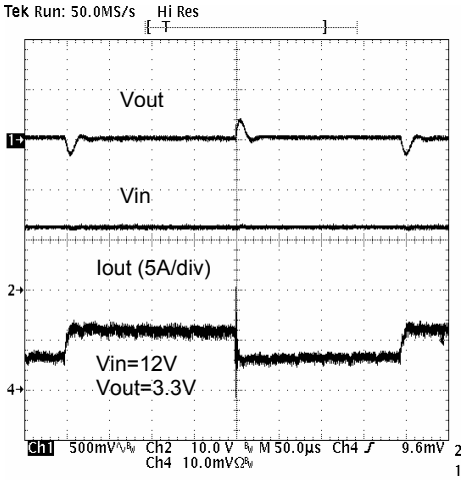


Figure 3. Load Step Response: 3->6A

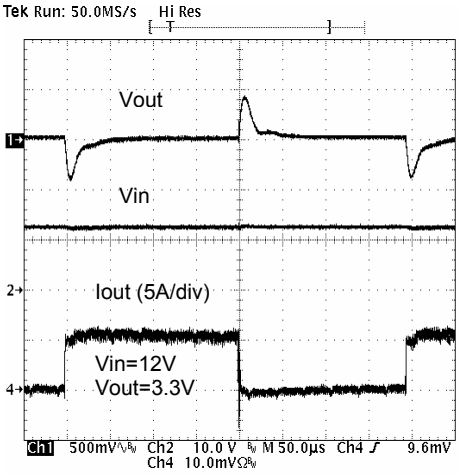


Figure 4. Load Step Response: 0->6A

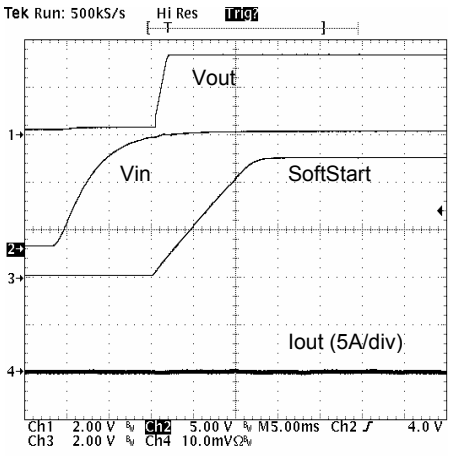


Figure 5. Start-Up Response: No Load

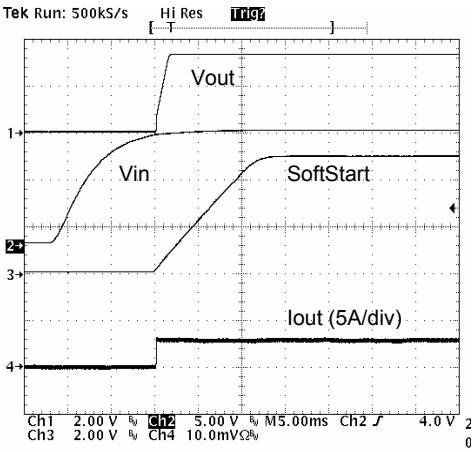


Figure 6. Start-Up Response: 3A Load

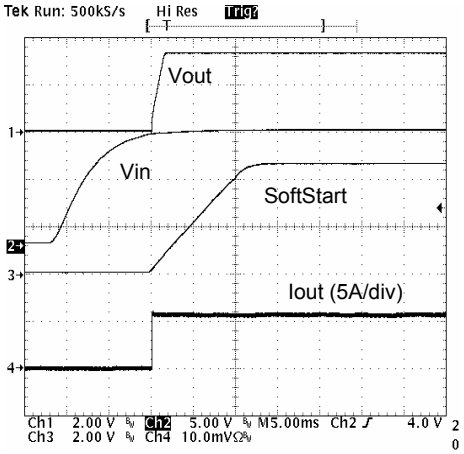


Figure 7. Start-Up Response: 6A Load

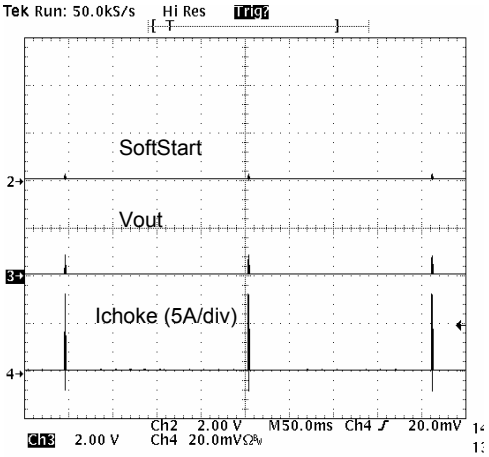
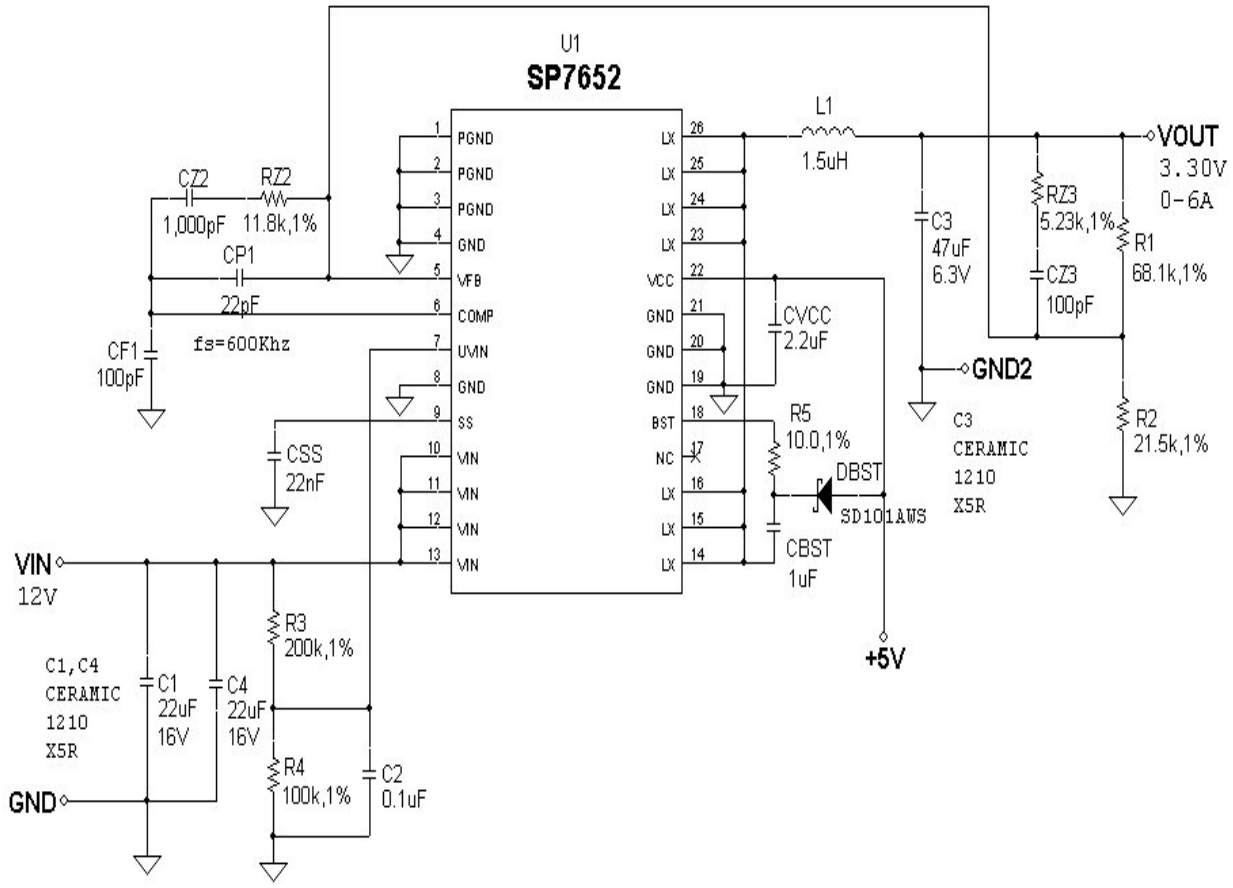


Figure 8. Output Load Short Circuit

+5V BIAS SUPPLY APPLICATION SCHEMATIC

In this application example, the SP7652ER is power by an external +5V bias supply which current consumption of 20mA Maximum. If this supply is not available than it is recommend Sipex SPX5205 Low-Noise LDO Voltage Regulator which is included on the SP7652 Evaluation Board.



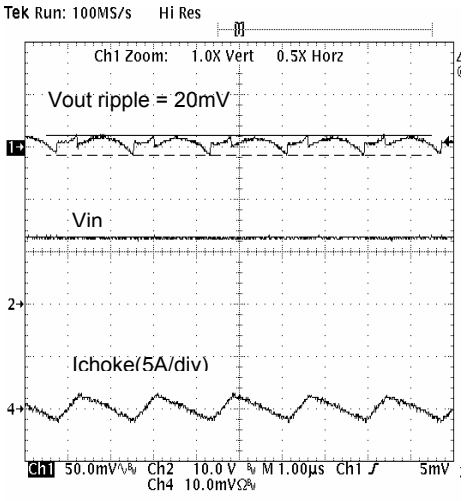


Figure 9. Output Ripple: No Load

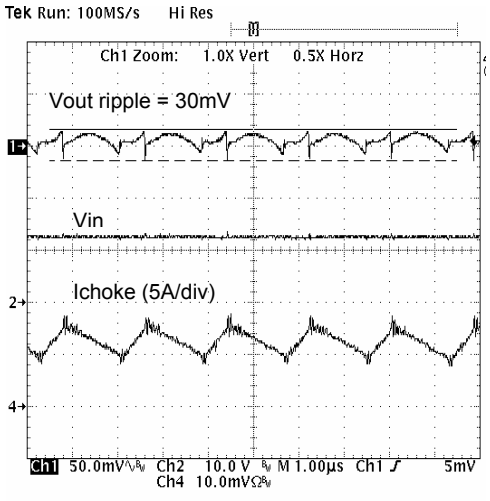


Figure 10. Output Ripple: 6A Load

DIFFERENT +5V BIAS SUPPLY SCHEMES APPLICATION SCHEMATIC

The SP7652ER VCC Bias Supply can be derived from Vin or external bias with several biasing options. The transistor plus zener diode +5V bias supply could also be used as shown in Figure 11.

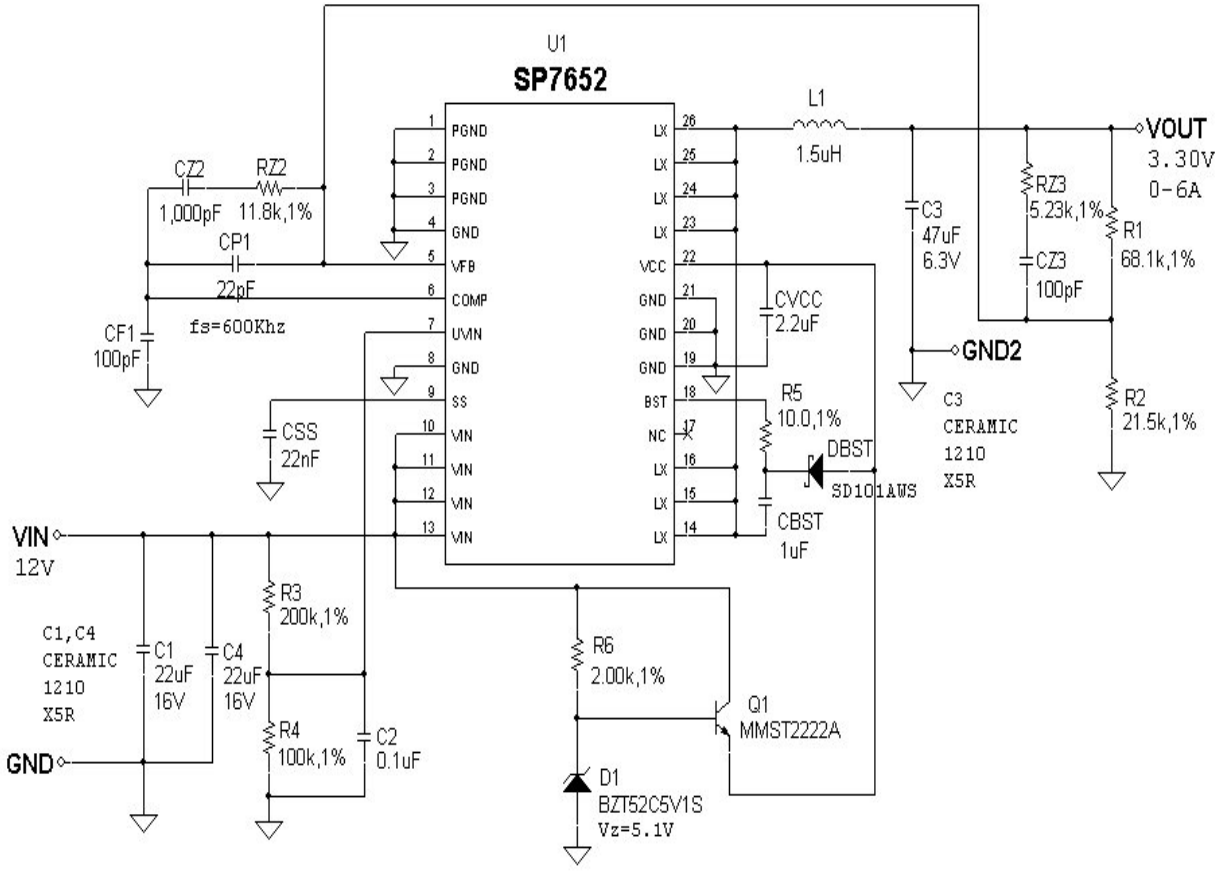


Figure 11. Transistor plus Zener Diode +5V Supply Application Schematic

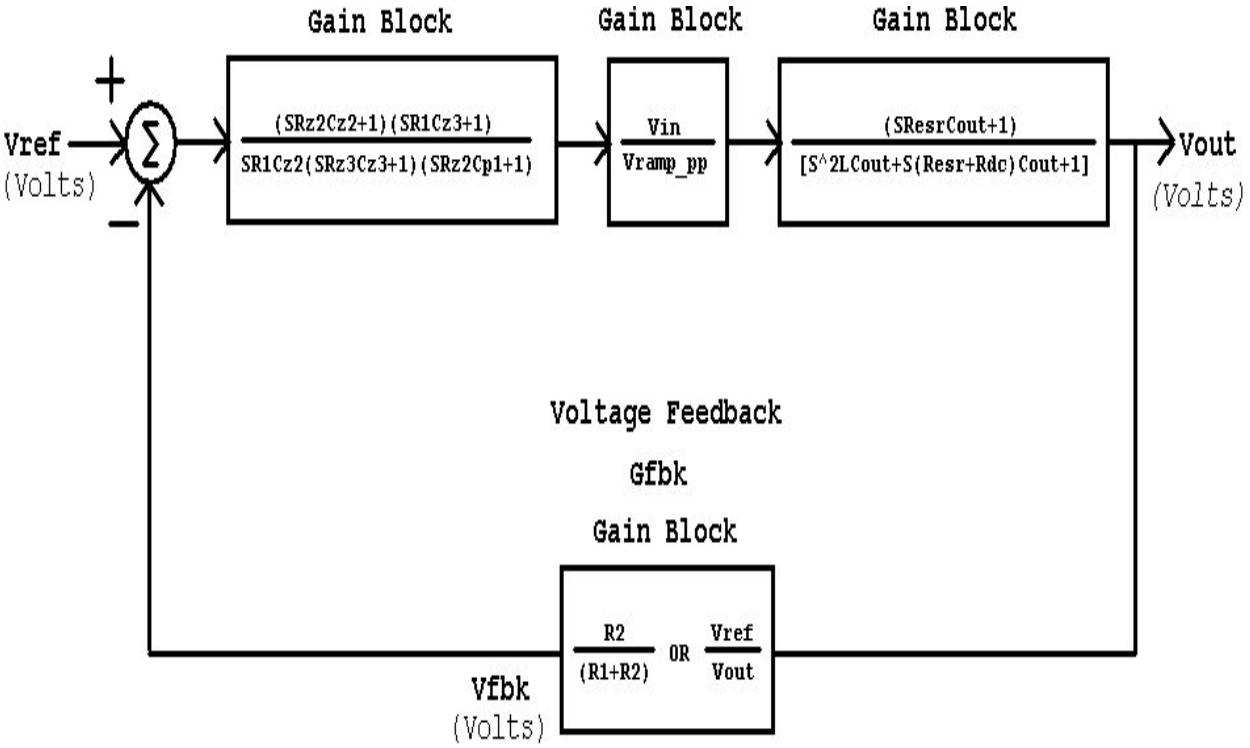
Table 1: SP7652EB Suggested Components and Vendor Lists

INDUCTORS - SURFACE MOUNT							
Inductance (uH)	Manufacturer/Part No.	Inductor Specification					Manufacturer Website
		Series R mOhms	Isat (A)	Size LxW(mm)	Size Ht.(mm)	Inductor Type	
1.5	**Vishay IHLP-2525CZ-01-1R5MTR**	**14**	**18**	**6.86x6.47**	**3.0**	**Shielded Ferrite Core**	www.vishay.com
1.5	Inter-Technical SC7232-1R5M	8.8	14	6.8x6.8	4.5	Shielded Ferrite Core	www.inter-technical.com
1.5	Coilcraft DO3316P-152	9.0	8.0	12.95x9.40	5.5	Non-Shielded Ferrite Core	www.coilcraft.com
CAPACITORS - SURFACE MOUNT							
Capacitance (uF)	Manufacturer/Part No.	Capacitor Specification					Manufacturer Website
		ESR mOhms (max)	Ripple Current (A) @ 45C	Size LxW(mm)	Size Ht.(mm)	Voltage (V)	Capacitor Type
22	**TDK C3225X5R1C226M**	**2.0**	**4.0**	**3.2x2.5**	**2.0**	**16.0**	**X5R Ceramic**	www.tdk.com
47	**TDK C3225X5R0J476M**	**2.0**	**4.0**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic**	www.tdk.com

Note: Components highlighted in **bold** are those used on the SP7652 Evaluation Board.

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7652EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7652EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7652 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 12. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows.

a. Choose **fco** = fs / 10

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2 / R1** gain for the desired gain bandwidth
Rz2 = R1 (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP7652ER internal Error Amplify

As a particular example, consider for the following SP7652EB with a **Type III** Voltage Loop Compensation component selections:

Vin = 5 to 15V
Vout = 3.30V @ 0 to 6A load
Select **L = 1.5uH** => yield ≈ 48% of maximum 6A output current ripple.
Select **Cout = 47uF Ceramic** capacitor (Resr ≈ **2mΩ**)
fs = 600khz SP7652 internal Oscillator Frequency
Vramp_pp = 1.0V SP7652 internal Ramp Peak to Peak Amplitude

<u>Step by step design procedures</u>:

a. **fco** = 600khz / 10 = 60khz

b. **fp_LC** = 1 / 2π [(1.5uH)(47uF)]^1/2 ≈ 20khz

c. **fz_ESR** = 1 / 2π (2mΩ)(47uF) ≈ 1.7Mhz

d. **R1** = 68.1kΩ, 1%

e. **R2** = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz2** = 68.1kΩ (1.0V / 15V) (60khz / 20khz) ≈ 11.8kΩ, 1%

g. **Cz2** = 1 / π (11.8kΩ) (20khz) ≈ 1,000pF, X7R

h. **Cp1** = 1 / 2π (11.8kΩ) (1.7Mhz) ≈ 10pF => Select **Cp1** = 22pF for noise filtering

i. **Rz3** = 2 (68.1kΩ) (20khz) / 600khz ≈ 5.23kΩ, 1%

j. **Cz3** = 1 / π (5.23kΩ) (600khz) ≅ 100pF, COG

k. **Cf1** = 100pF to stabilize SP7652ER internal Error Amplify

+5V INPUT WITH A TYPE III COMPENSATION APPLICATION SCHEMATIC

Figure 13 shows another example of SP7652ER configures for +5V input by simply changing a few external resistors and capacitors components value for delivering a 0-6A output with excellent line and load regulation.

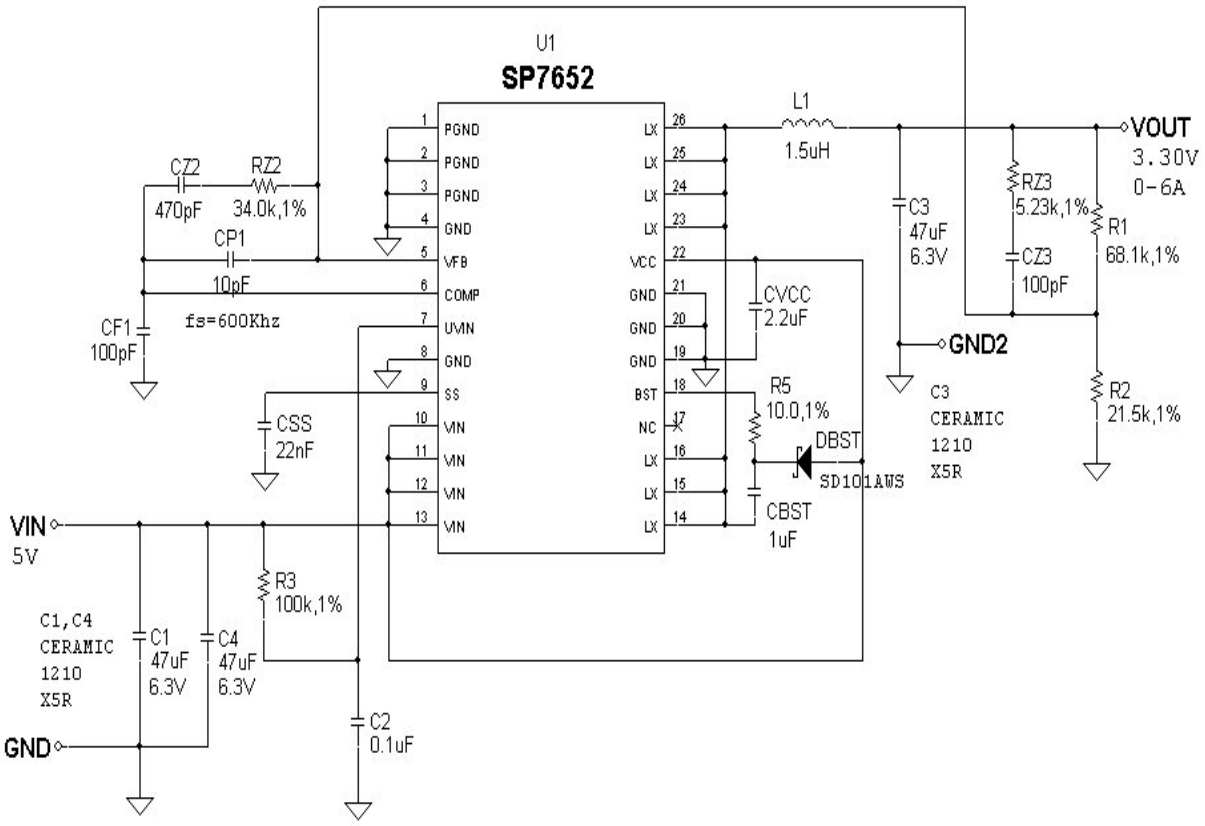


Figure 13. SP7652ER Configures for Vin = 5V, Vout = 3.3V at 0-6A Output Load Current

TYPE II LOOP COMPENSATION DESIGN

Type II compensation is specifically used when an Electrolytic or Tantalum output capacitor is chosen at the converter output due to its low cost. In that case, the zero caused by the output capacitor ESR is within a few khz and this is of course greatly simplifying the voltage loop compensation design. By adding an additional zero in the compensation loop before the first pole, the voltage loop bandwidth is extended with a 90º phase boost and hence the overall transient response time is improved. Most previous guidelines for calculating the component values for Type III compensation can be carries over for Type II except for the new **Rz**, **Cz** and **Cp** components. Note that Rz2, Cz2, Cp1, Rz3, and Cz3 components are not required for the Type II Loop Compensation Design.

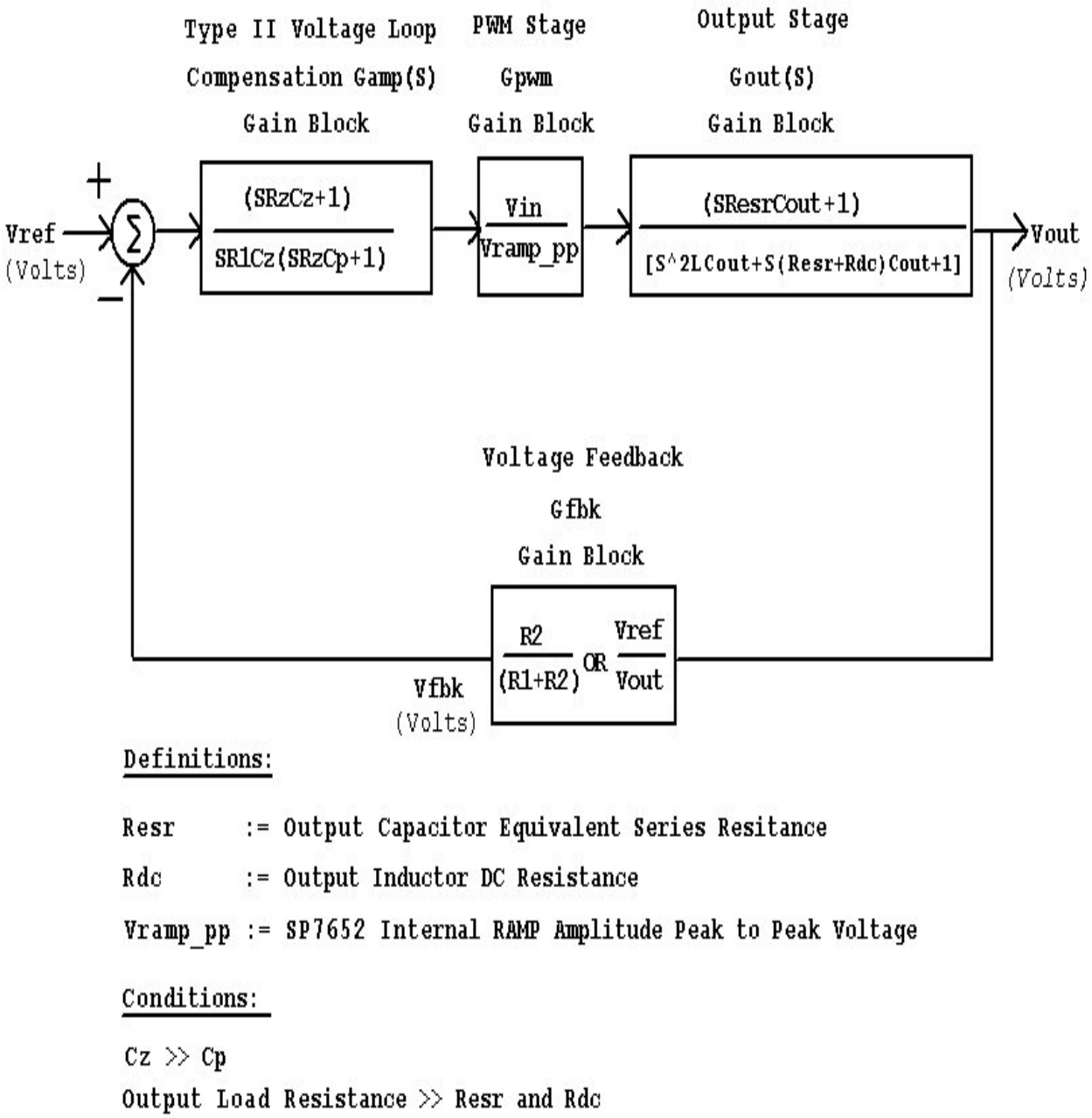


Figure 14. Voltage Mode Control Loop with Loop Dynamic for Type II Compensation

f. Select the ratio of **Rz / R1** gain for the desired gain bandwidth
Rz = R1 (Vramp_pp / Vin_max) (fco) [fz_ESR / (fp_LC) ^ 2]

g. Calculate **Cz** by placing the zero at 1/10 of the output filter pole frequency
Cz = 1 / 0.1(2π) (Rz) (fp_LC)

h. Calculate **Cp** by placing the second pole at ½ of the switching frequency
Cp = 1 / π (Rz) (fs)

As a particular example, consider for the following SP7652EB with a **Type II** Voltage Loop Compensation component selections:

Vin = 5 to 15V
Vout = 3.30V @ 0 to 6A load
Select **L = 1.5uH** => yield ≈ 48% of maximum 6A output current ripple.
Select **Cout = 330uF Tantalum** capacitor (Resr ≈ **10mΩ**)
fs = 600khz SP7652 internal Oscillator Frequency
Vramp_pp = 1.0V SP7652 internal Ramp Peak to Peak Amplitude

Step by step design procedures:

a. fco = 600khz / 10 = 60khz

b. fp_LC = 1 / 2π [(1.5uH) (330uF)] ^ 1/2 ≈ 7khz

c. fz_ESR = 1 / 2π (10mΩ) (330uF) ≈ 50khz

d. R1 = 68.1kΩ, 1%

e. R2 = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz** = 68.1kΩ (1.0V / 15V) (60khz) [50khz / (7khz) ^ 2] ≈ 280kΩ, 1%

g. **Cz** = 1 / 0.1 (2π) (280kΩ) (7khz) ≈ 820pF, COG

h. **Cp** = 1 / π (280kΩ) (600khz) ≈ 2.2pF => Select **Cp1** = 10pF for noise filtering

l. Cf1 = 100pF to stabilize SP7652ER internal Error Amplify

+5V OUTPUT WITH A TYPE II COMPENSATION APPLICATION SCHEMATIC

SP7652ER with Tantalum output capacitor configures for Vin = 12V, Vout = +5V at 0-6A output current. Figure 16 and 17 show output voltage ripple less than 60mV at no load to 6A load. Figure 18 and 19 show typical 92% efficiency and 0.3% load regulation plots with a Type II compensation application circuits.

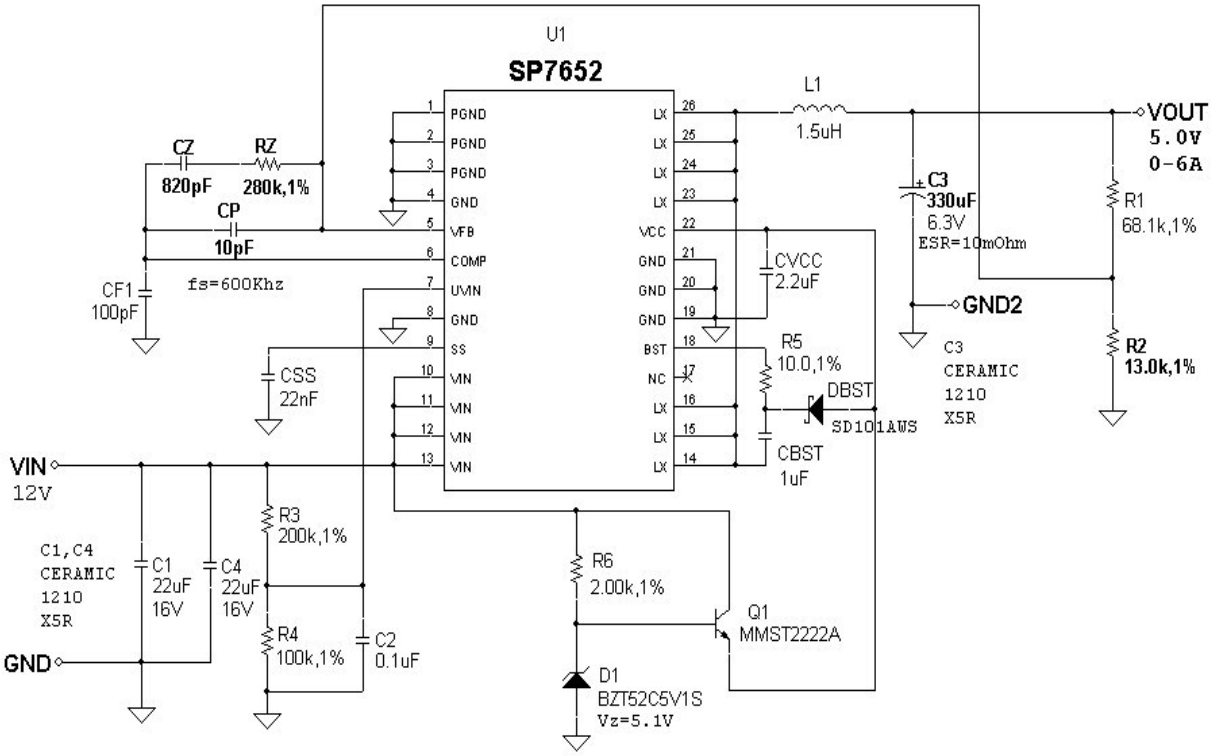


Figure 15. SP7652ER with Tantalum Output Capacitor Configures for +5V Output

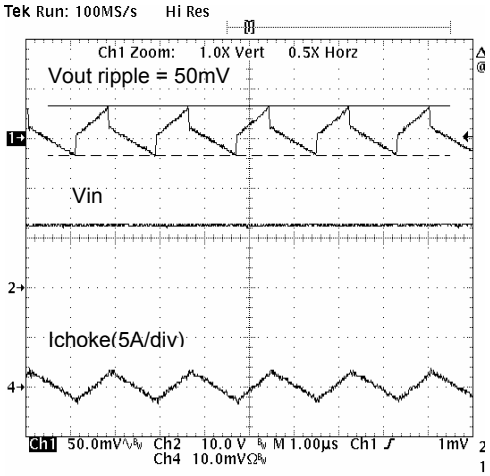


Figure 16. Output Ripple: No Load

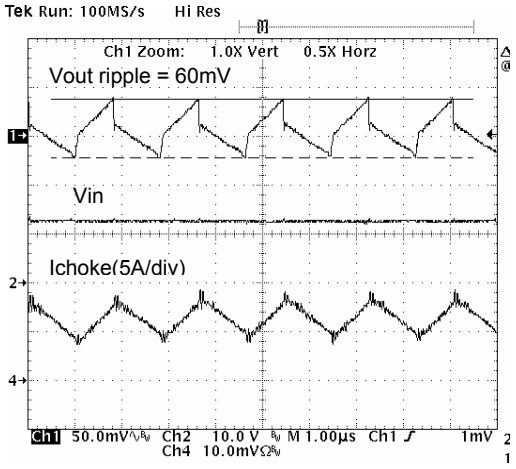


Figure 17. Output Ripple: 6A Load

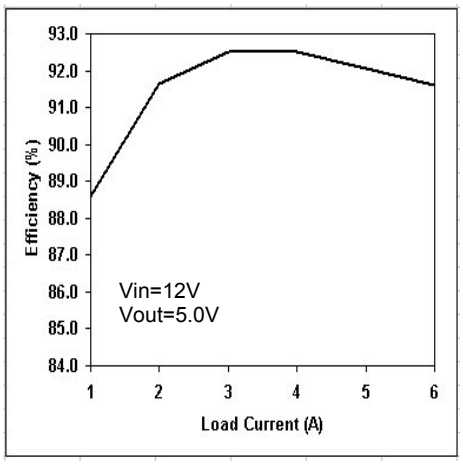


Figure 18. Efficiency vs Load

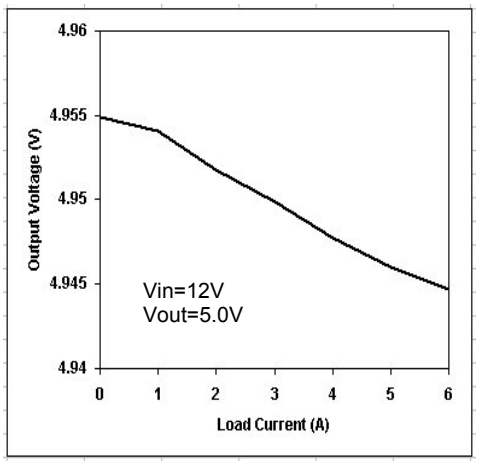


Figure 19. Load Regulation

+5V INPUT WITH A TYPE II COMPENSATION APPLICATION SCHEMATIC

SP7652ER with Tantalum output capacitor configures for Vin = 5V, Vout = +3.3V at 0-6A output current. Figure 21 and 22 show output voltage ripple less than 60mV at no load to 6A load. Figure 23 and 24 show typical 94% efficiency and 0.3% load regulation plots with a Type II compensation application circuits.

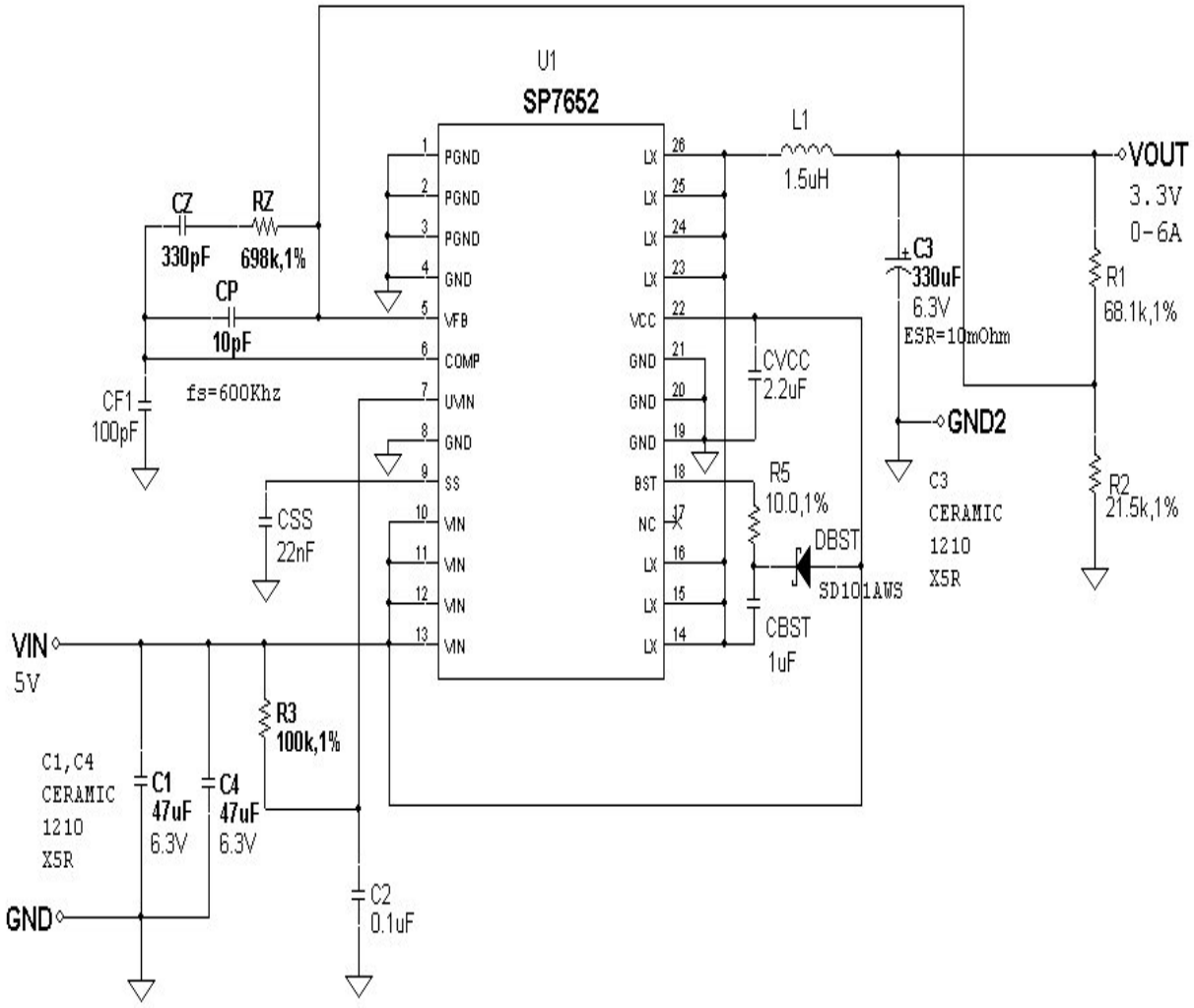


Figure 20. SP7652ER with Tantalum Output Capacitor Configures for +5V Input

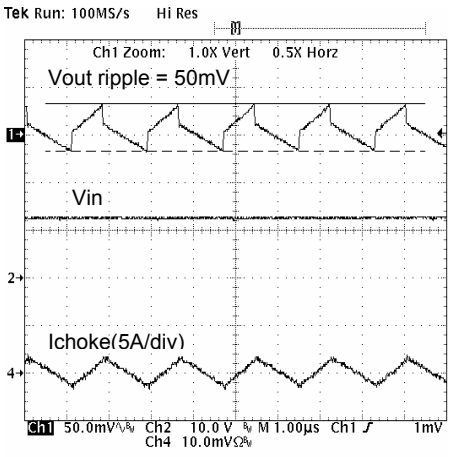


Figure 21. Output Ripple: No Load

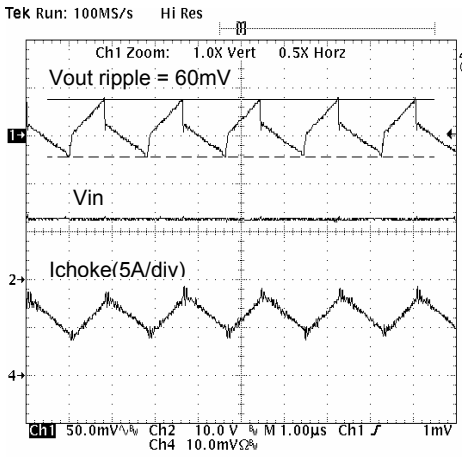


Figure 22. Output Ripple: 6A Load

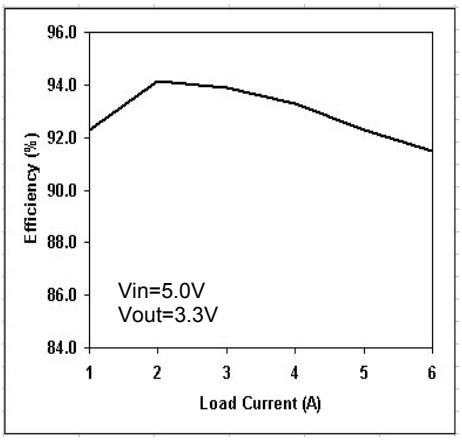


Figure 23. Efficiency vs Load

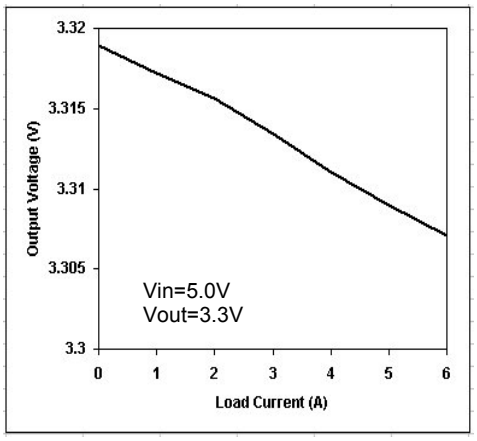


Figure 24. Load Regulation

PC LAYOUT DRAWINGS

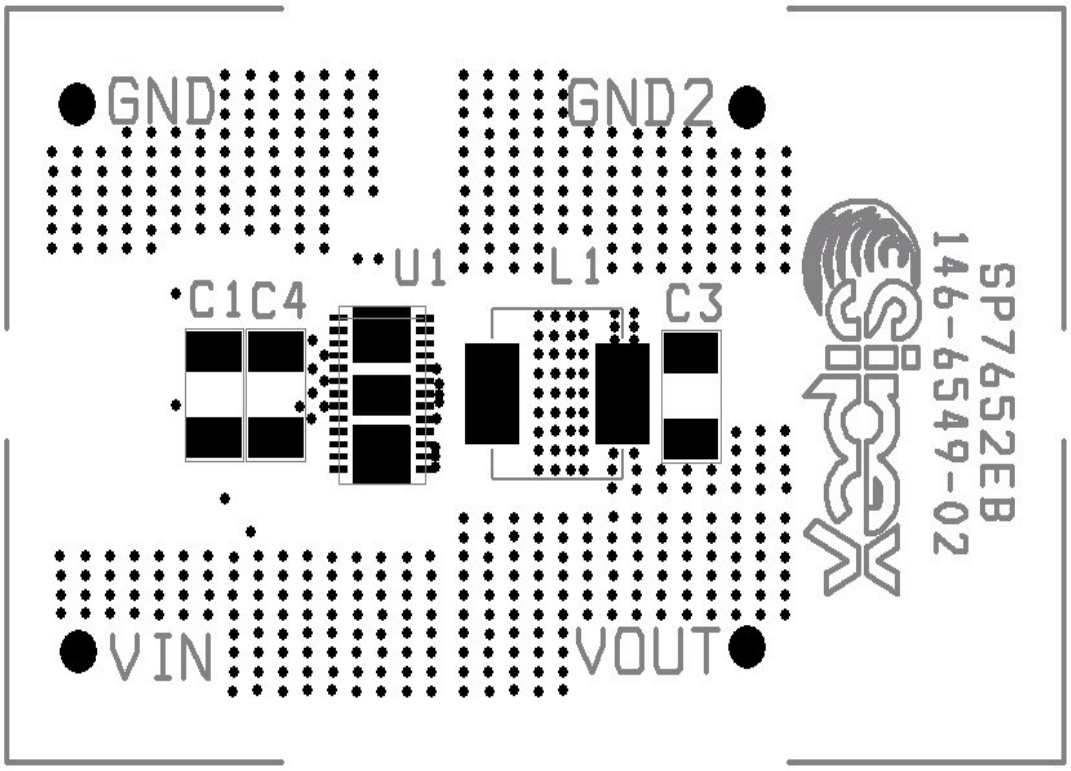


Figure 25. SP7652EB Component Placement

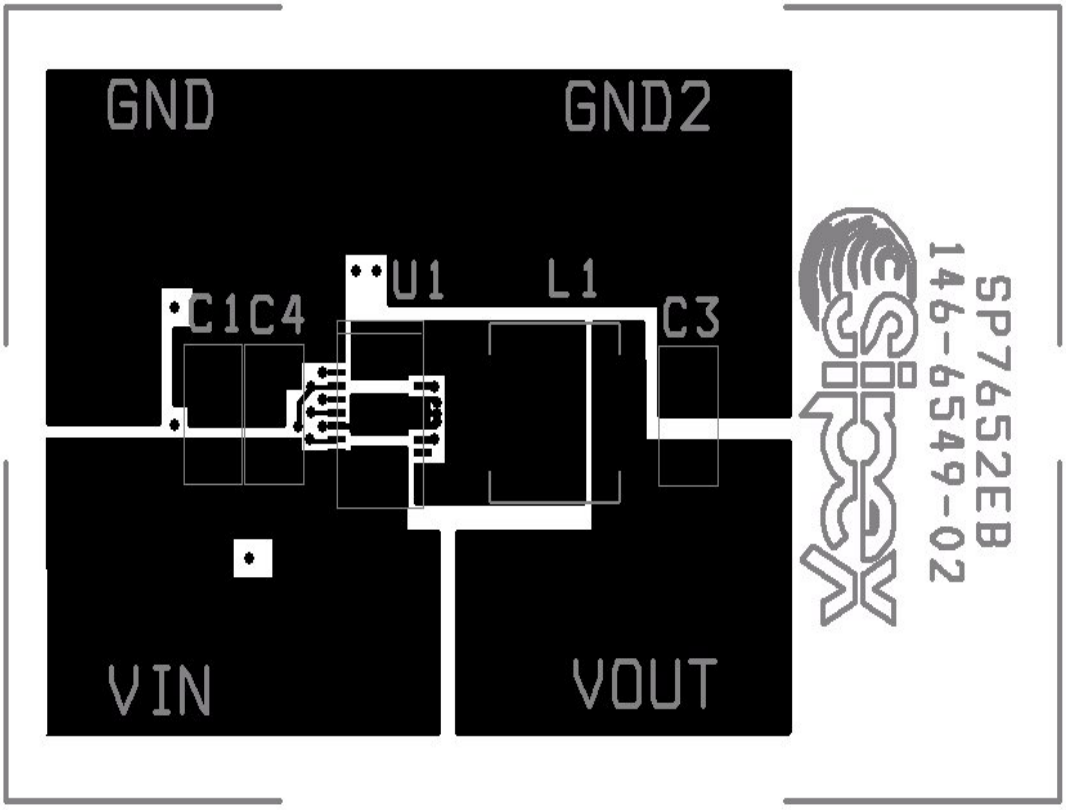


Figure 26. SP7652EB PC Layout Top Side

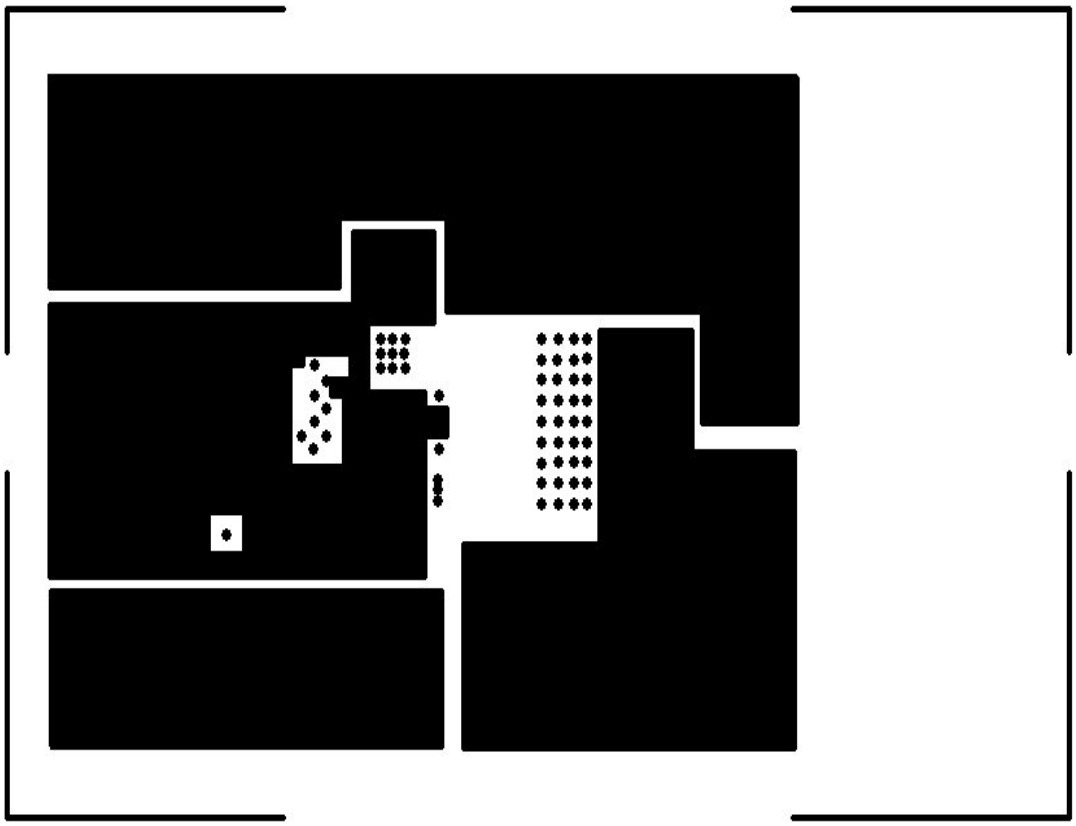


Figure 27. SP7652EB PC Layout 2nd Layer Side

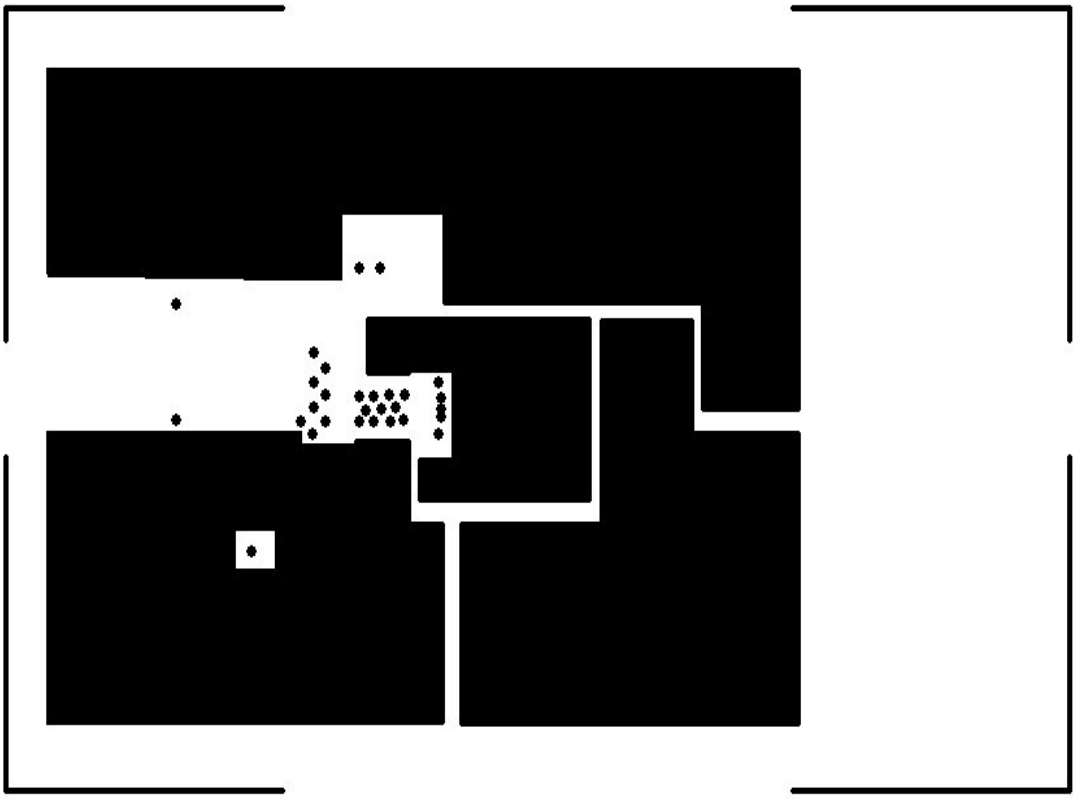


Figure 28. SP7652EB PC Layout 3rd Layer Side

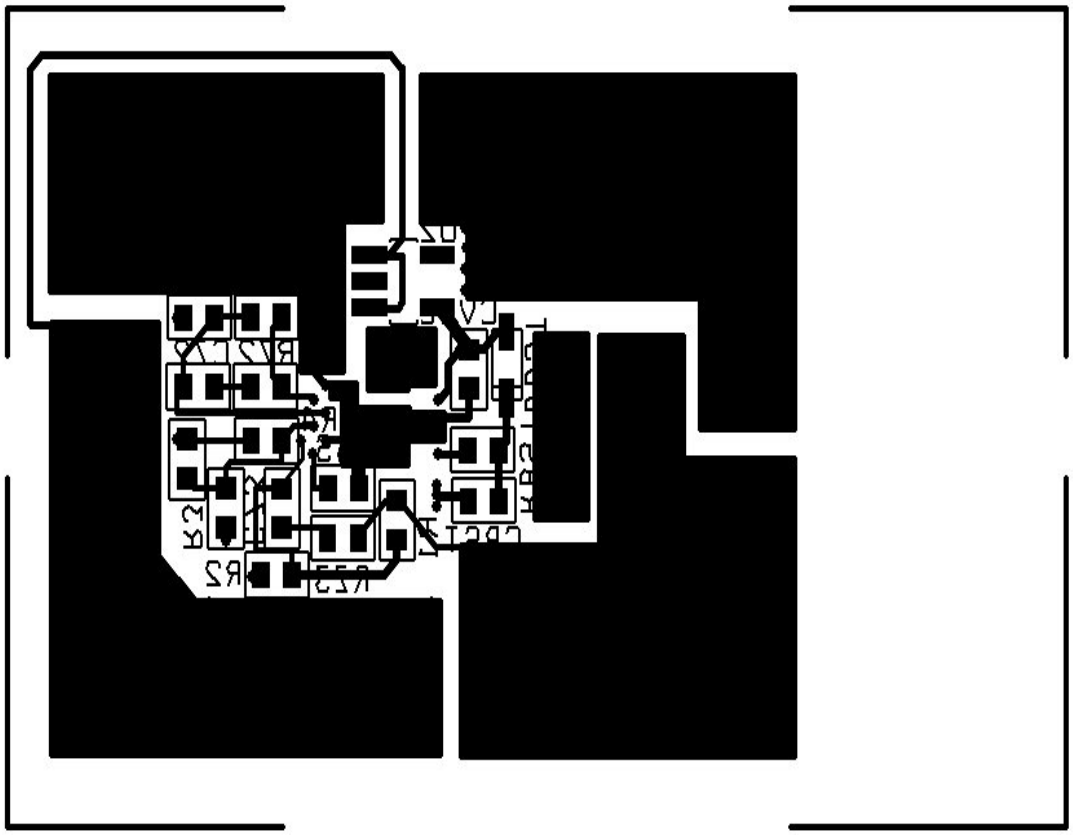


Figure 29. SP7652EB PC Layout Bottom Side

Table 2: SP7652EB List of Materials

			SP7652 Evaluation Board Rev. 02 List of Materials				9/8/2004
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
1	PCB	1	Sipex	146-6549-02	2.75"X1.75"	SP7652EB	978-667-8700
2	U1	1	Sipex	SP7652ER	DFN-26	2-FETs Buck Ctrl	978-667-8700
3	U2	1	Sipex	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Reg	978-667-7800
4	DBST	1	Diodes Inc	SD101AWS	SOD-323	15mA Schottky Diode	805-446-4800
5	L1	1	Vishay dale	IHLP-2525CZ-01-1R5MTR	6.86X6.47mm	1.5uH Coil 18A 14mohm	402-563-6866
6	C3	1	TDK	C3225X5R0J476M	1210	47uF Ceramic X5R 6.3V	603-622-0003
7	C1,C4	2	TDK	C3225X5R1C226M	1210	22uF Ceramic X5R 16V	603-622-0003
8	CVCC	1	TDK	C1608X5R1A225K	0603	2.2uF Ceramic X5R 10V	603-622-0003
9	CBST	1	AVX	0603ZD105KAT2A	0603	1.0uF Ceramic X5R 10V	843-448-9411
10	C2	1	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 50V	603-622-0003
11	CSS	1	AVX	06035C223KAT2A	0603	22,000pF Ceramic X7R 50V	843-448-9411
12	CP1	1	AVX	06035A220JAT2A	0603	22pF Ceramic COG 50V	843-448-9411
13	CZ2	1	AVX	06035A102JAT2A	0603	1,000pF Ceramic COG 50V	843-448-9411
14	CF1, CZ3	2	AVX	06035A101JAT2A	0603	100pF Ceramic COG 50V	843-448-9411
15	RZ2	1	Dale	CRCW0603-1182FRT1	0603	11.8K Ohm Thick Film Res 1%	402-563-6866
16	R2	1	Dale	CRCW0603-2152FRT1	0603	21.5K Ohm Thick Film Res 1%	402-563-6866
17	RZ3	1	Dale	CRCW0603-5231FRT1	0603	5.23K Ohm Thick Film Res 1%	402-563-6866
18	R1	1	Dale	CRCW0603-6812FRT1	0603	68.1K Ohm Thick Film Res 1%	402-563-6866
19	R3	1	Dale	CRCW0603-2003FRT1	0603	200K Ohm Thick Film Res 1%	402-563-6866
20	RBST	1	Dale	CRCW0603-10R0FRT1	0603	10.0 Ohm Thick Film Res 1%	402-563-6866
21	R4	1	Dale	CRCW0603-1003FRT1	0603	100K Ohm Thick Film Res 1%	402-563-6866
22	VIN, VOUT, GND, GND2	4	Vector Electronic	K24C/M	.042 Dia	Input/Output Terminal Posts	800-344-4539

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7652EB	-40°C to +85°C	SP7652 Evaluation Board
SP7652ER	-40°C to +85°C	26-pin DFN