NXP EM783 Electronic components datasheet

The EM783-SC/SP/TP/MC3/MC6 is an ARM Cortex-M0-based, low-cost 32-bit family of application processors, designed for energy measurement and monitoring applications. The EM783 offers programmability and on-chip metrology functionality combined with a low power, simple instruction set. It also has memory addressing together with reduced code size compared to existing 8/16-bit architectures.

EM783

Energy metering IC; 32 kB flash, 8 kB SRAM, 4 kB EEPROM

Rev. 2 — 17 January 2014 | Product data sheet

1. General description

The EM783-SC/SP/TP/MC3/MC6 is an ARM Cortex-M0-based, low-cost 32-bit family of application processors, designed for energy measurement and monitoring applications. The EM783 offers programmability and on-chip metrology functionality combined with a low power, simple instruction set. It also has memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The EM783 operate at CPU frequencies of up to 48 MHz.

The digital peripherals on the EM783 include:

- 32 kB of flash memory
- 4 kB of EEPROM data memory
- 8 kB of SRAM data memory
- Fast-mode Plus I^2C-bus interface
- RS-485/EIA-485 USART
- one SSP controller
- two general-purpose counter/timers
- up to 22 general-purpose I/O pins

A metrology engine with built-in temperature sensor is used for energy measurements. A 10-bit DAC and an internal voltage reference are also available.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 48 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug (SWD).
  - System tick timer.
- Memory:
  - 32 kB on-chip flash program memory.
  - 4 kB on-chip EEPROM data memory for energy registers and calibration parameters; byte erasable and byte programmable.
  - 8 kB SRAM data memory.
  - 16 kB boot ROM.
  - In-System Programming (ISP) for flash and In-Application Programming (IAP) for flash and EEPROM via on-chip bootloader software.
  - Includes ROM-based 32-bit integer division routines.

- Digital peripherals:
  - Up to 22 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 9 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns. Two pins are configurable for 20ns glitch filter and another two pins are configurable for 50 ns glitch filters.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current source output driver (20 mA) on one pin (P0_21).
  - High-current sink driver (20 mA) on true open-drain pins (P0_2 and P0_3).
  - Two general-purpose counter/timers with a total of up to four capture inputs and five match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).
- Analog peripherals:
  - Metrology engine for smart metering with one voltage input, one bias input, from two up to six current inputs and a temperature sensor.
  - Internal voltage reference.
  - 10-bit DAC with flexible conversion triggering.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - One SSP controller with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports ARM Cortex-M0 Sleep mode as reduced power mode.
  - Power profiles residing in boot ROM allowed to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - BrownOut Detect (BOD) with two separate programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage drops below 2.4 V.
- Unique device serial number for identification.

- Single 3.3 V power supply (2.6 V to 3.6 V).
- Temperature range –40 °C to +85 °C.
- Available as a 33-pin HVQFN 7 mm × 7 mm × 0.85 mm package.

3. Applications

- Smart plugs and plug meters
- Single phase residential meters
- Industrial submeters
- Server power monitoring
- Smart appliances

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
EM783-SC	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
EM783-SP	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
EM783-TP	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
EM783-MC3	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
EM783-MC6	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM	EEPROM	Metrology engine inputs	10-bit DAC	USART	SSP/SPI	I^{2}C	Package
EM783-SC	32 kB	8 kB	4 kB	1x I, 1x V	1	1	1	1	HVQFN33
EM783-SP	32 kB	8 kB	4 kB	2x I, 1x V	1	1	1	1	HVQFN33
EM783-TP	32 kB	8 kB	4 kB	3x I, 3x V	1	1	1	1	HVQFN33
EM783-MC3	32 kB	8 kB	4 kB	3x I, 1x V	1	1	1	1	HVQFN33
EM783-MC6	32 kB	8 kB	4 kB	6x I, 1x V	1	1	1	1	HVQFN33

5. Block diagram

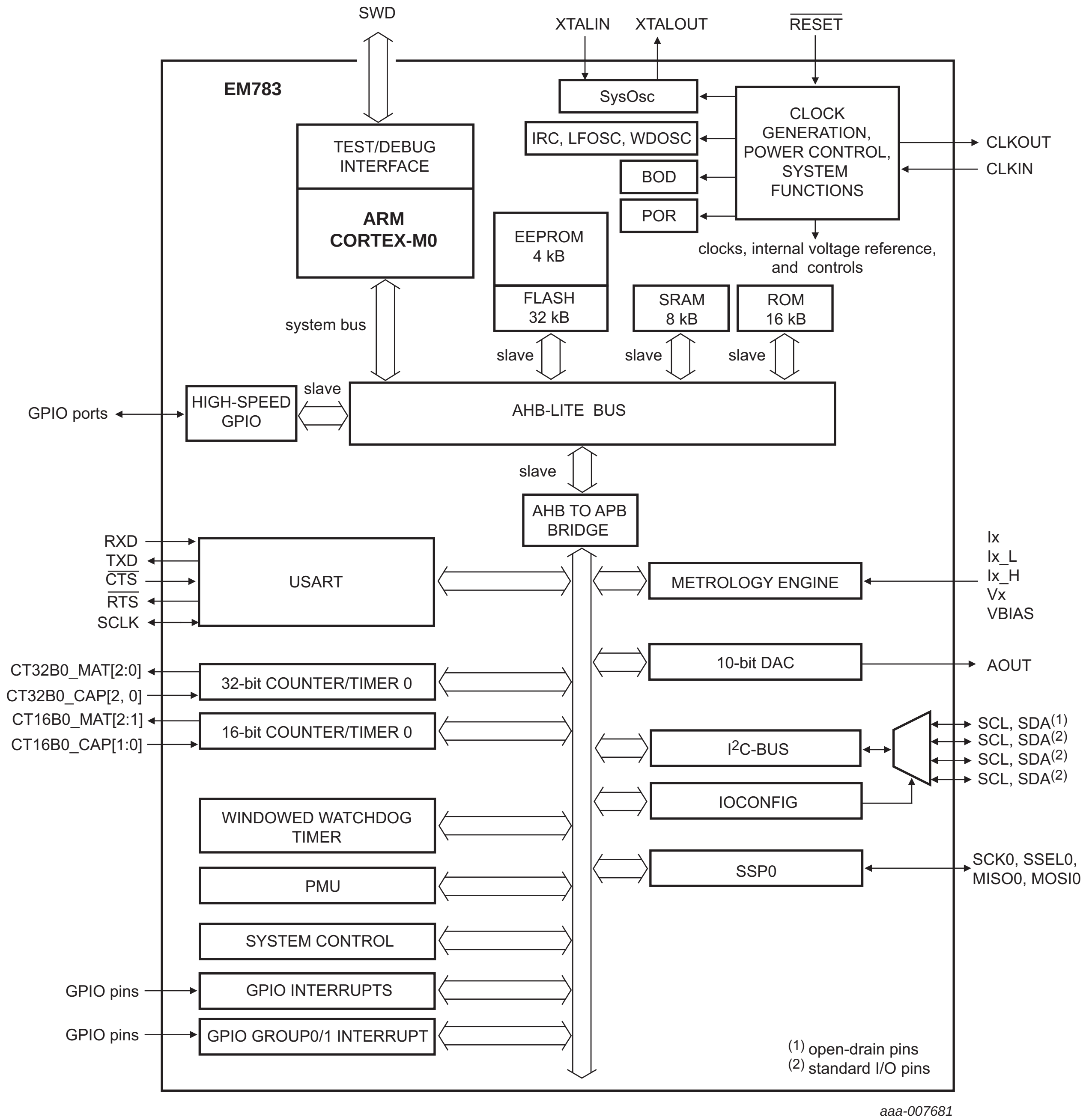
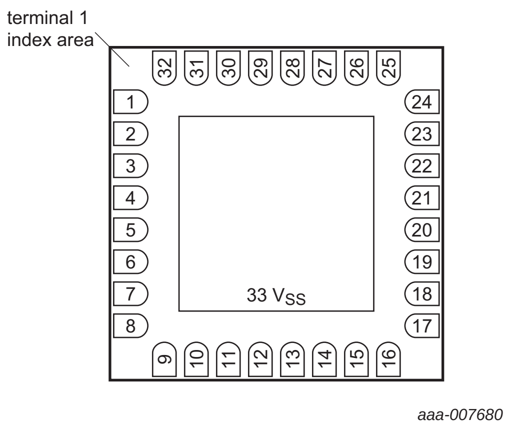


Fig 1. EM783 block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration HVQFN33 package

6.2 Pin description

All functional pins on the EM783, except for metrology inputs, are mapped to GPIO port 0 (see Table 3). The port pins are multiplexed to accommodate more than one function (see Table 4).

The IOCONFIG register, controls the pin function (see the *EM783 user manual*). The standard I/O pad configuration is illustrated in Figure 24 and a detailed pin description is given in Table 4.

Table 3. Pin multiplexing

Function	Type	Port	Glitch filter	Pin
System clocks, reset, and wake-up				
CLKIN	I	P0_1	no	3
		P0_12	no	31
		P0_19	no	9
		P0_24	no	7
CLKOUT	O	P0_1	no	3
		P0_19	no	9
XTALIN	I (analog)	-	-	4
XTALOUT	O (analog)	-	-	5
$\overline{\text{RESET}}$	I	P0_0	20 ns [1]	2
Serial Wire Debug (SWD)				
SWCLK	I	P0_2	50 ns [2]	10
		P0_5	10 ns [2]	19

Table 3. Pin multiplexing *…continued*

Function	Type	Port	Glitch filter	Pin
SWDIO	I/O	P0_3	50 ns [2]	11
		P0_10	10 ns [2]	25
Metrology engine				
V1	I (analog)	-	no	28
VBIAS	I (analog)	-	no	14
V1	I (analog)	-	no	22
VBIAS	I (analog)	-	no	23
I1	I (analog)	-	no	20
I1_L	I (analog)	-	no	20
I1_H	I (analog)	-	no	21
I5	I (analog)	-	no	21
I2_L	I (analog)	-	no	24
I2	I (analog)	-	no	24
I2_H	I (analog)	-	no	25
V2	I (analog)	-	no	25
I6	I (analog)	-	no	25
I3_L	I (analog)	-	no	26
I3	I (analog)	-	no	26
I3_H	I (analog)	-	no	27
I4	I (analog)	-	no	27
V3	I (analog)	-	no	27
Analog peripherals				
AOUT	O (analog)	P0_4	no	18
ATRG0	I (analog)	P0_16	10 ns [2]	13
I²C-bus interface				
SCL	I/O	P0_2	50 ns [2]	10
		P0_12	no	31
		P0_16	10 ns [2]	13
		P0_24	no	7
SDA	I/O	P0_3	50 ns [2]	11
		P0_13	10 ns [2]	32
		P0_15	10 ns [2]	27
		P0_25	no	12
SSP0 controller				
MISO0	I/O	P0_22	10 ns [2]	17
MOSI0	I/O	P0_4	10 ns [2]	18
		P0_19	no	9
SCK0	I/O	P0_5	10 ns [2]	19
		P0_20	no	15

Table 3. Pin multiplexing *…continued*

Function	Type	Port	Glitch filter	Pin
SSEL0	I/O	P0_1	no	3
		P0_18	no	8
USART				
RXD	I	P0_1	no	3
		P0_12	no	31
TXD	O	P0_13	no	32
		P0_15	no	27
		P0_26	no	1
SCLK	I/O	P0_11	10 ns [2]	26
		P0_21	no	16
		P0_23	no	30
$\overline{CTS}$	I	P0_9	10 ns [2]	24
		P0_21	no	16
$\overline{RTS}$	O	P0_10	no	25
		P0_23	no	30
16-bit counter/timer CT16B0				
CT16B0_CAP0	I	P0_2	50 ns [2]	10
		P0_18	no	8
CT16B0_CAP1	I	P0_16	10 ns [2]	13
CT16B0_MAT1	O	P0_4	no	18
		P0_9	no	24
CT16B0_MAT2	O	P0_5	no	19
		P0_10	no	25
32-bit counter/timer CT32B0				
CT32B0_CAP0	I	P0_11	10 ns [2]	26
		P0_23	no	30
CT32B0_CAP2	I	P0_15	10 ns [2]	27
		P0_26	no	1
CT32B0_MAT0	O	P0_12	no	31
CT32B0_MAT1	O	P0_13	no	32
CT32B0_MAT2	O	P0_1	no	3
Supply and ground pins				
$V_{DD(IO)}$	Supply	-	-	6
$V_{DD(3V3)}$	Supply	-	-	29
V_{SS}	Ground	-	-	33
$V_{SS(IO)}$	Ground	-	-	33

[1] Always on.

[2] Programmable on/off. By default, the glitch filter is disabled.

Table 4 shows all pins in order of increasing pin number. The default function after reset is listed first. Port pins P0_0 to P0_26 have internal pull-up resistors enabled after reset except for the true open-drain pins P0_2 and P0_3.

Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCONFIG registers for each of the port pins.

Table 4. EM783 pin description

Pin no.	EM783 symbol						Type	Reset state [1]	Description
	SC	SP	TP	MC3	MC6				
1	P0_26/TXD/CT32B0_CAP2					[2]	I/O	I; PU	**P0_26 —** General-purpose digital input/output pin.
							O	-	**TXD —** Transmitter data output for USART.
							I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
2	$\overline{\text{RESET}}$/P0_0					[3]	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with fixed 20 ns glitch filter: A LOW going pulse on this pin resets the device. It causes I/O ports and peripherals to take on their default states and processor execution to begin at address 0.
							I/O	-	**P0_0 —** General-purpose digital input/output pin.
3	P0_1/RXD/CLKOUT/CT32B0_ MAT2/SSEL0/CLKIN					[2]	I/O	I; PU	**P0_1 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
							I	-	**RXD —** Receiver data input for USART.
							O	-	**CLKOUT —** Clock output.
							O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
							I/O	-	**SSEL0 —** Slave Select for SSP0.
							I	-	**CLKIN —** External clock input.
4	XTALIN					[4]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
5	XTALOUT					[4]	-	-	Output from the oscillator amplifier.
6	$V_{DD(IO)}$					[5] [6]	-	-	3.3 V input/output supply voltage.
7	P0_24/SCL/CLKIN					[2]	I/O	I; PU	**P0_24 —** General-purpose digital input/output pin.
							I/O	-	**SCL —** I^{2}C-bus clock input/output. This pin is not an I^{2}C-bus open-drain pin[10].
							I	-	**CLKIN —** External clock input.
8	P0_18/SSEL0/CT16B0_CAP0					[2]	I/O	I; PU	**P0_18 —** General-purpose digital input/output pin.
							I/O	-	**SSEL0 —** Slave Select for SSP0.
							I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
9	P0_19/CLKIN/CLKOUT/MOSI0					[2]	I/O	I; PU	**P0_19 —** General-purpose digital input/output pin.
							I	-	**CLKIN —** External clock input.
							O	-	**CLKOUT —** Clock output.
							I/O	-	**MOSI0 —** Master Out Slave In for SSP0.

Table 4. EM783 pin description *…continued*

Pin no.	EM783 symbol						Type	Reset state [1]	Description
	SC	SP	TP	MC3	MC6				
10	P0_2/SCL/SWCLK/CT16B0_CAP0					[7]	I/O	I; IA	**P0_2 —** General-purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
							I/O	-	**SCL —** I^{2}C-bus clock (true open-drain) input/output with selectable 50 ns input glitch filter. Input glitch filter (50 ns) capable.
							I	-	**SWCLK —** Serial Wire Debug Clock (secondary). Input glitch filter (50 ns) capable.
							I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
11	P0_3/SDA/SWDIO					[7]	I/O	I; IA	**P0_3 —** General-purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
							I/O	-	**SDA —** I^{2}C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
							I/O	-	**SWDIO —** Serial Wire Debug I/O (secondary). Input glitch filter (50 ns) capable.
12	P0_25/SDA					[2]	I/O	I; PU	**P0_25 —** General-purpose digital input/output pin.
							I/O	-	**SDA —** I^{2}C-bus data input/output. This pin is not an I^{2}C-bus open-drain pin[10].
13	P0_16/ATRG0/CT16B0_CAP1/SCL					[8]	I/O	I; PU	**P0_16 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							I	-	**ATRG0 —** Conversion trigger for DAC. Input glitch filter (10 ns) capable.
							I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0. Input glitch filter (10 ns) capable.
							I/O	-	**SCL —** I^{2}C-bus clock input/output. This pin is not an I^{2}C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
14	VBIAS					[8]	I	-	**VBIAS —** Bias voltage input for metrology engine.
15	P0_20/SCK0					[2]	I/O	I; PU	**P0_20 —** General-purpose digital input/output pin.
							I/O	-	**SCK0 —** Serial clock for SSP0.
16	P0_21/$\overline{\text{CTS}}$/SCLK					[2]	I/O	I; PU	**P0_21 —** General-purpose digital input/output pin. If configured as output, this pin is a high-current source output driver (20 mA).
							I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
							I/O	-	**SCLK —** Serial clock for USART.
17	P0_22/MISO0					[2]	I/O	I; PU	**P0_22 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							I/O	-	**MISO0 —** Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.

Table 4. EM783 pin description *…continued*

Pin no.	EM783 symbol SC	SP	TP	MC3	MC6		Type	Reset state [1]	Description
18	P0_4/AOUT/CT16B0_MAT1/MOSI0					[9]	I/O	I; PU	**P0_4 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**AOUT —** DAC output.
							O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
							I/O	-	**MOSI0 —** Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
19	SWCLK/P0_5/CT16B0_MAT2/SCK0					[8]	I	I; PU	**SWCLK —** Primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
							I/O	-	**P0_5 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
							I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.
20	I1_L	I1_L	I1	I1_L	I1	[9]	I	-	**I1_L —** Low-gain current input for metrology engine of SC, SP and MC3 variant.
							I	-	**I1 —** Current input for metrology engine of TP and MC6 variants.
21	I1_H	I1_H	R	I1_H	I5	[8]	I	-	**I1_H —** High-gain current input for metrology engine of SC, SP and MC3 variant.
							I	-	**I5 —** Current input for metrology engine of MC6 variant.
							I	I; PU	**R —** Reserved
22	V1					[8]	I	-	**V1 —** Voltage input for metrology engine.
23	VBIAS					[8]	I	-	**VBIAS —** Bias voltage input for metrology engine.
24	R/P0_9/ CT16B0_ MAT1/$\overline{\text{CTS}}$	I2_L	I2	I2_L	I2	[8]	I	I; PU	**R —** Reserved
							I/O	-	**P0_9 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
							I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART. Input glitch filter (10 ns) capable.
							I	-	**I2_L —** Low-gain current input for metrology engine of SP and MC3 variant.
							I	-	**I2 —** Current input for metrology engine of TP and MC6 variants.

Table 4. EM783 pin description *…continued*

Pin no.	EM783 symbol						Type	Reset state [1]	Description
	SC	SP	TP	MC3	MC6				
25	SWDIO/P0_10/CT16B0MAT2/$\overline{RTS}$	I2_H	V2	I2_H	I6	[8]	I/O	I; PU	**SWDIO —** Primary (default) Serial Wire Debug I/O. Input glitch filter (10 ns) capable.
							I/O	-	**P0_10 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
							O	-	**$\overline{RTS}$ —** Request To Send output for USART.
							I	-	**I2_H —** High-gain current input for metrology engine of SP and MC3 variant.
							I	-	**I6 —** Current input for metrology engine of MC6 variant.
							I	-	**V2 —** Voltage input for metrology engine of TP variant.
26	P0_11/SCLK/CT32B0_CAP0		I3	I3_L	I3	[8]	I/O	I; PU	**P0_11 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							I/O	-	**SCLK —** Serial clock for USART. Input glitch filter (10 ns) capable.
							I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. Input glitch filter (10 ns) capable.
							I	-	**I3_L —** Low-gain current input for metrology engine of MC3 variant.
							I	-	**I3 —** Current input for metrology engine of TP and MC6 variants.
27	P0_15/TXD/CT32B0_CAP2/SDA		V3	I3_H	I4	[8]	I/O	I; PU	**P0_15 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**TXD —** Transmitter data output for USART.
							I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0. Input glitch filter (10 ns) capable.
							I/O	-	**SDA —** I^2C-bus data input/output. This pin is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
							I	-	**I3_H —** High-gain current input for metrology engine of MC3 variant.
							I	-	**I4 —** Current input for metrology engine of MC6 variant.
							I	-	**V3 —** Voltage input for metrology engine of TP variant.
28	V1					[2]	I	-	**V1 —** Voltage input for metrology engine.
29	$V_{DD(3V3)}$					[5] [6]	-	-	3.3 V supply voltage to the metrology engine, internal regulator, and internal clock generator circuits. Also used as the metrology engine reference voltage.
30	P0_23/$\overline{RTS}$/CT32B0_CAP0/SCLK					[2]	I/O	I; PU	**P0_23 —** General-purpose digital input/output pin.
							O	-	**$\overline{RTS}$ —** Request To Send output for USART.
							I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
							I/O	-	**SCLK —** Serial clock for USART.

Table 4. EM783 pin description *…continued*

Pin no.	EM783 symbol						Type	Reset state [1]	Description
	SC	SP	TP	MC3	MC6				
31	P0_12/RXD/CT32B0_MAT0/SCL/CLKIN					[2]	I/O	I; PU	**P0_12 —** General-purpose digital input/output pin.
							I	-	**RXD —** Receiver data input for USART.
							O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
							I/O	-	**SCL —** I^{2}C-bus clock input/output. This pin is not an I^{2}C-bus open-drain pin [10].
							I	-	**CLKIN —** External clock input.
32	P0_13/TXD/CT32B0_MAT1/SDA					[8]	I/O	I; PU	**P0_13 —** General-purpose digital input/output pin. Input glitch filter (10 ns) capable.
							O	-	**TXD —** Transmitter data output for USART.
							O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
							I/O	-	**SDA —** I^{2}C-bus data input/output. This pin is not an I^{2}C-bus open-drain pin [10]. Input glitch filter (10 ns) capable.
33	$V_{SS(IO)}/V_{SS}$						-	-	Ground [11].

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up resistor (weak PMOS device) enabled; IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes and configurable hysteresis (Figure 24).

[3] See Figure 25 for the reset configuration.

[4] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating. See Section 12.1 if an external clock is connected to the XTALIN pin.

[5] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the power supply pins are filtered for noise. Using separate filtered supplies reduces the noise to the metrology engine and analog blocks (see also Section 12.1).

[6] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[7] I^{2}C-bus pins compliant with the I^{2}C-bus specification for I^{2}C standard mode, I^{2}C Fast-mode, and I^{2}C Fast-mode Plus.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, digital section of the pin is disabled, and the pin is not 5 V tolerant (Figure 24).

[9] Not a 5 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, the digital section of the pin is disabled (Figure 24).

[10] I^{2}C-bus pins are standard digital I/O pins and have limited performance and electrical characteristics compared to the full I^{2}C-bus specification. Pins can be configured with an on-chip pull-up resistor (PMOS device) and with open-drain mode. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.

[11] Thermal pad. Connect to ground.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The EM783 contains up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The EM783 contains up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM are reserved and cannot be written to.

7.4 On-chip SRAM

The EM783 contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 Memory map

The EM783 incorporate several distinct memory regions, shown in the following figures. Figure 3 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This space allows simplifying the address decoding for each peripheral.

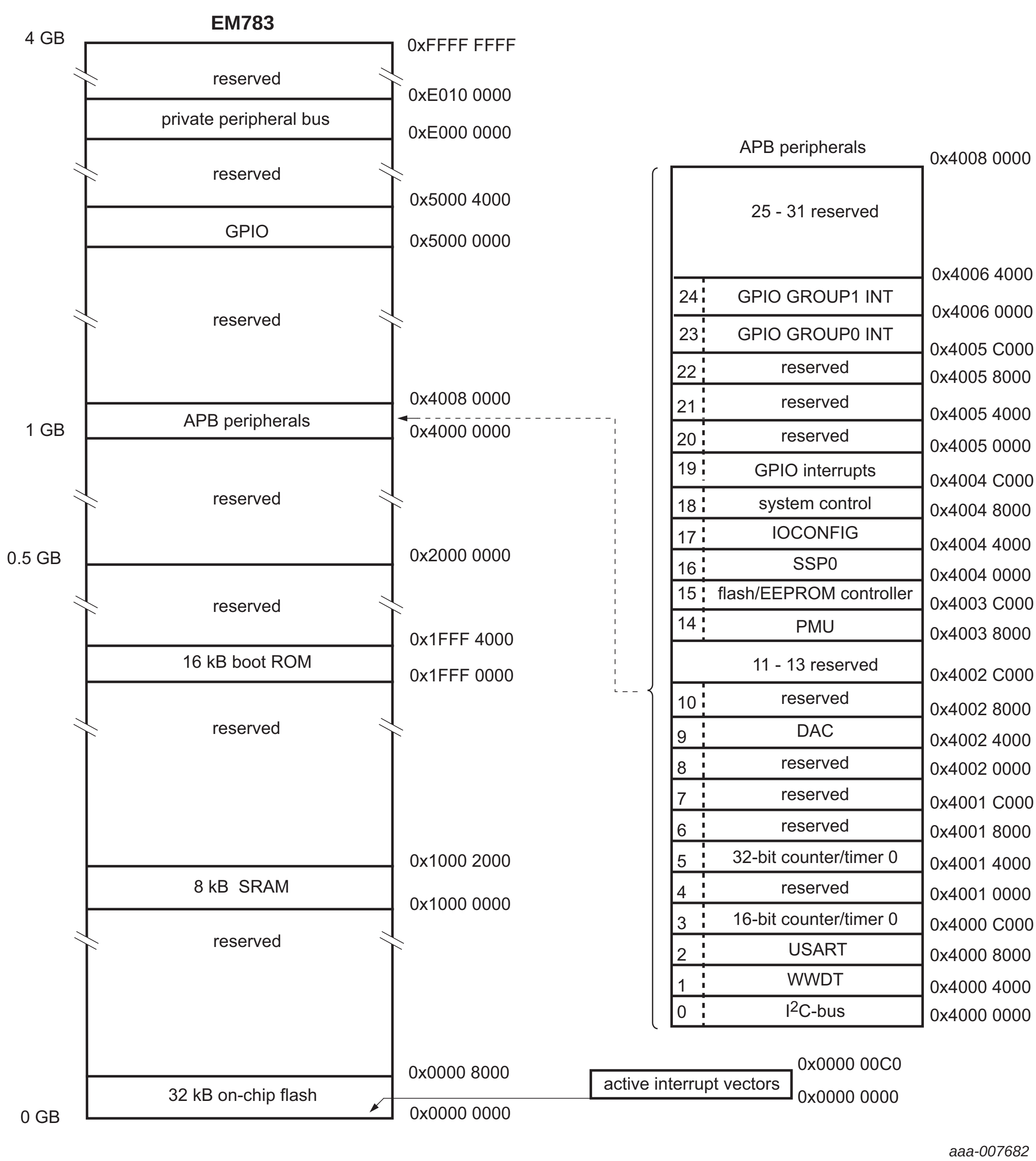


Fig 3. EM783 memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the EM783, the NVIC supports 32 vectored interrupts including up to 8 inputs to the start logic from the individual GPIO pins.

- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight GPIO pins can be programmed to generate an interrupt for a level, and/or a rising edge, and/or a falling edge. The interrupt generating GPIOs can be selected from the GPIO pins with a configurable input glitch filter. The interrupts can be generated regardless of the selected function.

7.7 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins before being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Up to 9 pins can be configured with a digital input glitch filter for removing voltage glitches with widths of 10 ns (see Table 3 and Table 4). Two pins can be configured with a 20 ns input glitch filter. Another two pins can be configured with a 50 ns digital input glitch filter.

7.8 Fast general-purpose parallel I/O

The GPIO registers control the device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

EM783 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- An entire port value can be written in one instruction.

GPIO pins providing a digital function (maximum 22 pins), can be programmed to generate an interrupt for a level, and/or a rising edge, and/or a falling edge.

7.8.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset, except for the I^2C-bus true open-drain pins P0_2 and P0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCONFIG block for each GPIO pin. For the functional diagrams, see Figure 24 and Figure 25.

- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.9 USART

The EM783 contains one USART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.9.1 Features

- Maximum USART data bit rate of 3.125 MBit/s.
- 16 byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Supports a full modem control handshake interface.
- Support for synchronous mode.

7.10 SSP serial I/O controller

The EM783 contains one SSP controller.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full-duplex transfers, with frames of 4 bits to 16 bits of data. The data flows from the master to the slave and from the slave to the master. In practice, often only one of the data-flows carries meaningful data.

7.10.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SPI mode).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

7.11 I²C-bus serial I/O controller

The EM783 contains one I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). A unique address recognizes each device which can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus that can be controlled by more than one bus master connected to it.

7.11.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins (P0_2 and P0_3). The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- The true open-drain pins P0_2 and P0_3 can be configured with a 50 ns digital input glitch filter.
- If the true open-drain pins are used for other purposes, a limited-performance I²C-bus interface can be configured from a choice of six GPIO pins. The six GPIO pins are configured in open-drain mode and with a pull-up resistor. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.
- Easy to configure as master, slave, or master/slave.
- Fail-safe operation. When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C-bus are floating and do not disturb the bus.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.12 Metrology engine

The EM783 contains a metrology engine designed to collect voltage and current inputs. It uses these inputs to calculate the active power, reactive power, apparent power and power factor of a load. The purpose of the metrology engine is for billing and non-billing applications such as plug meters, smart appliances, industrial and consumer submeters.

7.12.1 Features

- Up to 1.0 % accurate for scalable input sources. It maintains this accuracy with a factor of 1 to 1000 down from the maximum current.
- Automatically calculates:
  – Vrms
  – Irms
  – active power in W
  – reactive power in VAR
  – apparent power in VA
  – power factor
  – fundamental reactive power in VAR
  – fundamental apparent power in VA
  – fundamental power factor
  – non-fundamental apparent power
  – non-active power
  – total harmonic distortion of the current
  – mains frequency
  – CPU core temperature
- Standard API for initializing, starting, stopping and reading data from the metrology engine using the ARM Cortex-M0.
- Temperature measurement supporting temperature compensation. The temperature sensor has a maximum error of ±3 degrees °C over the ambient temperature range of –40 °C to +85 °C.
- Very accurate mains frequency measurement.
- Mains frequency operating range of 45 Hz to 65 Hz.
- EEPROM can be used for energy registers and calibration parameters.
- Measurements and active power according to IEC 62053-21.

7.13 10-bit DAC

The DAC allows generation of a variable, rail-to-rail analog output.

7.13.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
  – write operations to the DAC register.

  - a transition of pin ATRG0. Input signal must be held for a minimum of three system clock periods.
  - a timer match signal.
- If the DAC is not powered down, it holds the output value during Sleep mode.

7.14 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V. This value varies typically only ±3 mV over the 0 °C to 85 °C temperature range (see Table 21 and Figure 21).

7.15 General-purpose external event counter/timers

The EM783 includes one 32-bit counter/timer and one 16-bit counter/timer. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt. Up to three capture channels are pinned out.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.16 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.17 Windowed WatchDog Timer (WWDT)

If software fails to service the controller periodically within a programmable time window, the purpose of the watchdog is to reset it.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before a watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- If enabled, an incorrect feed sequence causes a reset or interrupt.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Clocking and power control

7.18.1 Crystal and internal oscillators

The EM783 include four independent oscillators.

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1 % accuracy.
3. The internal low-power, Low-Frequency Oscillator (LFOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40 % accuracy.
4. The dedicated WatchDog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40 % accuracy.

Each oscillator, except the WDOsc, can be used for more than one purpose as required in a particular application.

Following reset, the EM783 operates from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the EM783 clock generation.

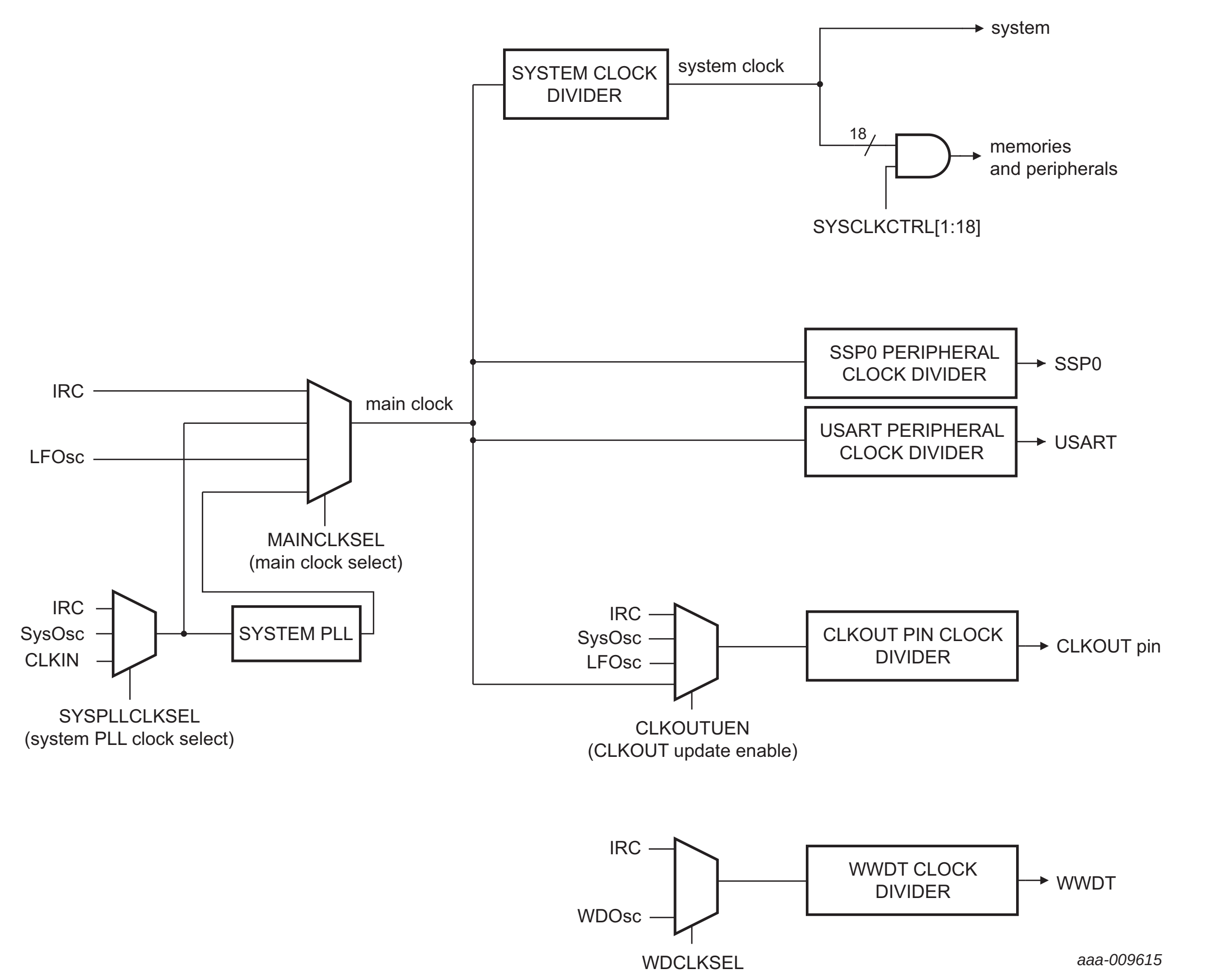


Fig 4. EM783 clock generation block diagram

7.18.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the EM783 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Internal Low-Frequency Oscillator (LFOsc) and WatchDog Oscillator (WDOsc)

The LFOsc and the WDOsc are identical internal oscillators. The nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ±40 %.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The LFOsc can be used as a clock source that directly drives the CPU or the CLKOUT pin.

7.18.2 Clock input

A 3.3 V external clock source (25 MHz typical) can be supplied on the selected CLKIN pin. A 1.8 V external clock source can be supplied on the XTALIN pin (see Section 12.1).

7.18.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. There is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. Software can enable the PLL and it is turned off and bypassed following a chip reset. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.4 Clock output

The EM783 features a clock output function that routes the IRC, the SysOsc, the LFOsc, or the main clock to an output pin.

7.18.5 Wake-up process

The EM783 begin operation at power-up and when awakened from Deep power-down mode by using the IRC as the clock source. This allows chip operation to resume quickly. If the application requires the SysOsc, the external clock source, or the PLL, software must enable these features. Before using them as a clock source, wait for them to stabilize.

7.18.6 Power control

The EM783 supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This control allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. The clock control allows fine-tuning of power consumption. It eliminates all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.6.2 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the EM783 for one of the following power modes:

- Power mode 0: Default mode corresponding to power configuration after reset.
- Power mode 1: CPU performance mode corresponding to optimized processing capability.
- Power mode 2: Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Power mode 3: Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.19 System control

7.19.1 UnderVoltage LockOut (UVLO) protection

See Section 10.1 “Power supply fluctuations” for details on the settling times of the BOD and POR circuits. These circuits constitute the UVLO protection.

7.19.2 Reset

Reset has four sources on the EM783: the $\overline{\text{RESET}}$ pin, the WatchDog reset, power-on reset (POR), the ARM SYSRESETREQ software request and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin and uses a special pad (see Figure 25). Assertion of chip reset by any source (after the operating voltage attains a usable level) starts the IRC and initializes the flash controller. After the BOD and the POR resets are released, the internal reset timer counts for 100 μs until the internal reset is removed.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

Writing to a special function register allows the software to reset peripherals such as the I^{2}C-bus interface, USART, SSP controller, counter/timers and DAC.

7.19.3 Brownout detection

The EM783 includes two programmable levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. To cause a CPU interrupt, this signal is enabled for interrupt in the Interrupt Enable Register in the NVIC. Software can monitor the signal by reading a dedicated status register. In addition, the BOD circuit supports one hardware controlled voltage level for triggering a chip reset.

7.19.4 Code security (Code Read Protection - CRP)

This feature of the EM783, allows different levels of security to be enabled in the system. It is used to restrict access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System-Programming (ISP). When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. The CRP does not affect IAP commands.

In addition, ISP entry via the P0_1 pin can be disabled without enabling CRP. Refer to the *EM783 user manual* for specific details.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using P0_1 pin. To enable flash update via the USART, the user application must provide a flash update mechanism using IAP calls or call reinvoke ISP command.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin P0_1 for valid user code can be disabled. Refer to the *EM783 user manual* for specific details.

7.19.5 APB interface

The APB peripherals are located on one APB bus.

7.19.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.19.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial Wire Debug (SWD) with four breakpoints and two watchpoints is supported.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	–0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[2][3][4]	–0.5	+5.5	V
		on pins P0_2 and P0_3	[5]	–0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[6]	–0.5	$V_{DD(IO)}$	V
		metrology	[7]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[8]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	–6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages relate to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins P0_2 and P0_3 and except the 3 V tolerant pins P0_4 and P0_5.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] Applies to 3 V tolerant pins P0_4 and P0_5.

[7] A Metrology engine input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the metrology engine inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] Dependent on package type.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			2.6	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			2.6	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash; $V_{DD(3V3)} = V_{DD(IO)}$ = 3.3 V; low-current mode (see Section 7.18.6.2)					
		system clock = 12 MHz; all peripherals disabled	[2][4][5]	-	3	-	mA
		system clock = 48 MHz; all peripherals disabled	[2][6][5]	-	8	-	mA
		Sleep mode; system clock = 12 MHz; $V_{DD(3V3)} = V_{DD(IO)}$ = 3.3 V; power mode 0 (see Section 7.18.6.2)					
		all peripherals disabled; 12 MHz	[2][4][5]	-	2	-	mA
		all peripherals disabled; 48 MHz	[2][4][5]	-	5	-	mA
Standard port pins, $\overline{RESET}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	1000	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	0.5	1000	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	0.5	1000	nA
V_I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
		5 V tolerant pins					
		3 V tolerant pins: P0_4 and P0_5	[7][8]			$V_{DD(IO)}$	
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V

Table 6. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	$3.0 V \leq V_{DD(IO)} \leq 3.6 V$		0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.6 V \leq V_{DD(IO)} \leq 3.6 V$; $I_{OH} = -4 mA$		$0.85V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	$2.6 V \leq V_{DD(IO)} \leq 3.6 V$; $I_{OL} = 4 mA$		-	-	$0.15V_{DD(IO)}$	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4 V$; $2.6 V \leq V_{DD(IO)} \leq 3.6 V$		−4	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4 V$ $2.6 V \leq V_{DD(IO)} \leq 3.6 V$		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0 V$	[9]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5 V$	[10]	10	50	150	µA
I_{pu}	pull-up current	$V_I = 0 V$; $2.6 V \leq V_{DD(IO)} \leq 3.6 V$		−15	−50	−85	µA
		$V_{DD(IO)} < V_I < 5 V$		0	0	0	µA
High-drive output pin (P0_21)							
I_{IL}	LOW-level input current	$V_I = 0 V$; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0 V$; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.6 V \leq V_{DD(IO)} \leq 3.6 V$; $I_{OH} = -20 mA$		$V_{DD(IO)} - 0.4$	-	-	V
		$2.6 V \leq V_{DD(IO)} < 2.5 V$; $I_{OH} = -12 mA$		$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.6 V \leq V_{DD(IO)} \leq 3.6 V$; $I_{OL} = 4 mA$		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4 V$; $2.6 V \leq V_{DD(IO)} \leq 3.6 V$		20	-	-	mA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−160	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = $V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−15	−50	−85	μA
		$V_{DD(IO)}$ < V_I < 5 V		0	0	0	μA
I^2C-bus pins (P0_2 and P0_3)							
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3$V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.05$V_{DD(IO)}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as high-current sink pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		20	-	-	mA
I_{LI}	input leakage current	V_I = $V_{DD(IO)}$	[11]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; SysOsc disabled; system PLL disabled.

[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

[6] IRC disabled; SysOsc enabled; system PLL enabled.

[7] Including voltage on outputs in 3-state mode.

[8] All supply voltages must be present.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

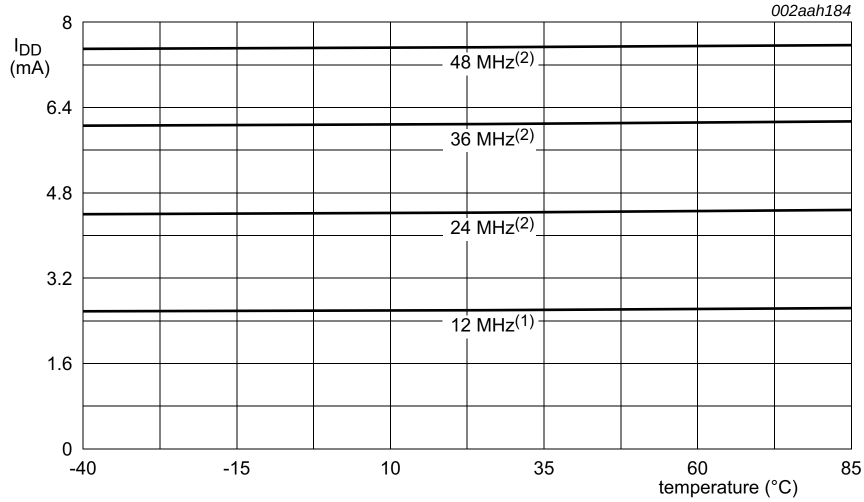
[10] Does not apply to 3 V tolerant pins P0_4.

[11] To V_{SS}.

9.1 Power consumption

Power measurements in Active and Sleep modes were performed under the following conditions (see *EM783 user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOn DIR registers.
- Drive all GPIO outputs to low.

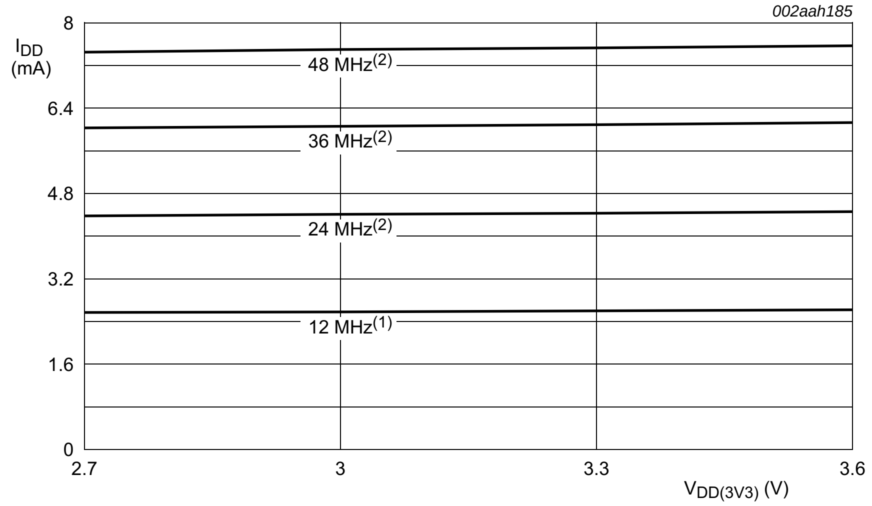


Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; power mode 0 (see Section 7.18.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 5. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals disabled)

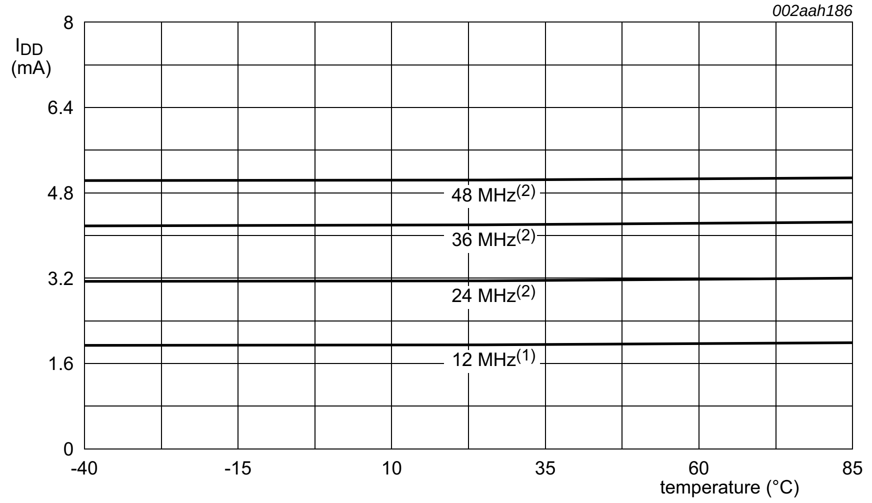


Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals enabled in the SYSAHBCLKCTRL register; all analog peripherals enabled in the PDRUNCFG register; power mode 0 (see Section 7.18.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 6. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals enabled)



Conditions: $V_{DD(3V3)}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register and PDRUNCFG register; all peripheral clocks disabled; BOD disabled; power mode 0 (see Section 7.18.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 7. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies (all peripherals disabled)

9.2 Peripheral power consumption

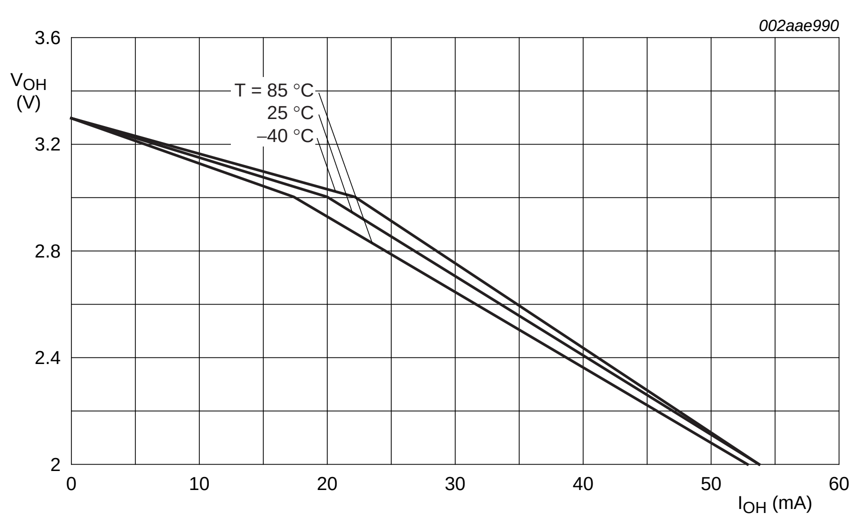
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	Average µA/MHz
	12 MHz [1]	
Analog peripherals		
BOD	0.05	-
Metrology engine	0.10	-
DAC	0.26	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0	0.02	2
32-bit counter/timer 0	0.02	2
WWDT	0.02	2

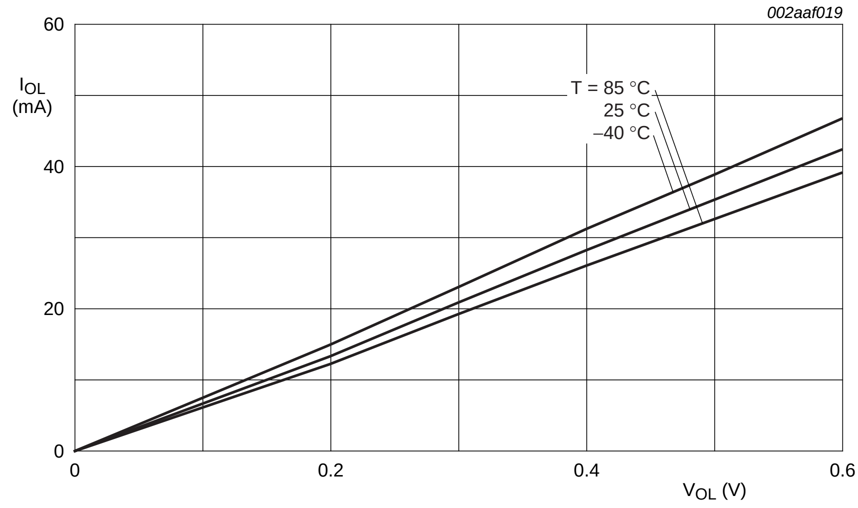
[1] IRC on; PLL off.

9.3 Electrical pin characteristics



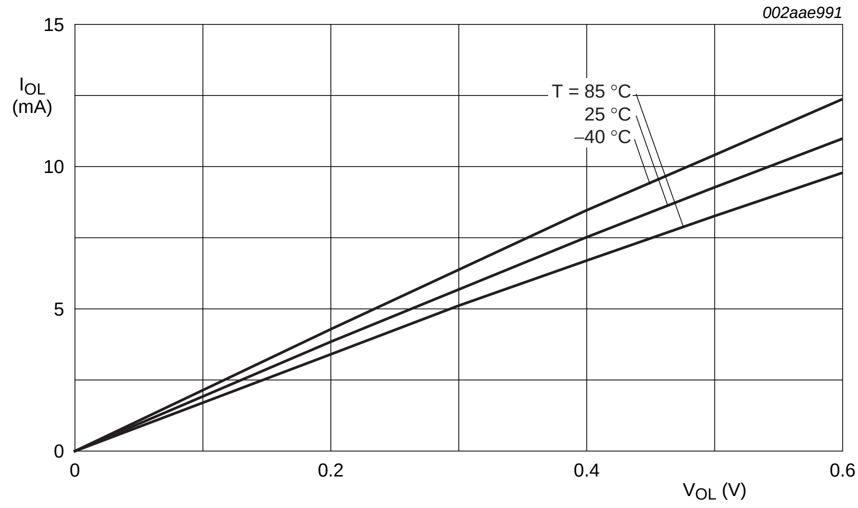
Conditions: $V_{DD(IO)}$ = 3.3 V; on pin P0_21.

Fig 8. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



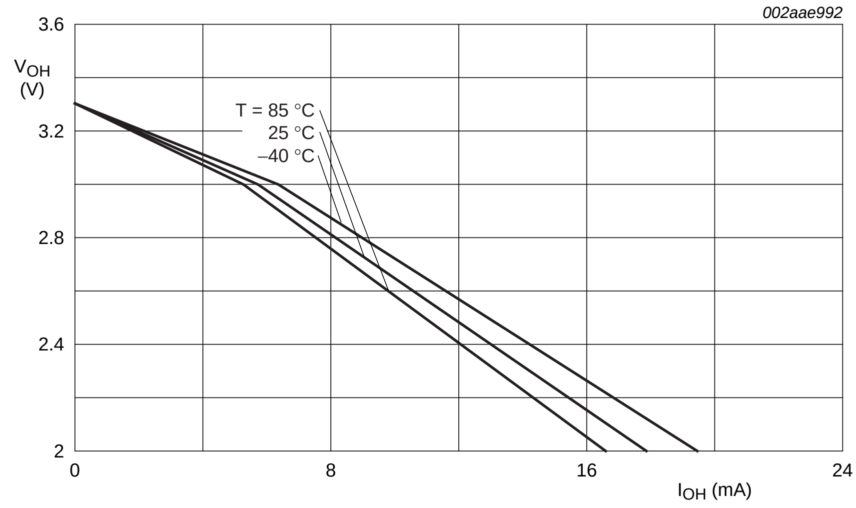
Conditions: $V_{DD(IO)}$ = 3.3 V; on pins P0_2 and P0_3.

Fig 9. High-current sink pins: Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



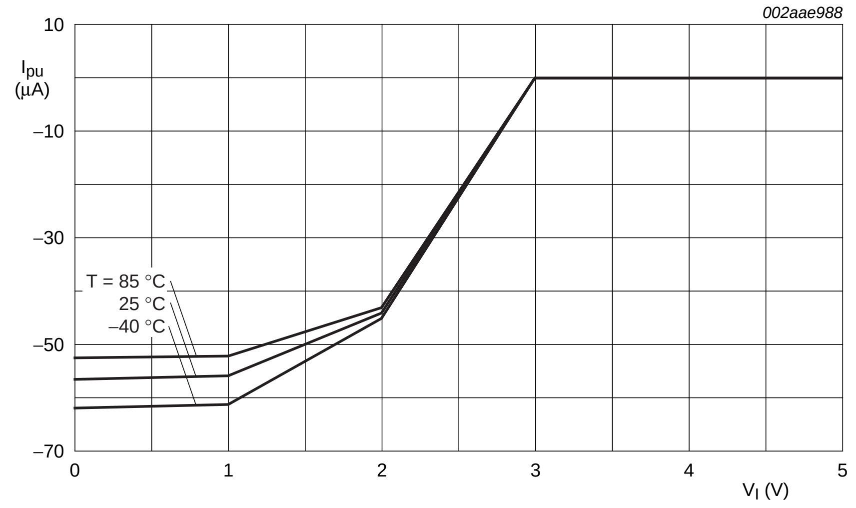
Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins and P0_21.

Fig 10. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



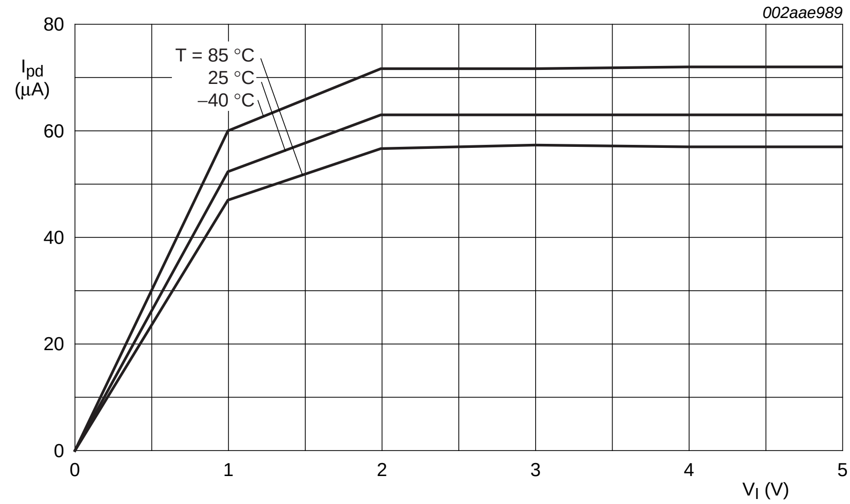
Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 11. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Power supply fluctuations

If the input voltage ($V_{DD(3V3)}$) to the internal regulator fluctuates, the EM783 is held in reset during a brownout condition as long as the UVLO circuit is operating. The settling times of the BOD and POR circuits, which constitute the UVLO, determine the minimum time the supply level must remain in the shallow or deep brownout condition. This time ensures that the internal reset is asserted properly.

Table 8. POR and BOD circuit settling characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_s	settling time	power droop:				
		from active level to shallow brownout level ($0.9\ V \leq V_{DD(3V3)} \leq 2.4\ V$)	5	-	-	µs
		from active level to deep brownout level ($0\ V < V_{DD(3V3)} < 0.9\ V$)	12	-	-	µs

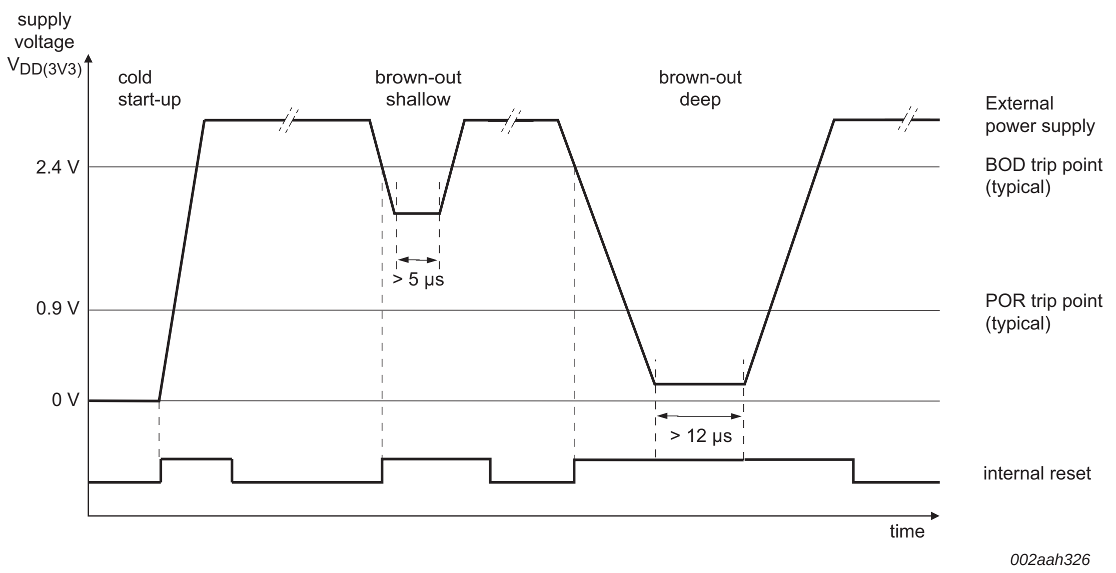


Fig 14. UVLO timing

10.2 Power supply voltage profile

The use of power supply ramp-up and ramp-down procedures outside of the specification shown in Table 9 results in functional failure of the EM783.

Table 9. Power supply ramp characteristics

T_{amb} = –40 °C to 85 °C. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Cold power-up (see regions A to C in Figure 15)							
t_{wait}	wait time	**Region A**: power-down supply voltage = GND	[1]	-	-	-	-
t_r	rise time	**Region B**: ramp up GND ≤ supply voltage ≤ V_{DD}		0	-	-	µs
t_{wait}	wait time	**Region C**: powered-up supply voltage = V_{DD}		150	-	-	µs
Shallow power droop cycle (see regions D to G in Figure 15); BOD enabled							
t_f	fall time	**Region D**: ramp down V_{DD} ≥ supply voltage > $V_{th(fast\_ramp)}$		0	-	-	µs
t_{wait}	wait time	**Region E**: power-down $V_{th(fast\_ramp)}$ < supply voltage < $V_{th(UVLO)}$		5	-	-	µs
t_r	rise time	**Region F**: ramp up $V_{th(fast\_ramp)}$ < supply voltage < V_{DD}		0	-	-	µs
t_{wait}	wait time	**Region G**: powered-up supply voltage = V_{DD}		5	-	-	µs
Deep power droop cycle (see regions H to J in Figure 15)							
t_{wait}	wait time	**Region H**: power-down GND < supply voltage < $V_{th(fast\_ramp)}$		12	-	-	µs
t_r	rise time	**Region I**: ramp up GND < supply voltage < V_{DD}		0	-	-	µs
t_{wait}	wait time	**Region J**: powered-up supply voltage = V_{DD}		150	-	-	µs
Voltage thresholds							
$V_{th(droop)}$	droop threshold voltage			-	900	-	mV

[1] Values are derived from simulation.

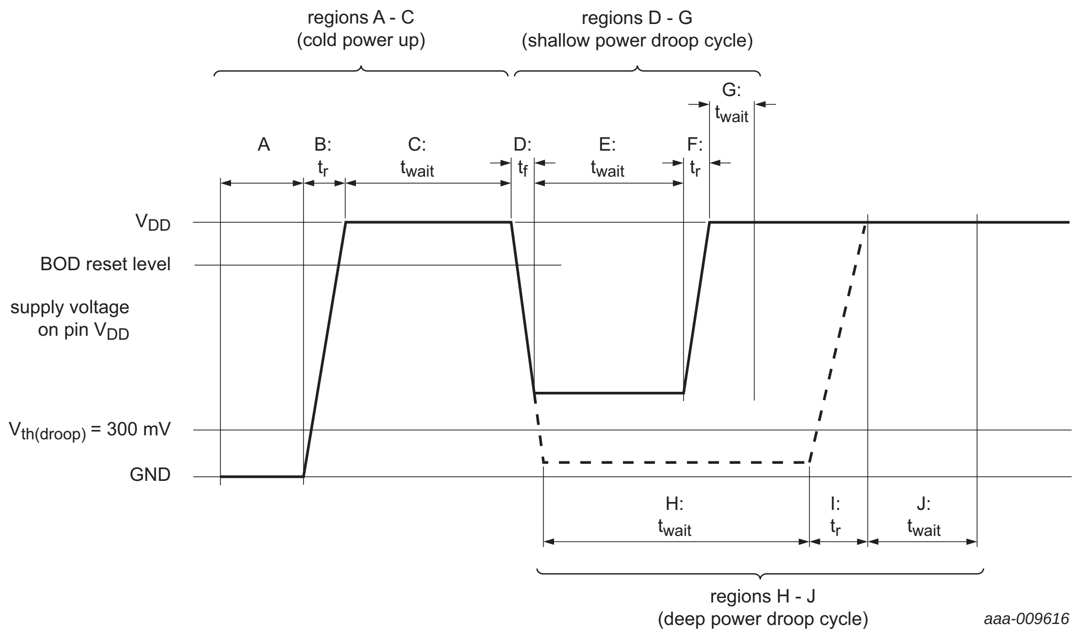


Fig 15. Power supply voltage profile

10.3 Flash/EEPROM memory

Table 10. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *EM783 user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 ms and 2 ms per 256 bytes.

Table 11. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ = 2.6 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{er}	erase time	64 bytes	-	1.8	-	ms
t_{prog}	programming time	64 bytes	-	1.1	-	ms

10.4 External clock for oscillator in slave mode

Remark: The input voltage on the XTALIN pin must be ≤ 1.95 V (see Table 6). For connecting the oscillator to the XTALIN/XTALOUT pins, see Section 12.1.

Table 12. Dynamic characteristic: external clock (XTALIN or CLKIN pin)

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$t_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$t_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$t_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

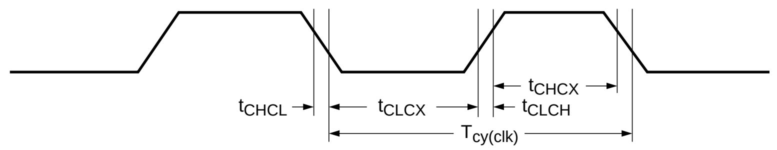


Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.5 Internal oscillators

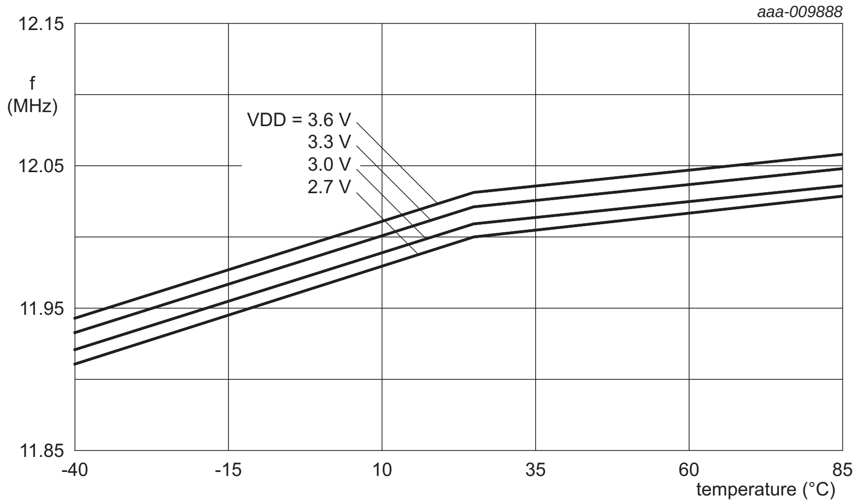
Table 13. Dynamic characteristic: IRC

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 17. Internal IRC frequency vs. temperature

Table 14. Dynamic characteristics: WDOsc and LFOsc

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ± 40 %.

[3] See the *EM783 user manual*.

10.6 I/O pins

Table 15. Dynamic characteristic: digital I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; load capacitor = 30 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output					
		SSO = 1	[2][3]	2.5	-	5.0	ns
		SSO = 6	[2][3]	2.5	-	4.5	ns
		SSO = 16	[2][4]	3.0	-	5.0	ns
t_f	fall time	pin configured as output	[2][3]				
		SSO = 1		2.0	-	4.5	ns
		SSO = 6	[2][3]	2.0	-	4.5	ns
		SSO = 16	[2][4]	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin. Simulated results.

[2] SSO indicates maximum number of simultaneously switching digital output pins. The pins are optimized for half of the maximum SSO.

[3] Set SLEW bit in the IOCONFIG register to 1.

[4] Set SLEW bit in the IOCONFIG register to 0.

10.7 I²C-bus

Remark: All I²C modes (Standard-mode, Fast-mode, Fast-mode Plus) can be configured for the true open-drain pins P0_2 and P0_3. If the limited-performance I²C-bus pins are used (I²C-bus functions on standard I/O pins), only Standard-mode with internal pull-up enabled or Fast-mode with external pull-up resistor are supported.

Table 16. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs

Table 16. Dynamic characteristic: I²C-bus pins[1] *...continued*

T_{amb} = –40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must provide an internal hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal). The hold time is to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ can be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL. It applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns before the SCL line is released. This is in accordance with the Standard-mode I²C-bus specification. Also the acknowledge timing must meet this set-up time.

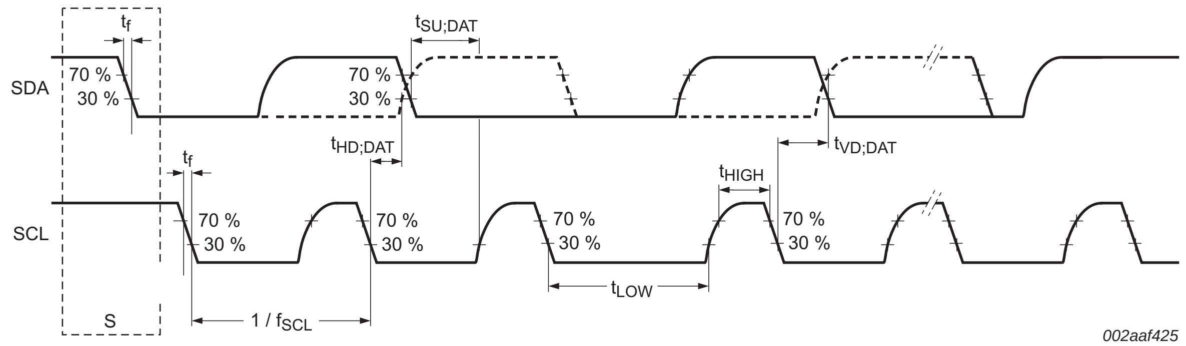


Fig 18. I²C-bus pins clock timing

10.8 SSP interface

Table 17. Dynamic characteristics of SSP pins in SPI mode

2.6 V <= VDD(3V3) = VDD(IO) <= 3.6 V.

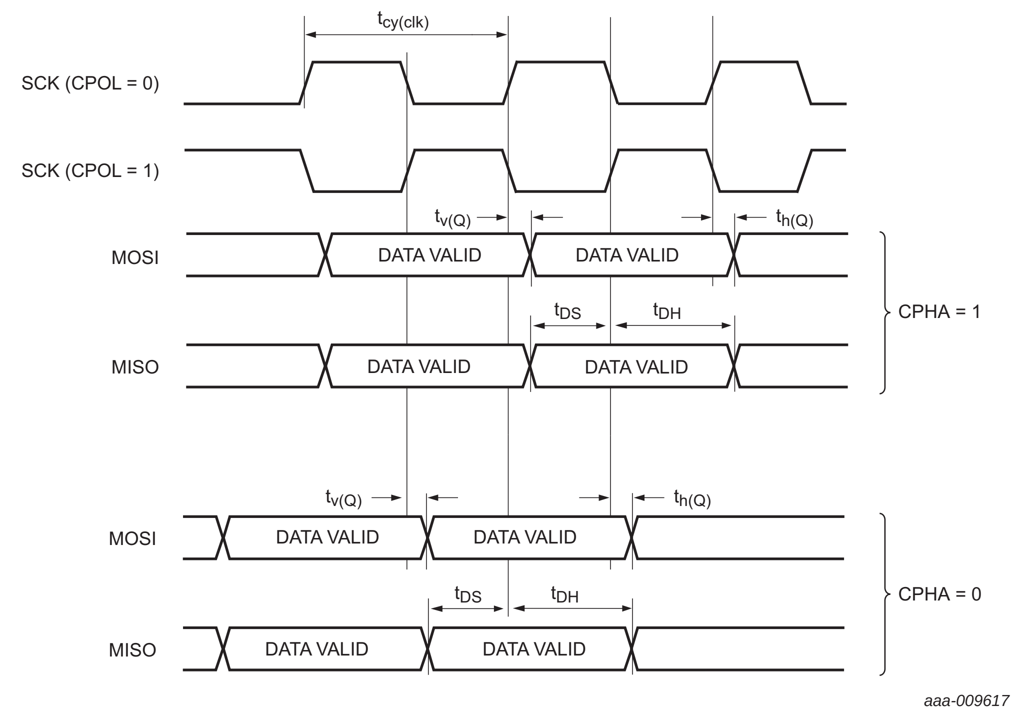
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master (in SPI mode)							
$t_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40	-	-	ns
t_{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SSP slave (in SPI mode)							
$t_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times t_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times t_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times t_{cy(PCLK)} + 5$	ns

[1] $t_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SSP bit rate $t_{cy(clk)}$, is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register) and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{amb} = -40$ °C to +85 °C.

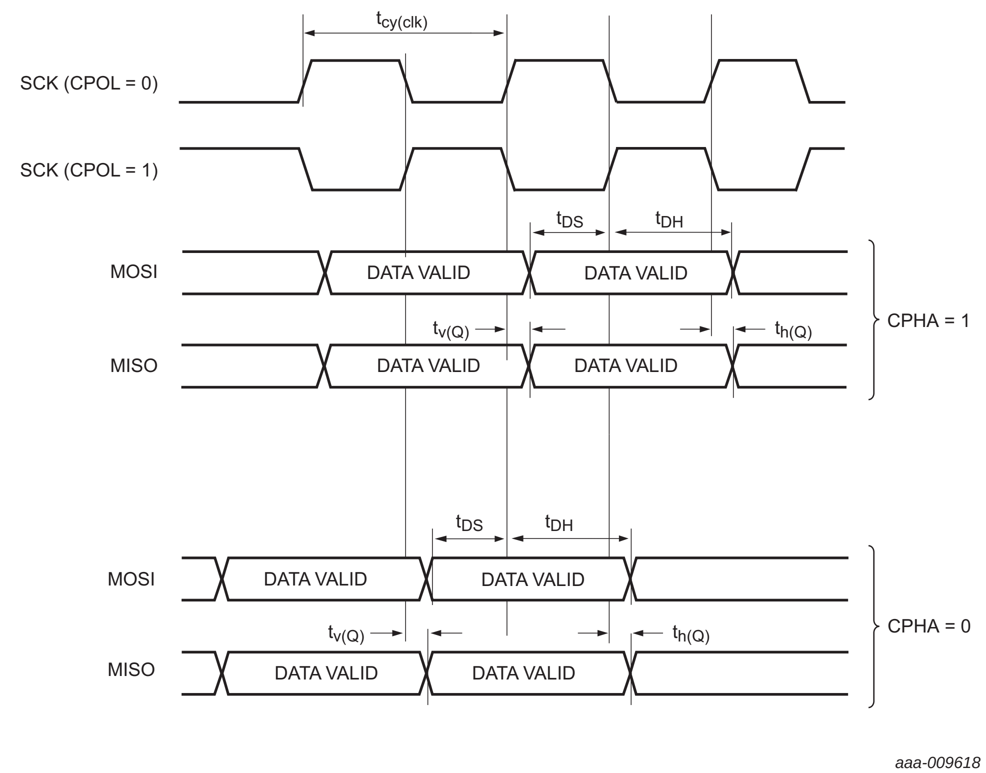
[3] $t_{cy(clk)} = 12 \times t_{cy(PCLK)}$.

[4] $T_{amb} = 25$ °C; for normal voltage supply range: $V_{DD(3V3)} = 3.3$ V.



Pin names SCK, MISO, and MOSI refer to pins for SSP peripheral SSP0.

Fig 19. SSP master timing in SPI mode



Pin names SCK, MISO, and MOSI refer to pins for SSP peripheral SSP0.

Fig 20. SSP slave timing in SPI mode

11. Characteristics of analog peripherals

Table 18. BOD static characteristics[1]

$T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *EM783 User manual*.

Table 19. DAC static and dynamic characteristics

$V_{DD(3V3)}$ = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error			-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity			-	-	±2	LSB
E_O	offset error			-	-	25	mV
E_G	gain error			-	-	25	mV
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
R_O	output resistance		[1]	-	< 40		Ω
$f_{c(DAC)}$	DAC conversion frequency			-	0.4	1	MHz
t_s	settling time			-	-	1	µs
V_O	output voltage	Output voltage range with less than 1 LSB deviation; with minimum R_L connected to ground or power supply		0.3	-	$V_{DD(3V3)}$ − 0.3	V
		with minimum R_L connected to ground or power supply		0.175	-	$V_{DD(3V3)}$ − 0.175	V

[1] Measured on typical samples.

Table 20. DAC sampling frequency range and power consumption

Bias bit	Maximum current	DAC sampling frequency range
0	700 µA	0 MHz to 1 MHz
1	350 µA	0 MHz to 400 kHz

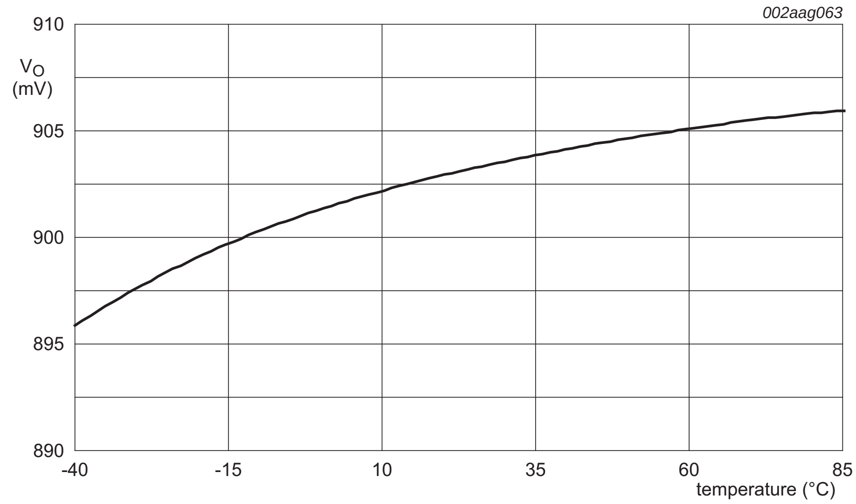
Table 21. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +85 °C	[1]	0.855	0.900	0.945	V
		T_{amb} = 70 °C to +85 °C	[2]	-	0.906	-	V
		T_{amb} = 50 °C	[2]	-	0.905	-	V
		T_{amb} = 25 °C	[3]	0.893	0.903	0.913	V
		T_{amb} = 0 °C	[2]	-	0.902	-	V
		T_{amb} = −20 °C	[2]	-	0.899	-	V
		T_{amb} = −40 °C	[2]	-	0.896	-	V
$t_{s(pu)}$	power-up settling time	up to 90 % of V_O	[3]	-	144	195	µs

[1] Characterized through simulation.

[2] Characterized on a typical silicon sample.

[3] Measured over process variations.



$V_{DD(3V3)}$ = 3.3 V

Fig 21. Typical internal voltage reference output voltage

12. Application information

12.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If a clock in slave mode drives the oscillator, it is recommended that the input is coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

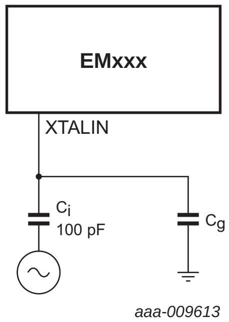


Fig 22. Slave mode operation of the on-chip oscillator

In slave mode, the input clock signal should be coupled using a capacitor of 100 pF (Figure 22), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 23 and in Table 22 and Table 23. Since the feedback resistance is integrated on chip, for fundamental mode oscillation, only connect a crystal and the capacitances C_{X1} and C_{X2} externally. L, C_L and R_S define the fundamental frequency. Capacitance C_P in Figure 23 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 22).

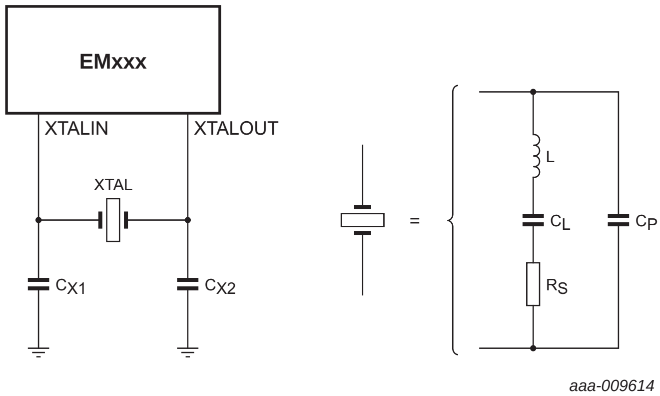


Fig 23. Oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 22. Recommended values for C_{X1}/C_{X2} in oscillation mode (low frequency mode)

Fundamental oscillation frequency F_{OSC}	XTAL load capacitance C_L	Max. XTAL series resistance R_S	External load capacitors	
			C_{X1}	C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF	18 pF
	20 pF	< 300 Ω	39 pF	39 pF
	30 pF	< 300 Ω	57 pF	57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF	18 pF
	20 pF	< 200 Ω	39 pF	39 pF
	30 pF	< 100 Ω	57 pF	57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF	18 pF
	20 pF	< 60 Ω	39 pF	39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF	18 pF

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (high frequency mode)

Fundamental oscillation frequency F_{OSC}	XTAL load capacitance C_L	Max. XTAL series resistance R_S	External load capacitors	
			C_{X1}	C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF	18 pF
	20 pF	< 100 Ω	39 pF	39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF	18 pF
	20 pF	< 80 Ω	39 pF	39 pF

12.2 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. To keep the noise coupled in via the PCB as small as possible, loops must be made as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen to accommodate the increase in parasitics of the PCB layout.

12.3 Standard I/O pad configuration

Figure 24 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on 17 pins
- Analog input

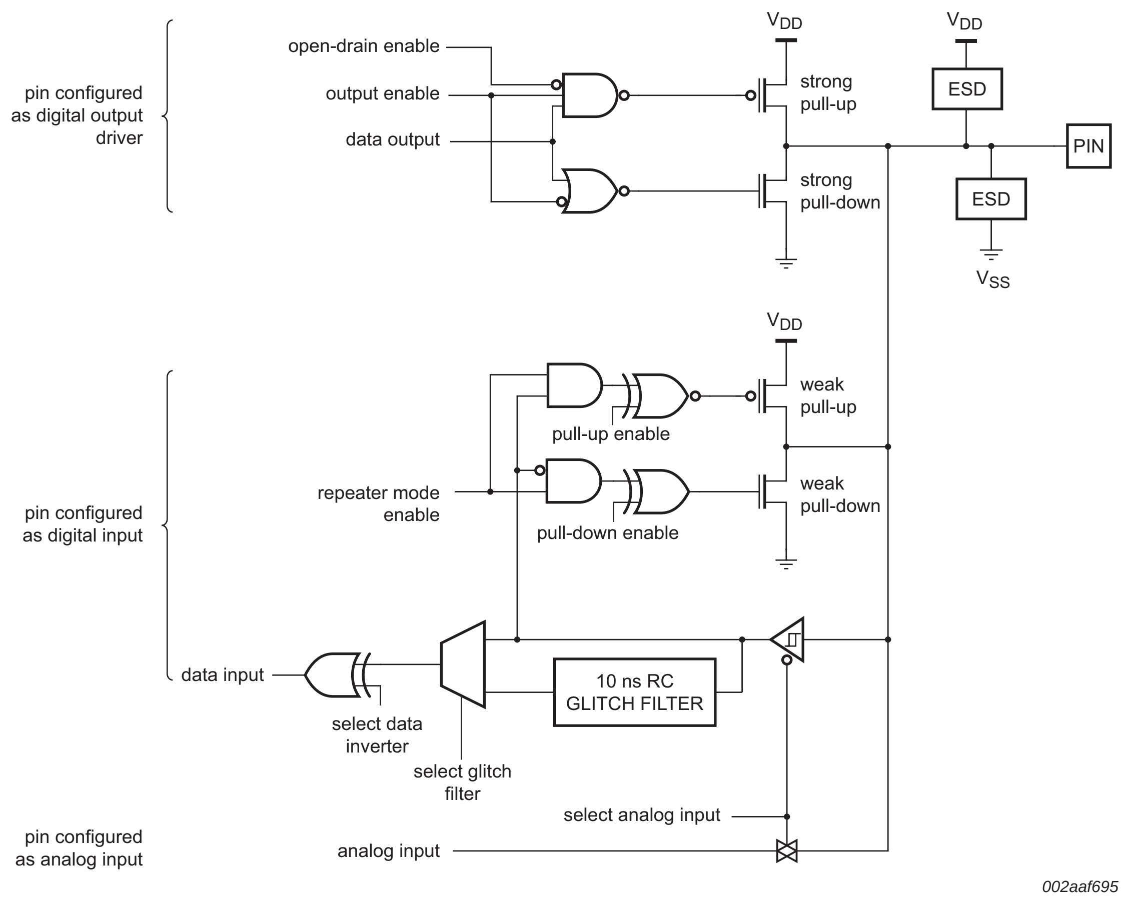
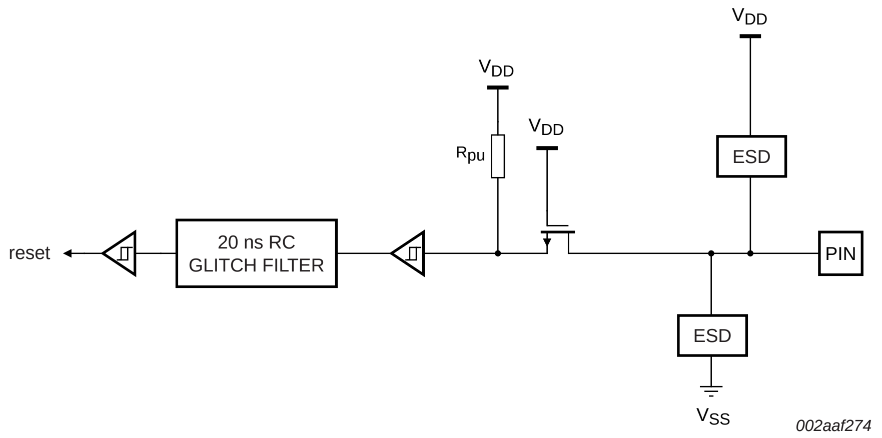


Fig 24. Standard I/O pad configuration

12.4 Reset pad configuration



Remark: The internal pull-up R_{pu} is disconnected in Deep-power down mode. To prevent the $\overline{\text{RESET}}$ pin from floating in Deep power-down mode, an external pull-up resistor should be added.

Fig 25. Reset pad configuration

12.5 UVLO protection and reset timer circuit

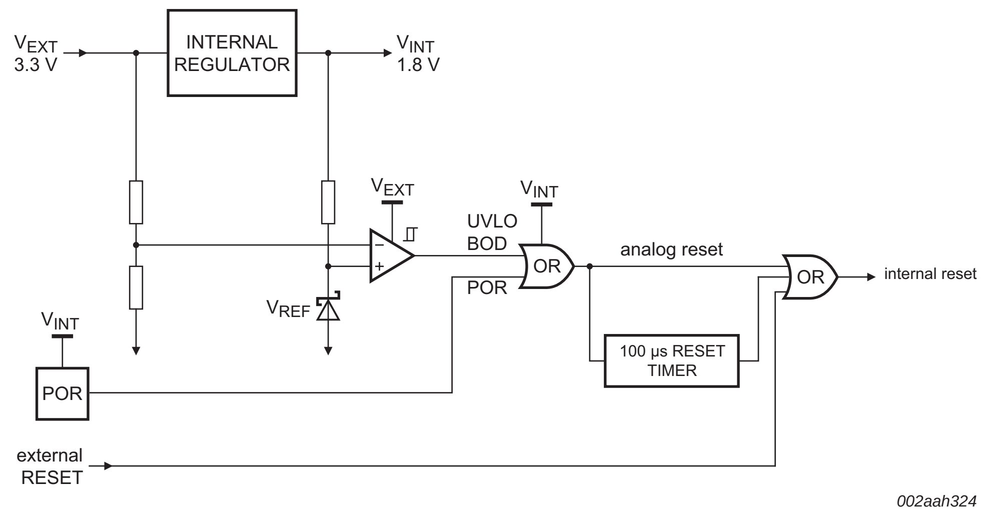


Fig 26. Functional diagram of the UVLO protection and reset timer circuit

12.6 Guidelines for selecting a power supply filter for UVLO protection

For the UVLO circuits to hold the part in reset during shallow and deep brownout conditions, the power supply line must be filtered to allow the BOD and POR circuits to settle when short voltage drops occur (see Section 10.1 "Power supply fluctuations").

Select the capacitance of the decoupling/bypass capacitor in accordance with the following guidelines.

$C >> I_{DD} \times t_s / \Delta V_{DD(3V3)}$ with:

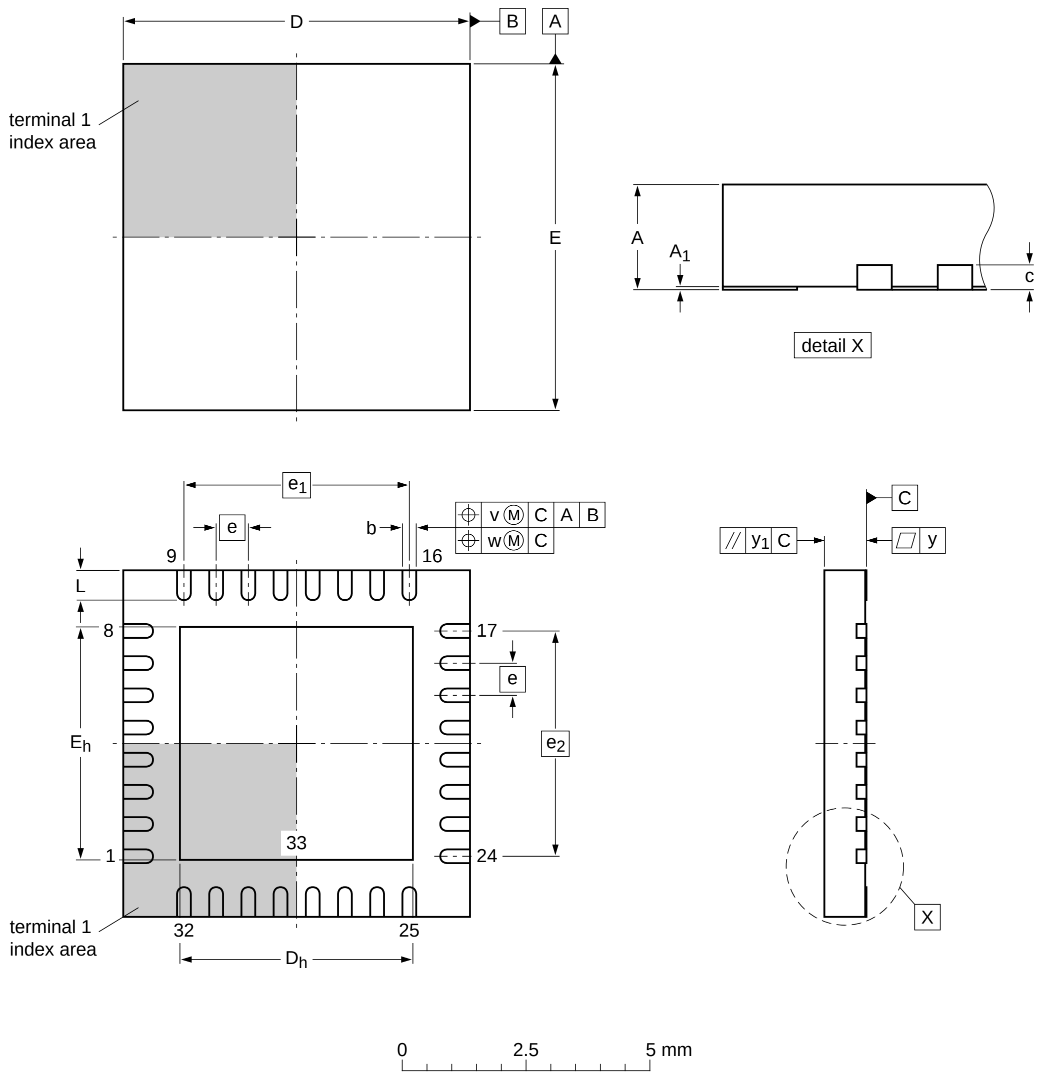
- $\Delta V_{DD(3V3)} \approx 100$ mV for a voltage drop below the BOD and POR trip points.
- $I_{DD} \approx 3$ mA with the IRC running and PLL/SysOsc off (see Figure 6).
- $t_s = 5$ µs for shallow brownout (see Table 8).
- $t_s = 12$ µs for deep brownout (see Table 8).

With these parameters, the value of the decoupling/bypass capacitor to be added to the supply line is:

- C = 0.15 µF for shallow brownout.
- C = 0.36 µF for deep brownout.

13. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
			- - -			~~09-03-17~~ 09-03-23

Fig 27. Package outline HVQFN33

14. Soldering

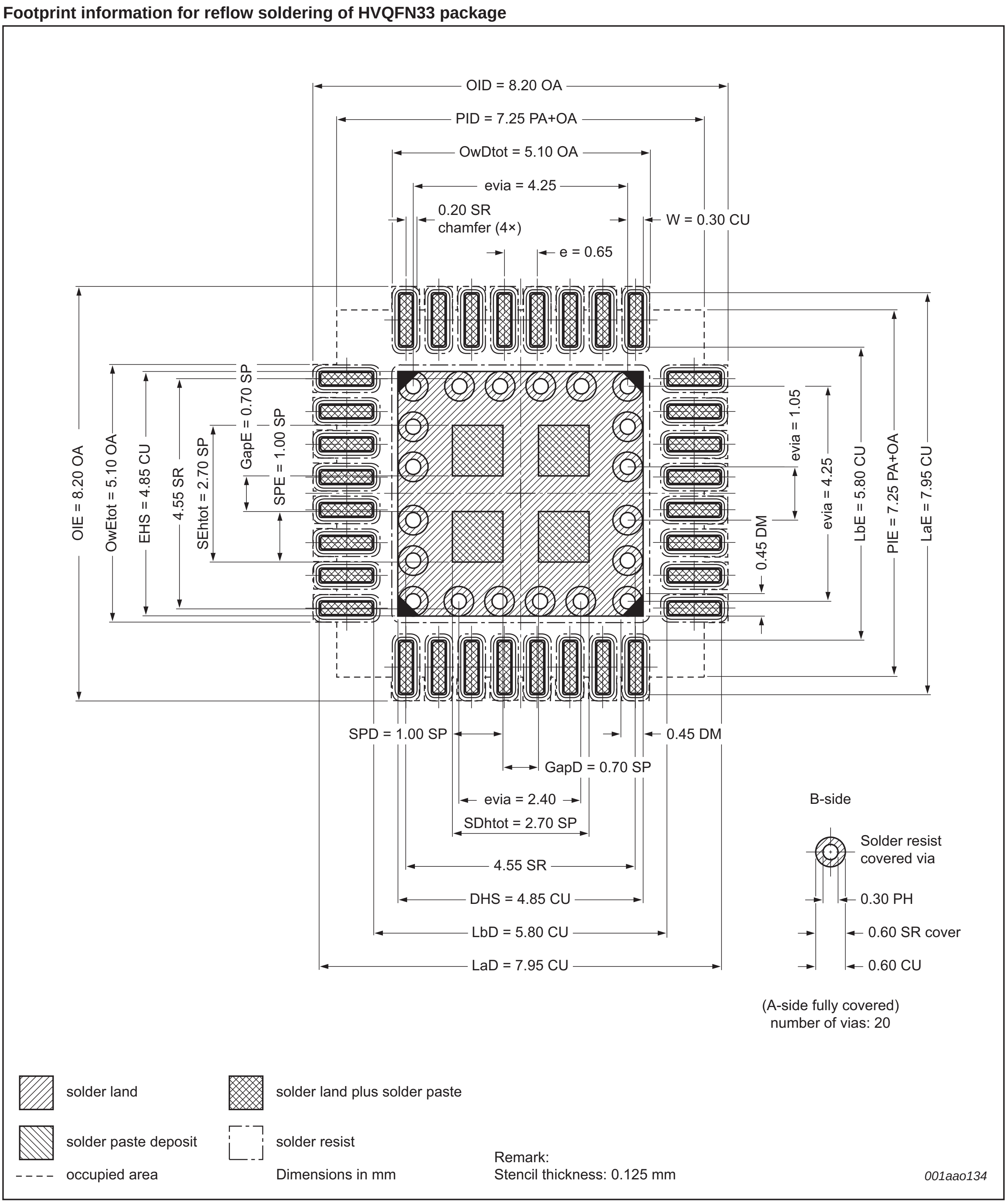


Fig 28. Reflow soldering of the HVQFN33(7x7) package

15. Abbreviations

Table 24. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
JEDEC	Joint Electron Devices Engineering Council
NVM	Non-Volatile Memory
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
UVLO	Under-Voltage Lockout

16. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
EM783 v.2	20140117	Product data sheet	-	EM783 v.1
EM783 v.1	20131108	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 17 January 2014

Document identifier: EM783