NTMD4102PR2

Product Preview

Trench Power MOSFET

-20 V, P-Channel, SO-8 Dual

This P-Channel device was designed using ON Semiconductor's leading edge trench technology for low $R_{DS(on)}$ performance in the SO-8 dual package for high power and current handling capability. The low $R_{DS(on)}$ performance is particularly suited for game systems, notebook and desktop computers, and printers.

Features & Benefits

- Leading -20 V Trench for Low $R_{DS(on)}$
- SO-8 Package Provides Excellent Thermal Performance
- Surface Mount SO-8 Package Saves Board Space
- Pb Free Package for Green Manufacturing

Applications

- Load/Power Management
- Battery Switching for Multi Cell Li-Ion
- Buck-Boost Synchronous Rectification

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-20	V
Gate-to-Source Voltage	V_{GS}	±20	V
Drain Current - Continuous @ T_A = 25°C (Note 1) - Pulsed Drain Current (t = 10 μs)	 I_D I_{DM}	 -6.5 -30	A
Steady State Power Dissipation @ T_A = 25°C (Note 1)	P_D	1.1	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Continuous Source Current (Body Diode)	I_S	-0.9	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)	T_L	260	°C

THERMAL RESISTANCE RATINGS

Thermal Resistance - Junction-to-Ambient - Steady State (Note 1) - Junction-to-Ambient - t ≤ 10 s (Note 1) - Junction-to-Lead - Steady State (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JL}$	 TBD TBD TBD	°C/W

1. Surface-mounted on FR4 board using 1″ sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq)

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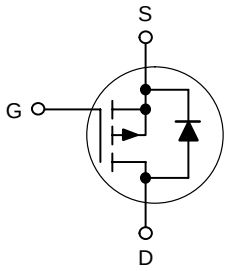
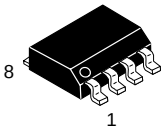
$V_{BR(DSS)}$ = -20 VOLTS
$R_{DS(on)}$ (max) = 19 mΩ @ -10 V
$I_{D(max)}$ (Note 1) = -8.5 A
$R_{DS(on)}$ (max) = 30 mΩ @ -4.5 V
$I_{D(max)}$ (Note 1) = -6.5 A

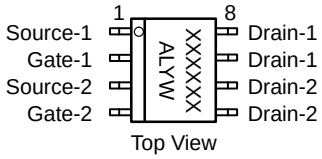
P-Channel MOSFET





SO-8
CASE 751
STYLE 12

MARKING DIAGRAM & PIN ASSIGNMENT



Top View

XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTMD4102PR2	SO-8	2500/Tape & Reel

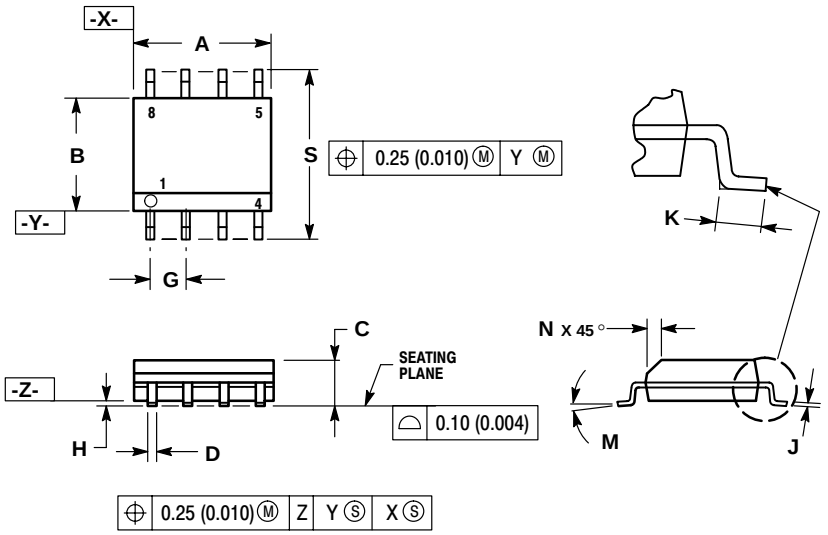
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V_{GS} = 0 V, I_D = 250 μA)		$V_{(BR)DSS}$	-20	-	-	V
Zero Gate Voltage Drain Current (Note 3) (V_{GS} = 0 V, V_{DS} = -16 V)		I_{DSS}	-	-	-1.0	μA
Gate-to-Source Leakage Current (V_{GS} = ±20 V, V_{DS} = 0 V)		I_{GSS}	-	-	±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage (Note 3) (V_{GS} = V_{DS}, I_D = -250 μA)		$V_{GS(th)}$	-1.0	-	-	V
Drain-to-Source On-Resistance (V_{GS} = -10 V, I_D = -8.5 A) (V_{GS} = -4.5 V, I_D = -6.5 A)		$R_{DS(on)}$	 - -	 TBD TBD	 19 30	mΩ
Forward Transconductance (V_{DS} = -10 V, I_D = -8.4 A)		g_{FS}	-	TBD	-	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	(V_{GS} = 0 V, f = 1 MHz, V_{DS} = -10 V)	C_{iss}	-	TBD	-	pF
Output Capacitance		C_{oss}	-	TBD	-	
Reverse Transfer Capacitance		C_{rss}	-	TBD	-	
Total Gate Charge	(V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -8.4 A)	$Q_{G(tot)}$	-	TBD	TBD	nC
Threshold Gate Charge	(V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -8.4 A)	$Q_{G(th)}$	-	TBD	TBD	nC
Gate-to-Source Gate Charge	(V_{DS} = -10 V, I_D = -8.4 A)	Q_{GS}	-	TBD	-	nC
Gate-to-Drain “Miller” Charge	(V_{DS} = -10 V, I_D = -8.4 A)	Q_{GD}	-	TBD	-	nC
Output Charge	(V_{DS} = -10 V, V_{GS} = 0 V)	Q_{OSS}	-	TBD	-	nC
Gate Resistance		R_G	-	TBD	-	Ω
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	(V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -1.0 A, R_G = 6.0 Ω)	$t_{d(on)}$	-	TBD	-	ns
Rise Time		t_r	-	TBD	-	
Turn-Off Delay Time		$t_{d(off)}$	-	TBD	-	
Fall Time		t_f	-	TBD	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	(V_{GS} = 0 V, I_{SD} = -1.7 A)	V_{SD}	-	TBD	TBD	V
Reverse Recovery Time	(V_{GS} = 0 V, V_{DS} = -10 V, dI_{SD}/dt = 100 A/μs, I_{SD} = -1.7 A)	t_{rr}	-	TBD	TBD	ns
Charge Time		t_a	-	TBD	-	ns
Discharge Time		t_b	-	TBD	-	ns
Reverse Recovery Charge		Q_{rr}	-	TBD	-	nC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

PUBLICATION ORDERING INFORMATION

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