64-Position OTP Digital Potentiometer

AD5171

FEATURES

64 positions
OTP (one-time programmable)[1] set-and-forget resistance setting—low cost alternative over EEMEM
Unlimited adjustments prior to OTP activation
5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ end-to-end resistance
Low tempco 5 ppm/°C in potentiometer mode
Low tempco 35 ppm/°C in rheostat mode
Compact standard SOT-23-8 package
Low power, I_{DD} = 8 µA max
Fast settling time, t_s = 5 µs typ in power-up
I²C compatible digital interface
Computer software replaces µc in factory programming applications
Full read/write of wiper register
Extra I²C device address pin
Power-on preset to midscale
6 V one-time programming voltage
Low operating voltage, 2.7 V to 5.5 V
OTP validation check function
Automotive temperature range −40°C to +125°C

APPLICATIONS

Systems calibrations
Electronics level settings
Mechanical potentiometers and trimmers® replacements
Automotive electronics adjustments
Gain control and offset adjustments
Transducer circuits adjustments
Programmable filters up to 1.5 MHz BW

GENERAL DESCRIPTION

The AD5171 is a 64-position, one-time programmable (OTP) digital potentiometer[2], which employs fuse link technology to achieve the memory retention of resistance setting function. OTP is a cost-effective alternative over the EEMEM approach for users who do not need to reprogram new memory setting in the digital potentiometer. This device performs the same electronic adjustment function like most mechanical trimmers and variable resistors do. The AD5171 is programmed using a 2-wire I²C compatible digital control. It allows unlimited adjustments before permanently setting the resistance value. During the OTP activation, a permanent fuse blown command is sent after the final value is determined; therefore freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). When this permanent setting is achieved, the value will not change regardless of supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in read mode.

For applications that program AD5171 in the factories, Analog Devices offers a device programming software, which operates across Windows® 95 to XP® platforms including Windows NT®. This software application effectively replaces the need for external I²C controllers or host processors and therefore significantly reduces users' development time.

An AD5171 evaluation kit is available, which includes the software, connector, and cable that can be converted for the factory programming applications.

The AD5171 is available in a compact SOT-23-8 package. All parts are guaranteed to operate over the automotive temperature range of −40°C to +125°C. Besides its unique OTP feature, the AD5171 lends itself well to other general-purpose digital potentiometer applications due to its temperature performance, small form factor, and low cost.

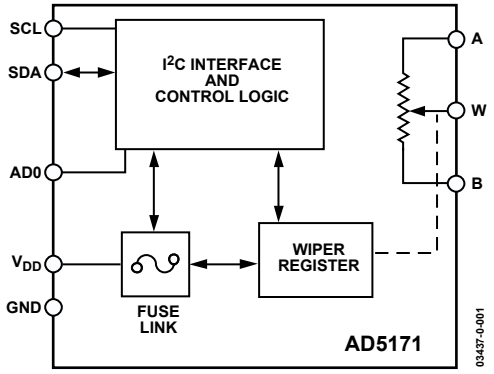

Figure 1. Functional Block Diagram

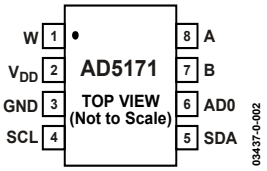

Figure 2. Pin Configuration

[1]One-time programmable (OTP) - Unlimited adjustments before permanent setting.
[2]The terms digital potentiometer and RDAC are used interchangeably.

Rev. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Table 1. 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ versions, V_{DD} = 3 V to 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = No Connect, R_{AB} = 10 kΩ, 50 kΩ, and 100 kΩ	−0.5	±0.2	+0.5	LSB
		R_{WB}, V_A = No Connect, R_{AB} = 5 kΩ	−1	±0.25	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = No Connect, R_{AB} = 10 kΩ, 50 kΩ, and 100 kΩ	−1	±0.25	+1	LSB
		R_{WB}, V_A = No Connect, R_{AB} = 5 kΩ	−1.5	±0.5	+1.5	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$		−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		60	115	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (Specifications apply to all RDACs)						
Resolution	N				6	Bits
Differential Nonlinearity[4]	DNL		−0.5	±0.1	+0.5	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x20		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F	−1.5	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00, R_{AB}=10 kΩ, 50 kΩ, and 100 kΩ	0	0.5	1.5	LSB
		Code = 0x00, R_{AB} = 5 kΩ	0		2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$	With respect to GND			V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, Code = 0x20		25		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x20		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS						
Input Logic High (SDA and SCL)	V_{IH}		0.7 V_{DD}		V_{DD}+0.5	V
Input Logic Low (SDA and SCL)	V_{IL}		−0.5		0.3V_{DD}	V
Input Logic High (AD0)	V_{IH}	V_{DD} = 3 V	3.0		V_{DD}	V
Input Logic Low (AD0)	V_{IL}	V_{DD} = 3 V	0		1.0	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			3		pF
DIGITAL OUTPUTS						
Output Logic Low (SDA)	V_{OL}	I_{OL} = 6 mA			0.4	V
Three-State Leakage Current (SDA)	I_{OZ}	V_{IN} = 0 V or 5 V			±1	µA
Output Capacitance[6]	C_{OZ}			3		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[7]	V_{DD_OTP}	T_A = 25°C	6		6.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		4	8	µA
OTP Supply Current[8]	I_{DD_OTP}	V_{DD_OTP} = 6 V, T_A = 25°C	100			mA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.02	0.04	mW
Power Supply Sensitivity	PSSR		−0.025	+0.001	+0.025	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS [6, 10, 11]						
Bandwidth –3 dB	BW_5k	R_{AB} = 5 kΩ, Code = 0x20		1500		kHz
	BW_10k	R_{AB} = 10 kΩ, Code = 0x20		600		kHz
	BW_50k	R_{AB} = 50 kΩ, Code = 0x20		110		kHz
	BW_100k	R_{AB} = 100 kΩ, Code = 0x20		60		kHz
Total Harmonic Distortion	THD	V_A =1 V rms, R_{AB} = 10 kΩ, V_B = 0 V D_C, f = 1 kHz		0.05		%
Adjustment Settling Time	t_{S1}	V_A= 5 V ± 1 LSB error band, V_B = 0, measured at V_W		5		µs
OTP Settling Time[12]	t_{S_OTP}	V_A = 5 V ± 1 LSB error band, V_B = 0, measured at V_W		400		ms
Power-up Settling Time—Post Fuses Blown	t_{S2}	V_A = 5 V ±1 LSB error band, V_B = 0, measured at V_W		5		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 5 kΩ, f = 1 kHz, Code = 0x20		8		nV/√Hz
		R_{AB} = 10 kΩ, f = 1 kHz, Code = 0x20		12		nV/√Hz
INTERFACE TIMING CHARACTERISTICS (Applies to all parts[6,12])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between Start and Stop	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL signals	t_9				0.3	µs
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs

[1]Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3]V_{AB} = V_{DD}, Wiper (V_W) = No connect.
[4]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5]Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6]Guaranteed by design and not subject to production test.
[7]Different from operating power supply, power supply for OTP is used one-time only.
[8]Different from operating current, supply current for OTP lasts approximately 400 ms for one-time needed only.
[9]P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[10]Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value result in the minimum overall power consumption.
[11]All dynamic characteristics use V_{DD} = 5 V.
[12]Different from settling time after fuse is blown. The OTP settling time occurs once only.

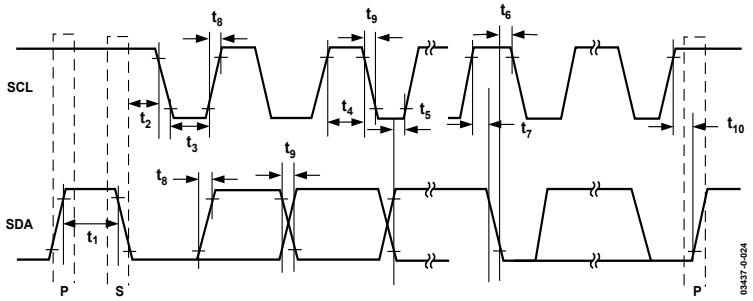

Figure 3. Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	–0.3, +7 V
V_A, V_B, V_W to GND	GND, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A open)[1]	±5 mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B open)[1]	±5 mA
Digital Inputs and Output Voltage to GND	0 V, V_{DD}
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance[2] θ_{JA}	230°C/W

[1]Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V_{DD} = 5 V.
[2]Package Power Dissipation = (T_J max – T_A) / θ_{JA}

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

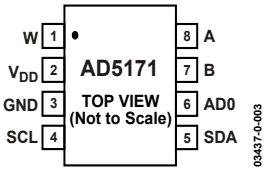

Figure 4. SOT-23-8

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W. GND ≤ V_W ≤ V_{DD}.
2	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 6 V and 100 mA driving capability.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires pull-up resistor.
5	SDA	Serial Data Input/Output. Requires pull-up resistor.
6	AD0	I^2C Device Address Bit. Allows maximum of two AD5171s to be addressed.
7	B	Resistor Terminal B. GND ≤ V_B ≤ V_{DD}.
8	A	Resistor Terminal A. GND ≤ V_A ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

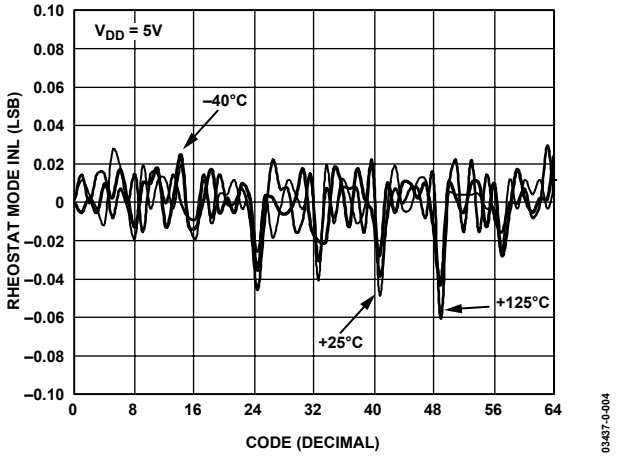

Figure 5. R-INL vs. Code vs. Temperature

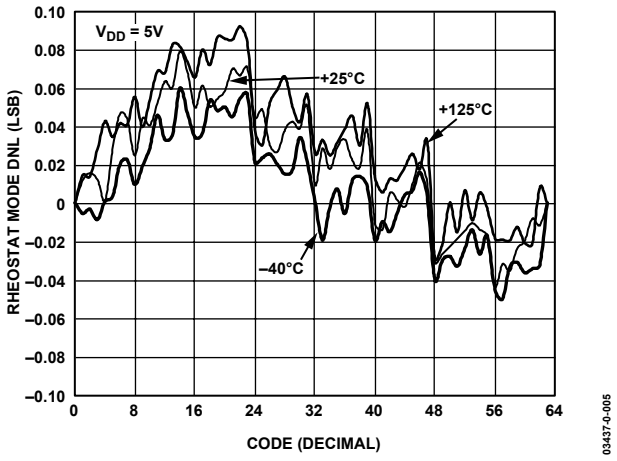

Figure 6. R-DNL vs. Code vs. Temperature

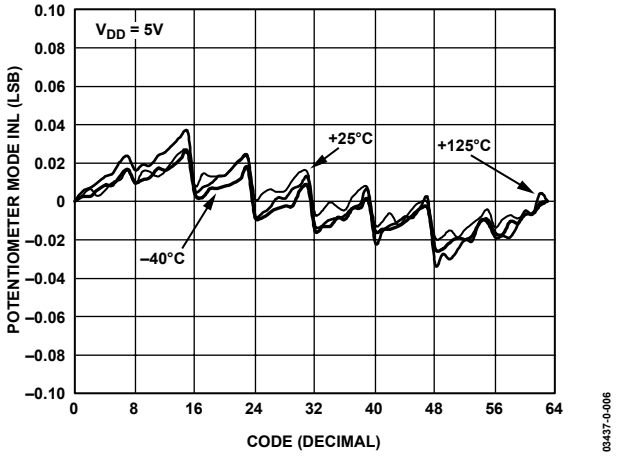

Figure 7. INL vs. Code vs. Temperature

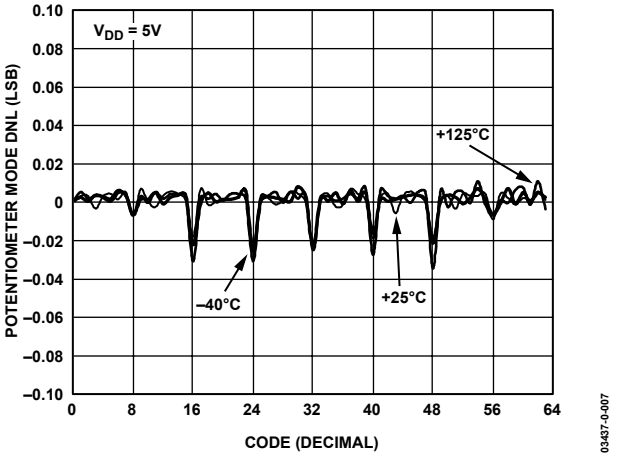

Figure 8. DNL vs. Code vs. Temperature

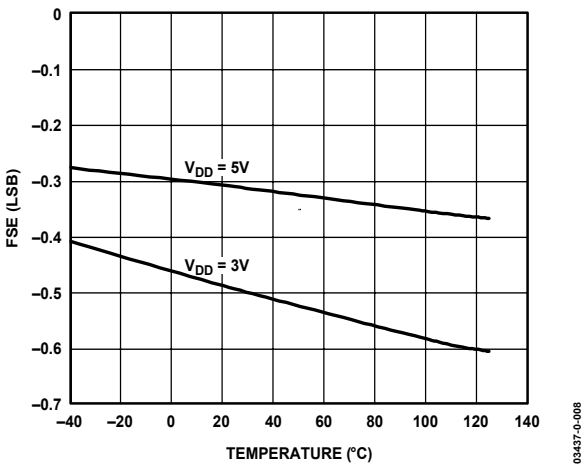

Figure 9. Full-Scale Error

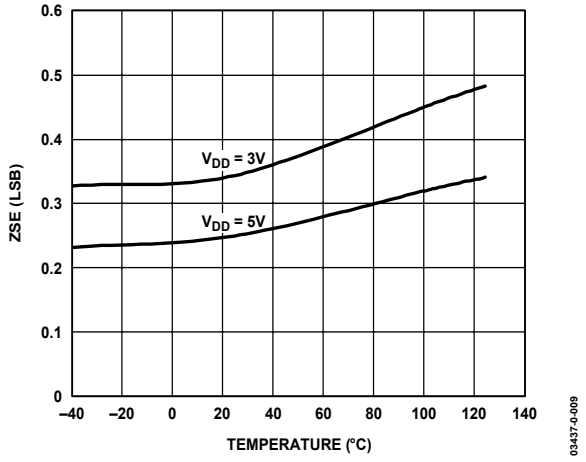

Figure 10. Zero-Scale Error

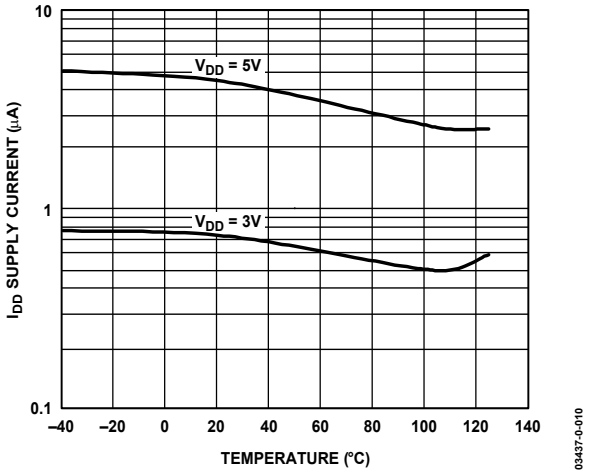

Figure 11. Supply Current vs. Temperature

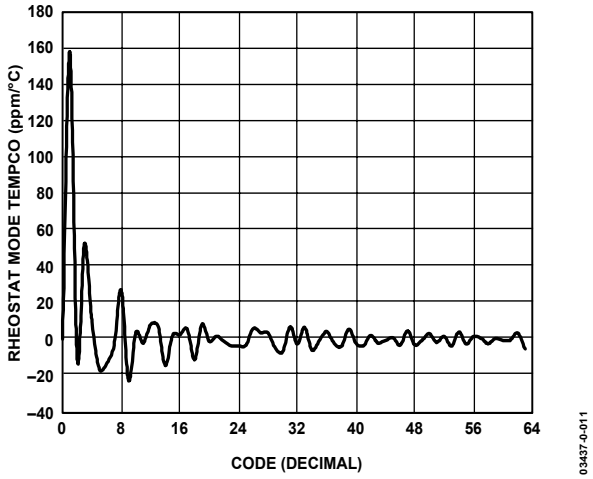

Figure 12. Rheostat Mode Tempco ($\Delta R_{AB}/R_{AB}$)/ ΔT vs. Code

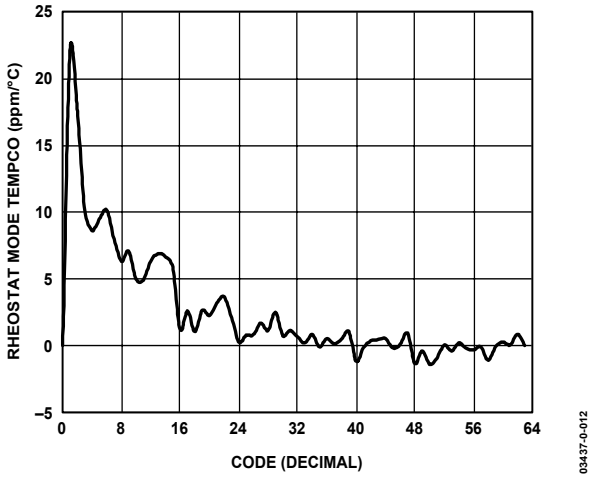

Figure 13. Potentiometer Mode Tempco ($\Delta V_W/V_W$)/ ΔT vs. Code

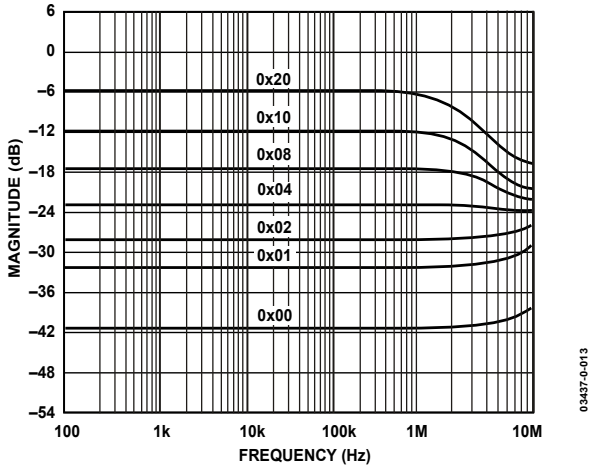

Figure 14. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

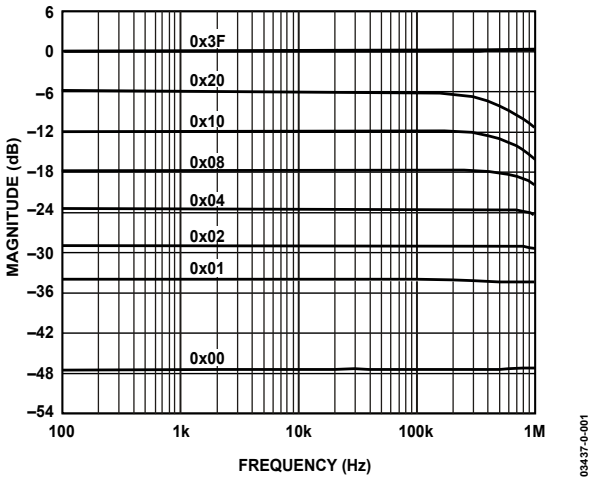

Figure 15. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

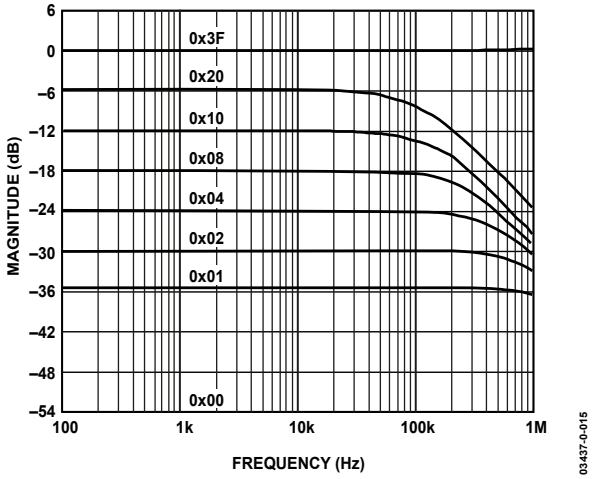

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 50 Ω

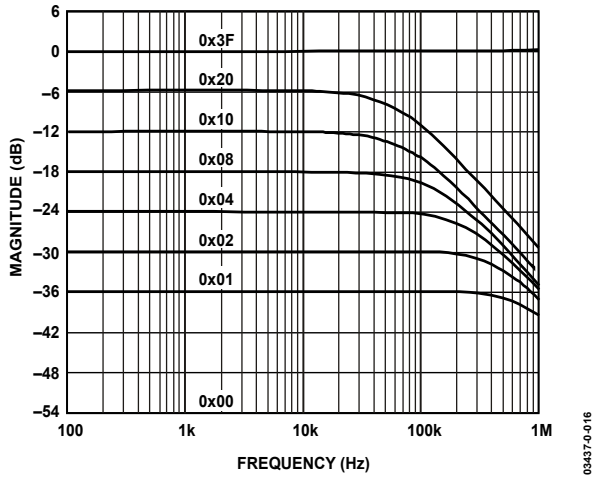

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

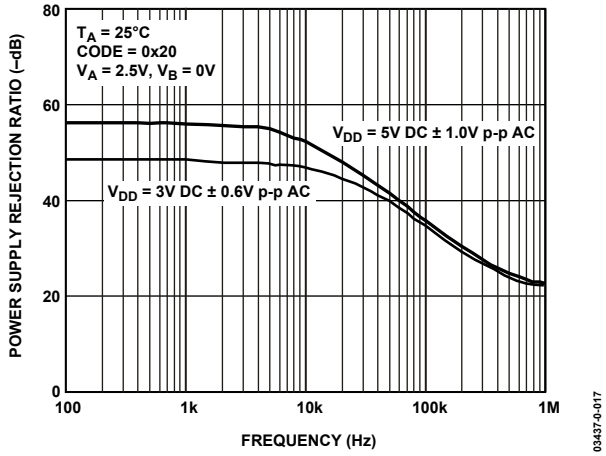

Figure 18. PSRR vs. Frequency

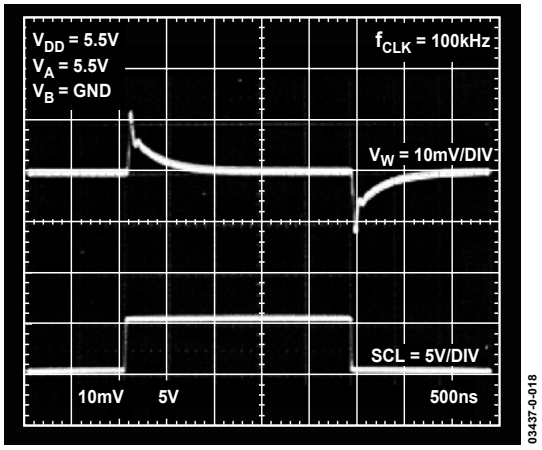

Figure 19. Digital Feedthrough vs. Time

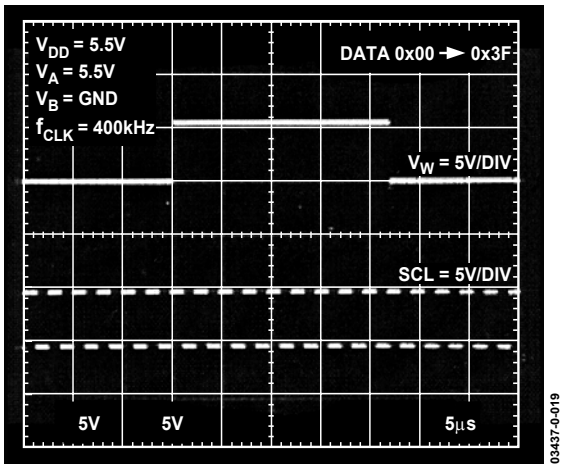

Figure 20. Settling Time

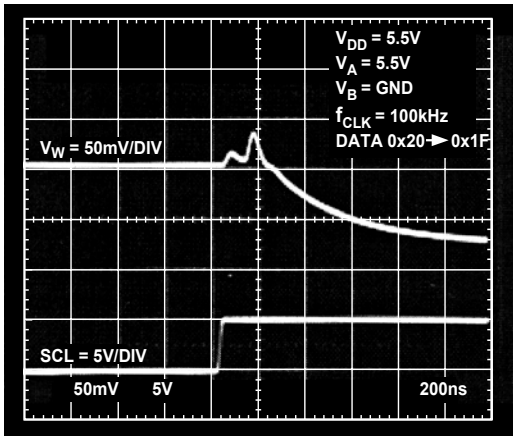

Figure 21. Midscale Glitch Energy

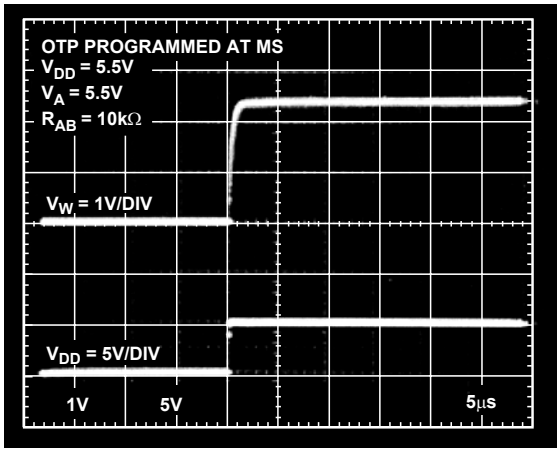

Figure 22. Power-Up Settling Time, after Fuses Blown

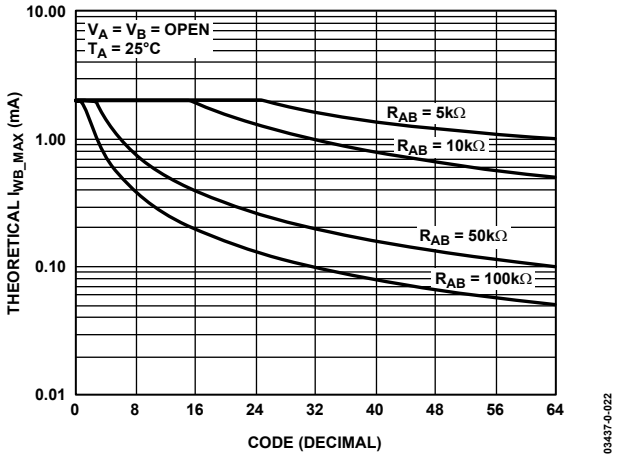

Figure 23. I_{WB}_max vs. Code

THEORY OF OPERATION

The AD5171 allows unlimited 6-bit adjustments, except for one-time programmable, set-and-forget resistance setting. OTP technology is a proven cost-effective alternative over EEMEM in one-time memory programming applications. AD5171 employs fuse link technology to achieve the memory retention of the resistance setting function. It comprises six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are blown.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5171 presets to midscale during power on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit to high along with the proper coding (Table 7).

The device control circuit has two validation bits, E1 and E0, that can be read back in the read mode for checking the programming status as shown in Table 4.

Table 4. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully. (For factory setup checking purpose only. Users should not see these combinations.)
1	0	Error. Some fuses are not blown. Try again.
1	1	Successful. No further programming is possible.

When the OTP T bit is set, the internal clock is enabled. The program will attempt to blow a test fuse. The operation stops if this fuse is not blown properly. The validation Bits E1 and E0 show 01, and the users should check the setup. If the test fuse is blown successfully, the data fuses will be programmed next. The six data fuses will be programmed in six clock cycles. The output of the fuses is compared with the code stored in the DAC register. If they do not match, E1 and E0 = 10 is issued as a error and the operation stops. Users may retry with the same codes. If the output and stored code match, the programming lock fuse will be blown so that no further programming is possible. In the meantime, E1 and E0 will issue 11 indicating the lock fuse is blown successfully. All the fuse latches are enabled at power-on and therefore the output corresponds to the stored setting from this point on. Figure 24 shows a detailed functional block diagram.

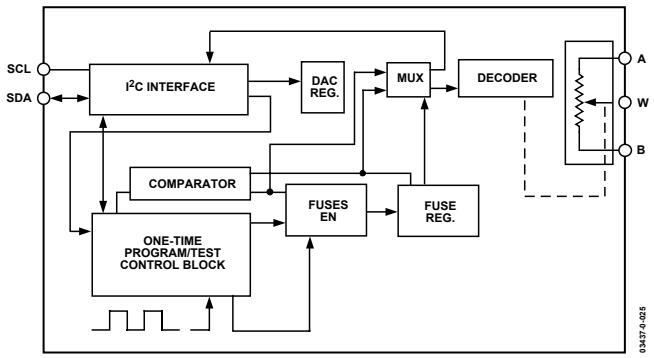

Figure 24. Detailed Functional Block Diagram

DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE

Rheostat Mode Operation

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with W. This operation is called rheostat mode (Figure 25).

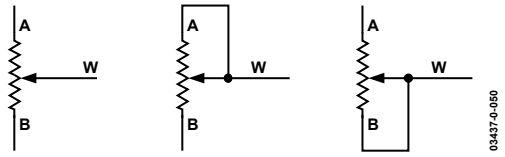

Figure 25. Rheostat Mode Configuration

The nominal resistance (R_{AB}) of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is considered. The 6-bit data in the RDAC latch is decoded to select one of the 64 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Such connection yields a minimum of 60 Ω resistance between terminals W and B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω ($R_{WB} = (1) \times R_{AB}/63 + R_W$) for data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω ($(63) \times R_{AB}/63 + R_W$). Figure 26 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the 6-bit binary code.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Table 5. R_{WB} vs. Codes; R_{AB} = 10 kΩ and the A Terminal Is Opened

D (Dec)	R_{WB} (Ω)	Output State
63	10060	Full-Scale ($R_{AB} + R_W$)
32	5139	Midscale
1	219	1 LSB
0	60	Zero-Scale (Wiper Contact Resistance)

Since a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened or shorted to W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \quad (2)$$

Table 6. R_{WA} vs. Codes; R_{AB} =10 kΩ and B Terminal Is Opened

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full-Scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero-Scale

The typical distribution of the resistance tolerance from device to device is process lot dependent, and it is possible to have ±30% tolerance.

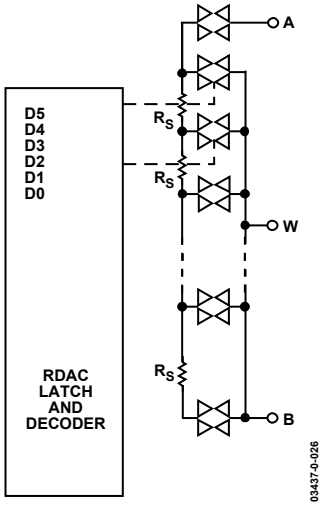

Figure 26. AD5171 Equivalent RDAC Circuit

Potentiometer Mode Operation

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (Figure 27).

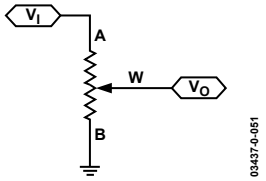

Figure 27. Potentiometer Mode Configuration

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{63} V_A \quad (3)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\frac{D}{63} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (4)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of D/63 with a relatively small error contributed by the R_W terms, and therefore the tolerance effect is almost cancelled. Although the thin film step resistor R_S and CMOS switches resistance R_W have very different temperature coefficients, the ratio-metric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode operations include others such as op amp input, feedback resistor networks, and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (Figure 28).

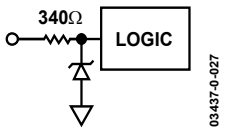

Figure 28. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals. The V_{DD} of AD5171 therefore defines their voltage boundary conditions, see Figure 29. Supply signals present on terminals A, B, and W that exceed V_{DD} will be clamped by the internal forward-biased diodes and should be avoided.

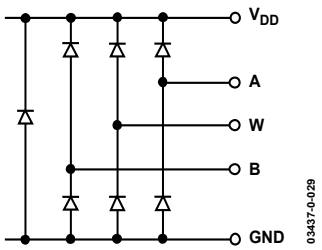

Figure 29. Maximum Terminal Voltages Set by V_{DD}

POWER-UP/POWER-DOWN SEQUENCES

Similarly, because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuits. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltages are applied to the same V_{DD} terminal of the AD5171. The AD5171 employs fuse link technology that requires 6 V to blow the internal fuses to achieve a given setting. On the other hand, it operates at 2.7 V to 5.5 V once the programming is complete. Such dual voltage requires isolation between supplies. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 6 V and be able to handle 400 ms and 100 mA of transient current for one-time programming. Once programming is complete, the 6 V supply must be removed to allow normal operation of 2.7 V to 5.5 V. Figure 30 shows the simplest implementation using a jumper. This approach saves one voltage supply, but draws additional current and requires manual configuration.

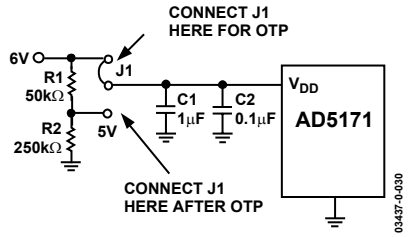

Figure 30. Power Supply Requirement

An alternate approach in 3.5 V to 5.5 V systems adds a signal diode between the system supply and the OPT supply for isolation, as shown in Figure 31.

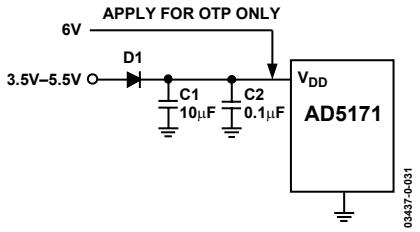

Figure 31. Isolating the 6 V OPT Supply from the 3.5V to 5.5 V Normal Operating Supply. The 6 V supply must be removed once OPT is complete.

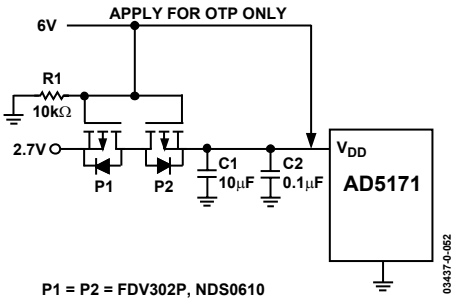

Figure 32. Isolating the 6 V OPT Supply from the 2.7 V Normal Operating Supply. The 6 V supply must be removed once OPT is complete.

For users who operate their systems at 2.7 V, it is recommended to use the bi-directional low-threshold P-Ch MOSFETs for the supplies isolation. As shown in Figure 32 assumes the 2.7 V system voltage is applied first but not the 6 V. The gates of P1 are P2 are pulled to ground, which turns on P1 and subsequently P2. As a result, V_{DD} of AD5171 becomes 2.7 V minus a few tenths of mV drop across P1 and P2. When the AD5171 setting is found, the factory tester applies the 6 V to V_{DD} and also to the gates of P1 and P2 to turn them off. While the OTP command is executing at this time to program AD5171, the 2.7 V source is therefore protected. Once the OTP is complete, the tester withdraws the 6 V, and AD5171 setting is permanently fixed.

CONTROLLING THE AD5171

There are two ways of controlling the AD5171. Users can either program the devices with computer software or external I²C controllers.

Software Programming

Due to the advantage of the one-time programmable feature, users may consider programming the device in the factory before shipping to end users. ADI offers a device programming software, which can be implemented in the factory on PCs that run Windows 95 to XP platforms. As a result, external controllers are not required, which significantly reduces development time. The program is an executable file that does not require any programming languages or user programming skills. It is easy to set up and use. Figure 33 shows the software interface. The software can be downloaded from www.analog.com.

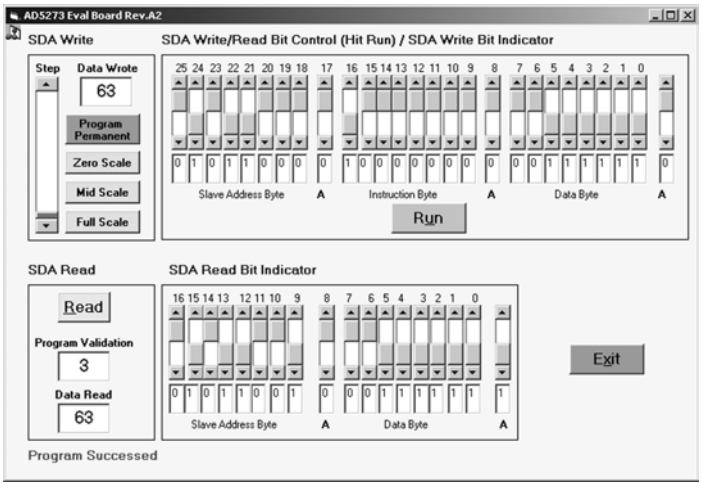

Figure 33. AD5171 Computer Software Interface

Write

The AD5171 starts at midscale after power-up prior to the OPT programming. To increment or decrement the resistance, the user may simply move the scrollbar on the left. To write any specific values, the user should use the bit pattern control in the upper screen and press the Run button. The format of writing data to the device is shown in Table 7. Once the desirable setting is found, the user may press the Program Permanent button to blow the internal fuse links for permanent setting. The user may also set the programming bit pattern in the upper screen and press the Run button to achieve the same result.

Read

To read the validation bits and data out from the device, the user may simply press the Read button. The user may also set the bit pattern in the upper screen and press the Run button. The format of reading data out from the device is shown in Table 8.

To apply the device programming software in the factory, users need to modify a parallel port cable and configure Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively for the control signals (Figure 34). Users should also layout the PCB of the AD5171 with SCL and SDA pads, as shown in Figure 35, such that pogo pins can be inserted for the factory programming.

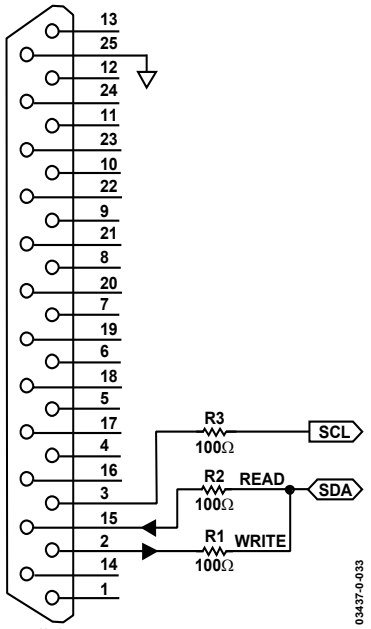

Figure 34. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND

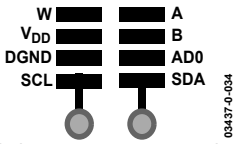

Figure 35. Recommended AD5171 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for programming (Figure 34).

Table 7. SDA Write Mode Bit Format

S	0	1	0	1	1	0	AD0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 8. SDA Read Mode Bit Format

S	0	1	0	1	1	0	AD0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte										

Table 9. SDA Bits Definitions and Descriptions

Bit	Description	Bit	Description
S	Start Condition.	D5, D4, D3, D2, D1, D0	Data Bits.
P	Stop Condition.	E1, E0	OTP Validation Bits.
A	Acknowledge.	0, 0	Ready to Program.
AD0	I²C Device Address Bit. Allows maximum of two AD5171s to be addressed.	0, 1	Test Fuse Not Blown Successfully. (For Factory Setup Checking Purpose Only. Users should not see these combinations).
X	Don't Care.	1, 0	Fatal Error. Try again.
T	OTP Programming Bit. Logic 1 programs wiper position permanently.	1, 1	Programmed Successfully. No further adjustments possible.

I²C Controller Programming

Write Bit Pattern Illustrations

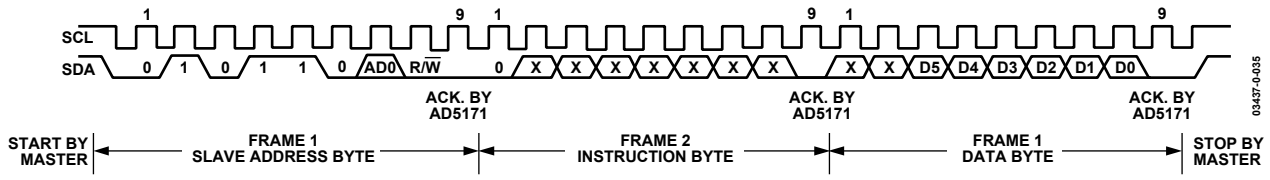

Figure 36. Writing to the RDAC Register

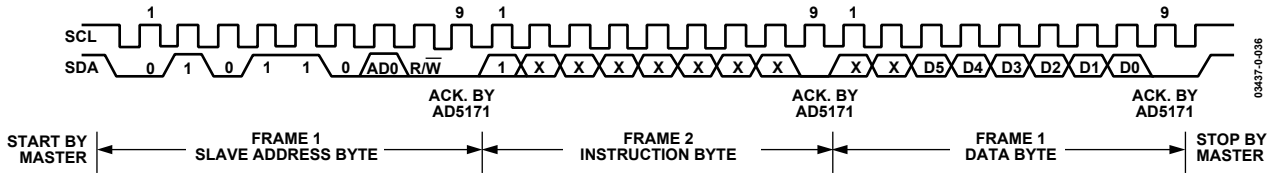

Figure 37. Activating One-Time Programming

Read Bit Pattern Illustration

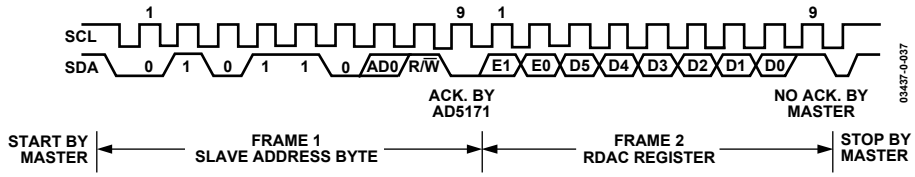

Figure 38. Reading Data from RDAC Register

For users who prefer to use external controllers, the AD5171 can be controlled via an I²C compatible serial bus and is connected to this bus as slave device. Referring to Figure 36, Figure 37, and Figure 38, the 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when SDA from high-to-low while SCL is high (Figure 36 and Figure 37). The following byte is the slave address byte, which consists of the 6 MSBs as a slave address defined as 010110. The next bit is AD0, which is an I²C device address bit. Depending on the states of their AD0 bits, two AD5171 can be addressed on the same bus (Figure 39). The last LSB is the R/$\overline{W}$ bit, which determines whether data will be read from or written to the slave device.

The slave whose address corresponds to the transmitted address responds by pulling the SDA line goes low during the 9th clock pulse (this is termed the Acknowledge bit). At

this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. The write operation contains one more instruction byte than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the one-time programming bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (Figure 36).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference with the write mode; there are eight data bits followed by a No Acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (Figure 38).

4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In the write mode, the master will pull the SDA line high during the 10th clock pulse to establish a stop condition (Figure 36 and Figure 37). In the read mode, the master will issue a No Acknowledge for the 9th clock pulse, i.e., the SDA line remains high. The master will then bring the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (Figure 38).

A repeated write function gives the user flexibility to update the RDAC output a number of times, except after permanent programming, addressing, and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the write mode has to be started with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

CONTROLLING TWO DEVICES ON ONE BUS

Figure 39 shows two AD5171 devices on the same serial bus. Each has a different slave address since the state of each AD0 pin is different. This allows each device to be operated independently. The master device output bus line drivers are open-drain pull-downs in a fully I^{2}C compatible interface.

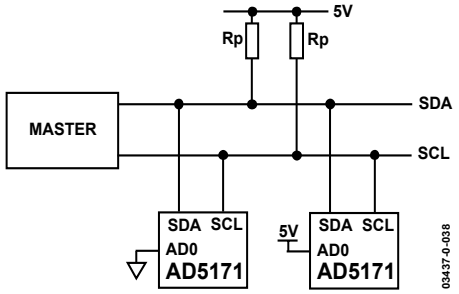

Figure 39. Two AD5171 Devices on One Bus

APPLICATIONS

PROGRAMMABLE VOLTAGE REFERENCE (DAC)

It is common to buffer the output of the digital potentiometer as a DAC unless the load is much larger than R_{WB}. The buffer serves the purpose of impedance conversion as well as delivering higher current, which may be needed.

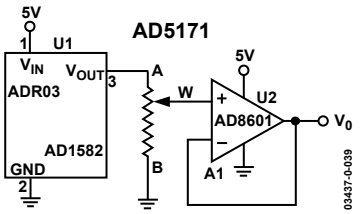

Figure 40. Programmable Voltage Reference (DAC)

GAIN CONTROL COMPENSATION

The digital potentiometers are commonly used in gain controls (Figure 41) or sensor transimpedance amplifier signal conditioning applications. To avoid gain peaking or in worst-case oscillation due to step response, a compensation capacitor is needed. In general, C2 in the range of a few picofarads to no more than a few tenths of a picofarad is adequate for the compensation.

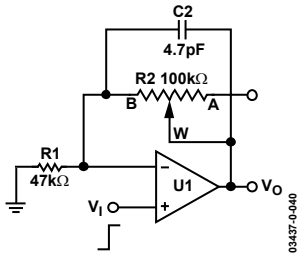

Figure 41. Typical Noninverting Gain Amplifier

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (Figure 42).

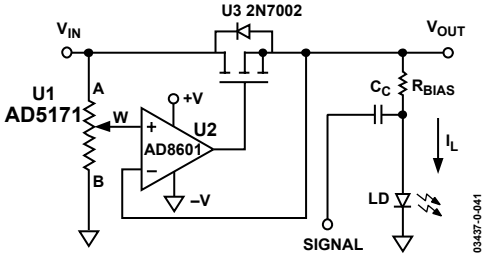

Figure 42. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N_1. N_1 power handling must be adequate to dissipate $(V_I - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at the A terminal of the digital potentiometer.

LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION

When users need to interface a 2.5 V controller with AD5171, a proper voltage level shift must be employed so that the digital potentiometer can be read from or written to the controller; Figure 43 shows one of the implementations. M1 and M2 should be low threshold N-Ch power MOSFETs, such as FDV301N.

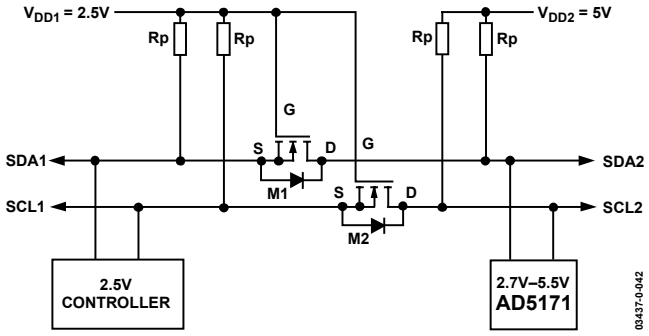

Figure 43. Level Shifting for Different Voltage Operation

RESISTANCE SCALING

The AD5171 offers 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ nominal resistances. For users who need to optimize the resolution with an arbitrary full-range resistance, the following techniques can be used. By paralleling a discrete resistor (Figure 44) a proportion tely lower voltage appears at terminal A to B, which is applicable to only the voltage divider mode.

This translates into a finer degree of precision because the step size at terminal W will be smaller. The voltage can be found as

$$V_W(D) = \frac{(R_{AB} \,||\, R2)}{R3 + R_{AB} \,||\, R2} \times \frac{D}{64} \times V_{DD} \quad (5)$$

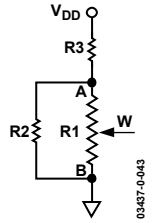

Figure 44. Lowering the Nominal Resistance

For log taper adjustment, such as volume control, Figure 45 shows another way of resistance scaling to achieve the log taper function. In this circuit, the smaller the R2 with respect to R_{AB}, the more like the pseudo log taper characteristic it behaves. The wiper voltage is simply

$$V_W(D) = \frac{(R_{WB} \,||\, R2)}{R_{WA} + R_{WB} \,||\, R2} \times V_I \quad (6)$$

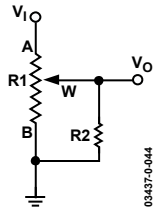

Figure 45. Resistor Scaling with Log Adjustment Characteristics

RESOLUTION ENHANCEMENT

The resolution can be doubled in the potentiometer mode of operation by using three digital potentiometers. Borrowed from ADI's patented RDAC segmentation technique, users can configure three AD5171 (Figure 46) to double the resolution. First, U_3 must be parallel with a discrete resistor R_P, which is chosen to be equal to a step resistance ($R_P = R_{AB}/64$). One can see that adjusting U1 and U2 together forms the coarse 6-bit adjustment and that adjusting U3 alone forms the finer 6-bit adjustment. As a result, the effective resolution becomes 12-bit.

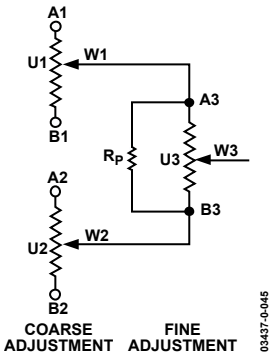

Figure 46. Doubling the Resolution

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5171 (5 kΩ resistor) measures 1.5 MHz at half scale. Figure 14 to Figure 17 provide the large signal BODE plot characteristics of the four available resistor versions 5 kΩ 10 kΩ, 50 kΩ, and 100 kΩ. A parasitic simulation model is shown in Figure 47. Listing 1 provides a macro model net list for the 10 kΩ device.

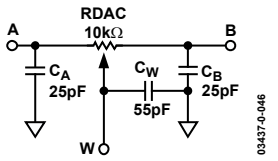

Figure 47. Circuit Simulation Model for RDAC = 10 kΩ

Listing 1. Macro Model Net List for RDAC

```
.PARAM D=64, RDAC=10E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A       0       25E-12
RWA     A       W       {(1-D/64)*RDAC+60}
CW      W       0       55E-12
RWB     W       B       {D/64*RDAC+60}
CB      B       0       25E-12
*
.ENDS DPOT
```

AD5171 EVALUATION BOARD

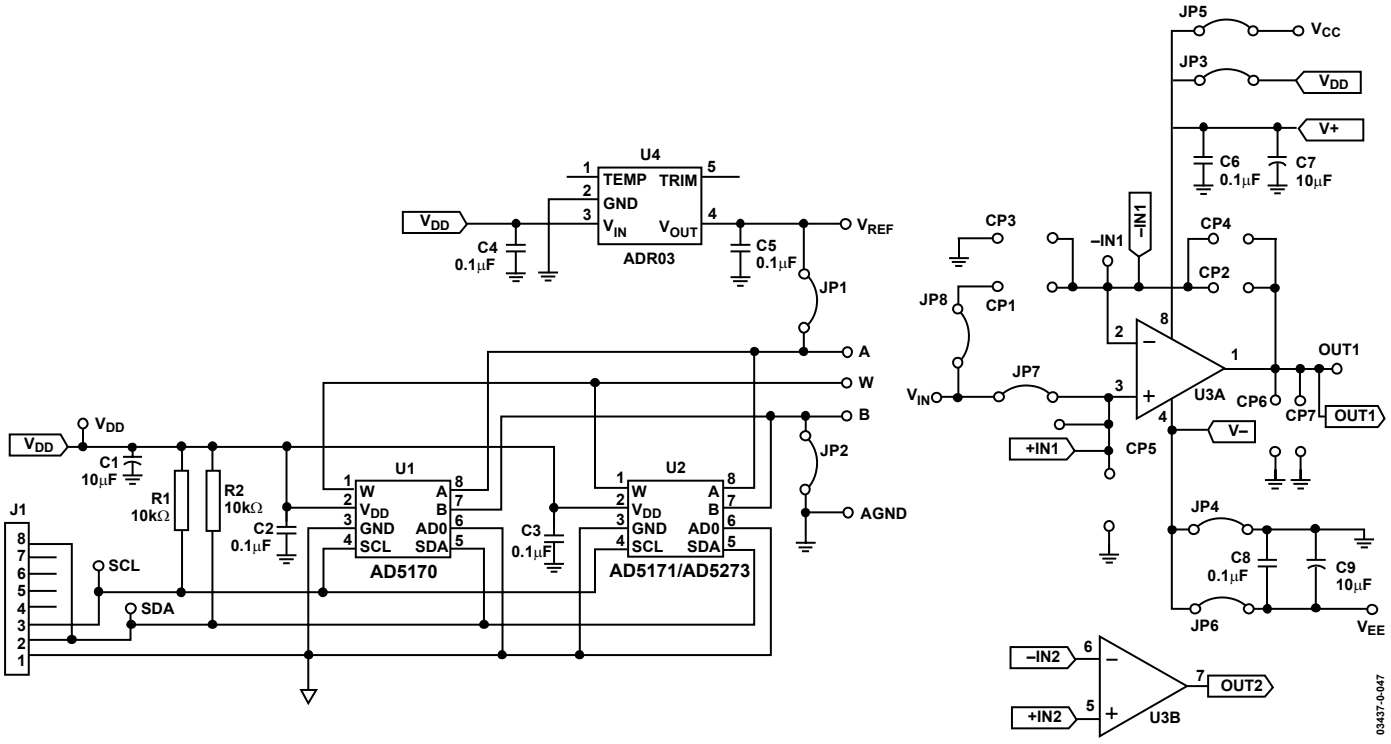

Figure 48. AD5171 Evaluation Board Schematic

The AD5171 evaluation board comes with a dual op amp AD822 and a 2.5 V reference ADR03. Users can configure many other building block circuits with minimum components needed. Figure 49 shows one of the examples. There is space available on the board that users can build additional circuits for further evaluations, see Figure 50.

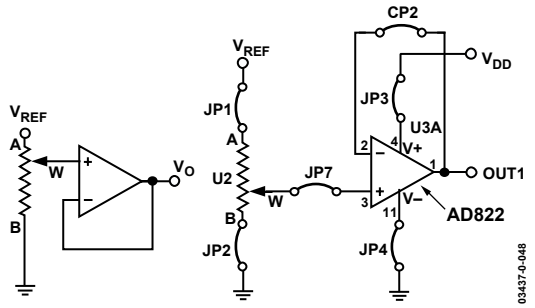

Figure 49. Programmable Voltage Reference

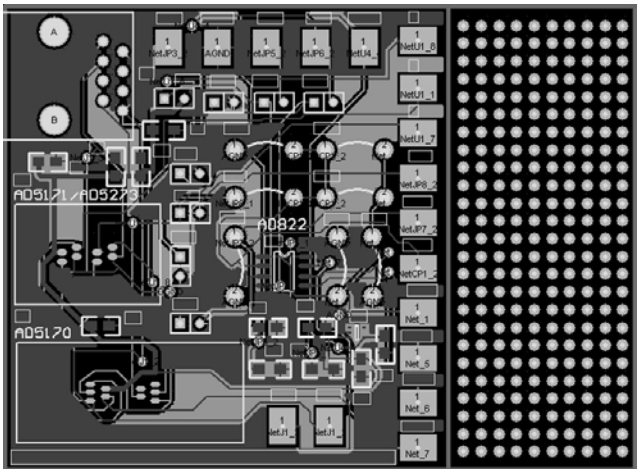

Figure 50. AD5171 Evaluation Board

OUTLINE DIMENSIONS

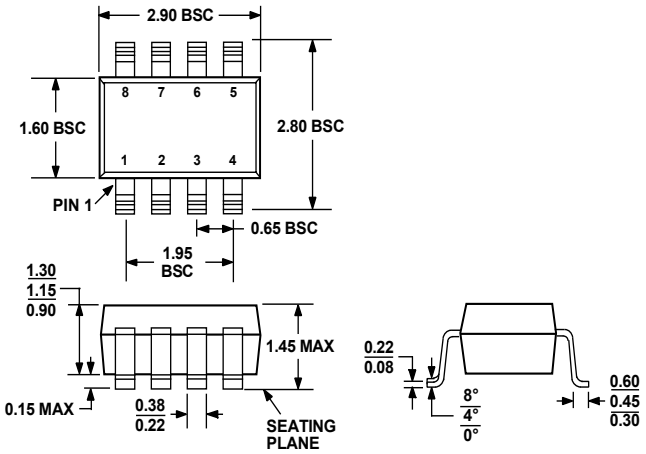

Figure 51. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Package Code	Package Description	Full Container Quantity	Branding
AD5171BRJ5-RL7	5	RJ-8	SOT-23-8	3000	D12
AD5171BRJ10-RL7	10	RJ-8	SOT-23-8	3000	D13
AD5171BRJ50-RL7	50	RJ-8	SOT-23-8	3000	D14
AD5171BRJ100-REEL7	100	RJ-8	SOT-23-8	3000	D15
AD5171BRJ5-R2	5	RJ-8	SOT-23-8	3000	D12
AD5171BRJ10-R2	10	RJ-8	SOT-23-8	3000	D13
AD5171BRJ50-R2	50	RJ-8	SOT-23-8	3000	D14
AD5171BRJ100-R2	100	RJ-8	SOT-23-8	3000	D15
AD5171EVAL*	10			1	

* The evaluation board is shipped with three pieces of 10 kΩ parts. Users should order extra samples or different resistance options if needed.

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

C03437-0-9/03(PrC)