Dual Current Output 12-/14-/16-Bit SoftSpan DACs with Parallel I/O

FEATURES

- **Six Programmable Output Ranges**
  Unipolar: 0V to 5V, 0V to 10V
  Bipolar: ±5V, ±10V, ±2.5V, –2.5V to 7.5V
- **Maximum 16-Bit INL Error: ±1 LSB over Temperature**
- **Low 1µA (Maximum) Supply Current**
- **Guaranteed Monotonic over Temperature**
- **Low Glitch Impulse 1nV•s**
- 2.7V to 5.5V Single Supply Operation
- 2µs Settling Time to ±1 LSB
- Parallel Interface with Readback of All Registers
- Asynchronous $\overline{CLR}$ Pin Clears DAC Outputs to 0V in Any Output Range
- Power-On Reset to 0V
- 48-Pin 7mm × 7mm QFN Package

APPLICATIONS

- High Resolution Offset and Gain Adjustment
- Process Control and Industrial Automation
- Automatic Test Equipment
- Data Acquisition Systems

DESCRIPTION

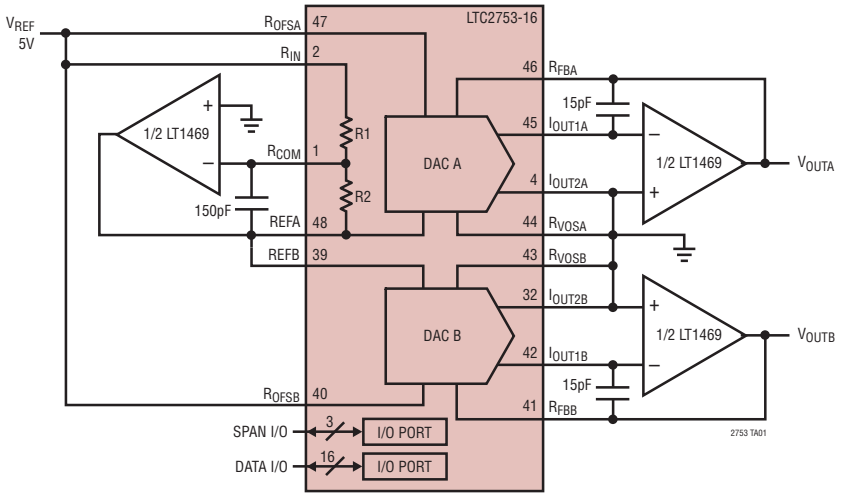
The LTC®2753 is a family of dual 12-, 14-, and 16-bit multiplying parallel-input, current-output DACs. These DACs operate from a single 2.7V to 5.5V supply and are all guaranteed monotonic over temperature. The LTC2753A-16 provides 16-bit performance (±1LSB INL and DNL) over temperature without any adjustments. These SoftSpan™ DACs offer six output ranges—two unipolar and four bipolar—that can be programmed through the parallel interface, or pinstrapped for operation in a single range.

The LTC2753 DACs use a bidirectional input/output parallel interface that allows readback of any on-chip register. A power-on reset circuit resets the DAC outputs to 0V when power is initially applied. A logic low on the $\overline{CLR}$ pin asynchronously clears the DACs to 0V in any output range.

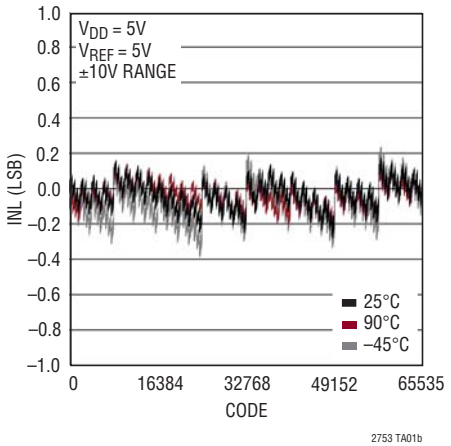
The parts are specified over commercial and industrial temperature ranges.

TYPICAL APPLICATION

Dual 16-Bit V_{OUT} DAC with Software-Selectable Ranges



LTC2753-16 Integral Nonlinearity (INL)

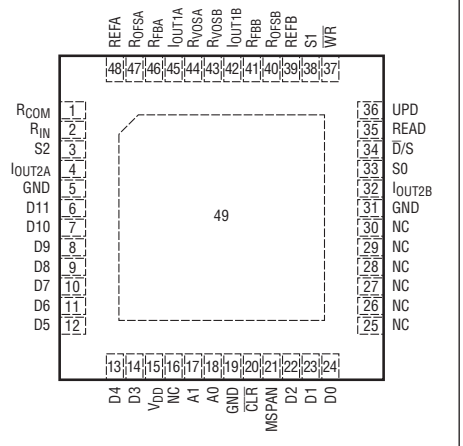


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

I_{OUT1X}, I_{OUT2X}, R_{COM} to GND .....±0.3V
R_{VOSX}, R_{FBX}, R_{OFSX}, R_{IN}, REF_X to GND .....±15V
V_{DD} to GND ..... –0.3V to 7V
Digital Inputs and Digital I/O
to GND .....–0.3V to V_{DD}+0.3V (max 7V)

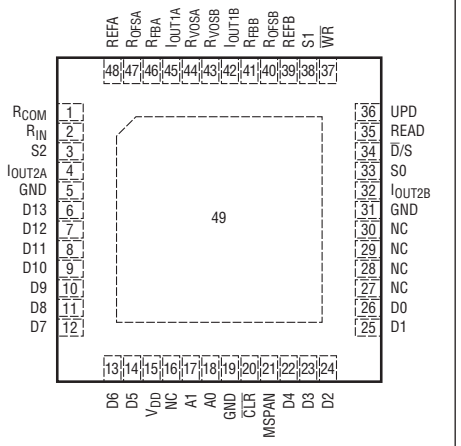
Operating Temperature Range
LTC2753C..... 0°C to 70°C
LTC2753I..... –40°C to 85°C
Maximum Junction Temperature..... 125°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



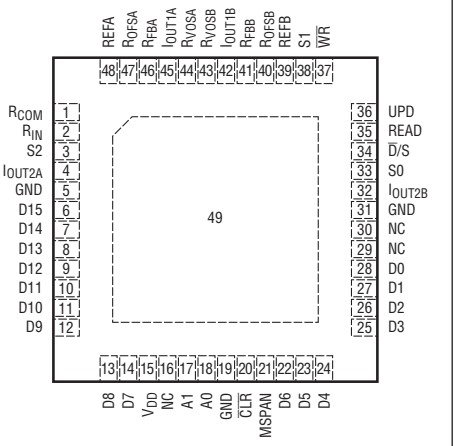
LTC2753-12 UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB



LTC2753-14 UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB



LTC2753-16 UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2753CUK-12#PBF	LTC2753CUK-12#TRPBF	LTC2753UK-12	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2753IUK-12#PBF	LTC2753IUK-12#TRPBF	LTC2753UK-12	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2753CUK-14#PBF	LTC2753CUK-14#TRPBF	LTC2753UK-14	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2753IUK-14#PBF	LTC2753IUK-14#TRPBF	LTC2753UK-14	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2753BCUK-16#PBF	LTC2753BCUK-16#TRPBF	LTC2753UK-16	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2753BIUK-16#PBF	LTC2753BIUK-16#TRPBF	LTC2753UK-16	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2753ACUK-16#PBF	LTC2753ACUK-16#TRPBF	LTC2753UK-16	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2753AIUK-16#PBF	LTC2753AIUK-16#TRPBF	LTC2753UK-16	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC2753-12 MIN	LTC2753-12 TYP	LTC2753-12 MAX	LTC2753-14 MIN	LTC2753-14 TYP	LTC2753-14 MAX	LTC2753B-16 MIN	LTC2753B-16 TYP	LTC2753B-16 MAX	LTC2753A-16 MIN	LTC2753A-16 TYP	LTC2753A-16 MAX	UNITS
Static Performance																
	Resolution		●	12			14			16			16			Bits
	Monotonicity		●	12			14			16			16			Bits
DNL	Differential Nonlinearity		●			±1			±1			±1		±0.2	±1	LSB
INL	Integral Nonlinearity		●			±1			±1			±2		±0.4	±1	LSB
GE	Gain Error	All Output Ranges	●		±0.5	±2		±1.5	±5			±20		±4	±14	LSB
GE_{TC}	Gain Error Temperature Coefficient	ΔGain/ΔTemp			±0.6			±0.6			±0.6			±0.6		ppm/°C
BZE	Bipolar Zero Error	All Bipolar Ranges	●		±0.2	±1		±0.6	±3			±12		±2	±8	LSB
BZS_{TC}	Bipolar Zero Temperature Coefficient				±0.5			±0.5			±0.5			±0.5		ppm/°C
PSR	Power Supply Rejection	V_{DD} = 5V, ±10% V_{DD} = 3V, ±10%	● ●			±0.025 ±0.06			±0.1 ±0.25			±0.4 ±1		±0.03 ±0.1	±0.2 ±0.5	LSB/V
I_{LKG}	I_{OUT1} Leakage Current	T_A = 25°C T_{MIN} to T_{MAX}	 ●		±0.05	±2 ±5		±0.05	±2 ±5		±0.05	±2 ±5		±0.05	±2 ±5	nA
C_{IOUT1}	Output Capacitance	Full-Scale Zero Scale			75 45			75 45			75 45			75 45		pF pF

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resistances (Note 3)							
R1, R2	Reference Inverting Resistors	(Note 4)	●	16	20		kΩ
R_{REF}	DAC Input Resistance		●	8	10		kΩ
R_{FB}	Feedback Resistor	(Note 3)	●	8	10		kΩ
R_{OFS}	Bipolar Offset Resistor	(Note 3)	●	16	20		kΩ
R_{VOS}	Offset Adjust Resistor		●	800	1000		kΩ
Dynamic Performance							
	Output Settling Time	0V to 10V Range, 10V Step. To ±0.0015% FS (Note 5)			2		µs
	Glitch Impulse	(Note 6)			1		nV•s
	Digital-to-Analog Glitch Impulse	(Note 7)			1		nV•s
	Multiplying Feedthrough Error	0V to 10V Range, V_{REF} = ±10V, 10kHz Sine Wave			0.5		mV
THD	Total Harmonic Distortion	(Note 8) Multiplying			–110		dB
	Output Noise Voltage Density	(Note 9) at I_{OUT1}			13		nV/√Hz

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	2.7		5.5	V
I_{DD}	Supply Current, V_{DD}	Digital Inputs = 0V or V_{DD}	●		0.5	1	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage	3.3V ≤ V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} < 3.3V	● ●	2.4 2			V V
V_{IL}	Digital Input Low Voltage	4.5V < V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} ≤ 4.5V	● ●			0.8 0.6	V V
I_{IN}	Digital Input Current	V_{IN} = GND to V_{DD}	●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 10)	●			6	pF
Digital Outputs							
V_{OH}	I_{OH} = 200µA		●	V_{DD} – 0.4			V
V_{OL}	I_{OL} = 200µA		●			0.4	V

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
Write and Update Timing							
t_1	I/O Valid to $\overline{WR}$ Rising Edge Set-Up		●	7			ns
t_2	I/O Valid to $\overline{WR}$ Rising Edge Hold		●	7			ns
t_3	$\overline{WR}$ Pulse Width Low		●	15			ns
t_4	UPD Pulse Width High		●	15			ns
t_5	UPD Falling Edge to $\overline{WR}$ Falling Edge	No Data Shoot-Through	●	0			ns
t_6	$\overline{WR}$ Rising Edge to UPD Rising Edge	(Note 10)	●	0			ns
t_7	$\overline{D}$/S Valid to $\overline{WR}$ Falling Edge Set-Up Time		●	7			ns
t_8	$\overline{WR}$ Rising Edge to $\overline{D}$/S Valid Hold Time		●	7			ns
t_9	A1-A0 Valid to $\overline{WR}$ Falling Edge Setup Time		●	5			ns
t_{10}	$\overline{WR}$ Rising Edge to A1-A0 Valid Hold Time		●	0			ns
t_{11}	A1-A0 Valid to UPD Rising Edge Setup Time		●	9			ns
t_{12}	UPD Falling Edge to A1-A0 Valid Hold Time		●	7			ns
Readback Timing							
t_{13}	$\overline{WR}$ Rising Edge to READ Rising Edge		●	7			ns
t_{14}	READ Falling Edge to $\overline{WR}$ Falling Edge	(Note 10)	●	20			ns
t_{15}	READ Rising Edge to I/O Propagation Delay	C_L = 10pF	●			40	ns
t_{26}	A1-A0 Valid to READ Rising Edge Setup Time		●	20			ns
t_{27}	READ Falling to A1-A0 Valid Hold Time	(Note 10)	●	0			ns

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{17}	UPD Valid to I/O Propagation Delay	C_L = 10pF	●			26	ns
t_{18}	$\overline{D}$/S Valid to READ Rising Edge	(Note 10)	●	7			ns
t_{19}	READ Rising Edge to UPD Rising Edge	No Update	●	0			ns
t_{20}	UPD Falling Edge to READ Falling Edge	No Update	●	0			ns
t_{22}	READ Falling Edge to UPD Rising Edge	(Note 10)	●	7			ns
t_{23}	I/O Bus Hi-Z to READ Rising Edge	(Note 10)	●	0			ns
t_{24}	READ Falling Edge to I/O Bus Active	(Note 10)	●	20			ns
$\overline{CLR}$ Timing							
t_{25}	$\overline{CLR}$ Pulse Width Low		●	15			ns
V_{DD} = 2.7V to 3.3V							
Write and Update Timing							
t_1	I/O Valid to $\overline{WR}$ Rising Edge Set-Up		●	15			ns
t_2	I/O Valid to $\overline{WR}$ Rising Edge Hold		●	15			ns
t_3	$\overline{WR}$ Pulse Width Low		●	30			ns
t_4	UPD Pulse Width High		●	30			ns
t_5	UPD Falling Edge to $\overline{WR}$ Falling Edge	No Data Shoot-Through	●	0			ns
t_6	$\overline{WR}$ Rising Edge to UPD Rising Edge	(Note 10)	●	0			ns
t_7	$\overline{D}$/S Valid to $\overline{WR}$ Falling Edge Set-Up Time		●	7			ns
t_8	$\overline{WR}$ Rising Edge to $\overline{D}$/S Valid Hold Time		●	7			ns
t_9	A1-A0 Valid to $\overline{WR}$ Falling Edge Setup Time		●	7			ns
t_{10}	$\overline{WR}$ Rising Edge to A1-A0 Valid Hold Time		●	0			ns
t_{11}	A1-A0 Valid to UPD Rising Edge Setup Time		●	15			ns
t_{12}	UPD Falling Edge to A1-A0 Valid Hold Time		●	15			ns
Readback Timing							
t_{13}	$\overline{WR}$ Rising Edge to Read Rising Edge		●	10			ns
t_{14}	Read Falling Edge to $\overline{WR}$ Falling Edge	(Note 10)	●	35			ns
t_{15}	Read Rising Edge to I/O Propagation Delay	C_L = 10pF	●			53	ns
t_{26}	A1-A0 Valid to READ Rising Edge Setup Time		●	35			ns
t_{27}	READ Falling to A1-A0 Valid Hold Time	(Note 10)	●	0			ns
t_{17}	UPD Valid to I/O Propagation Delay	C_L = 10pF	●			43	ns
t_{18}	$\overline{D}$/S Valid to Read Rising Edge	(Note 10)	●	12			ns
t_{19}	Read Rising Edge to UPD Rising Edge	No Update	●	0			ns
t_{20}	UPD Falling Edge to Read Falling Edge	No Update	●	0			ns

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 2.7V to 3.3V							
t_{22}	READ Falling Edge to UPD Rising Edge	(Note 10)	●	10			ns
t_{23}	I/O Bus Hi-Z to Read Rising Edge	(Note 10)	●	0			ns
t_{24}	Read Falling Edge to I/O Bus Active	(Note 10)	●	35			ns
$\overline{CLR}$ Timing							
t_{25}	$\overline{CLR}$ Pulse Width Low		●	20			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Because of the proprietary SoftSpan switching architecture, the measured resistance looking into each of the specified pins is constant for all output ranges if the I_{OUT1X} and I_{OUT2X} pins are held at ground.

Note 4: R1 is measured from R_{IN} to R_{COM}; R2 is measured from REFA to R_{COM}.

Note 5: Using LT1469 with $C_{FEEDBACK}$ = 15pF. A ±0.0015% settling time of 1.7µs can be achieved by optimizing the time constant on an individual basis. See Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.

Note 6: Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1469; C_{FB} = 27pF.

Note 7. Full-scale transition; REF = 0V.

Note 8. REF = $6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1469.

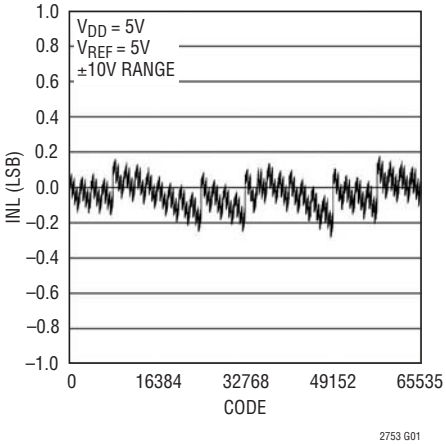
Note 9. Calculation from $V_n = \sqrt{4kTRB}$, where k = 1.38E-23 J/°K (Boltzmann constant), R = resistance (Ω), T = temperature (°K), and B = bandwidth (Hz).

Note 10. Guaranteed by design. Not production tested.

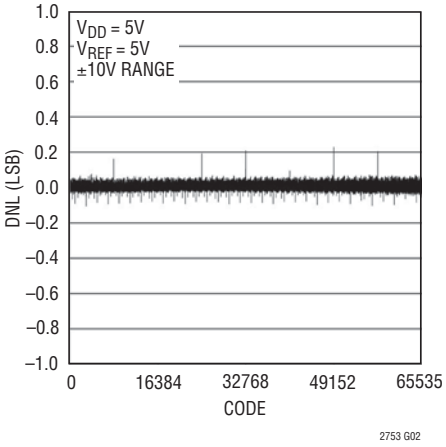
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2753-16

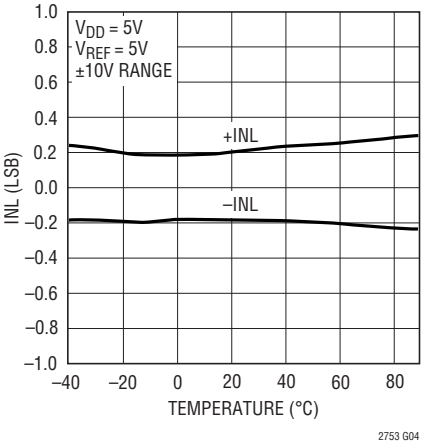
Integral Nonlinearity (INL)



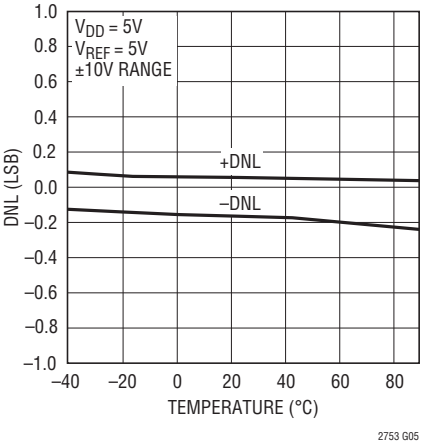
Differential Nonlinearity (DNL)



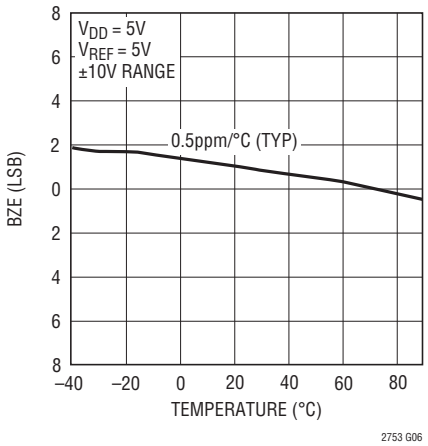
INL vs Temperature



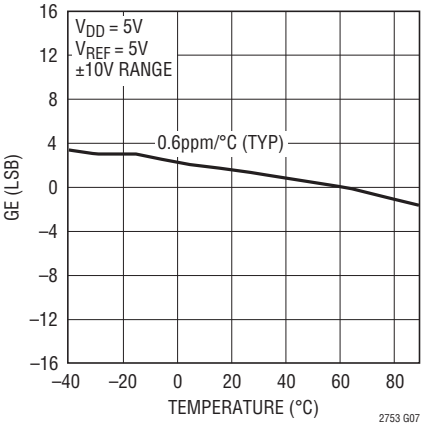
DNL vs Temperature



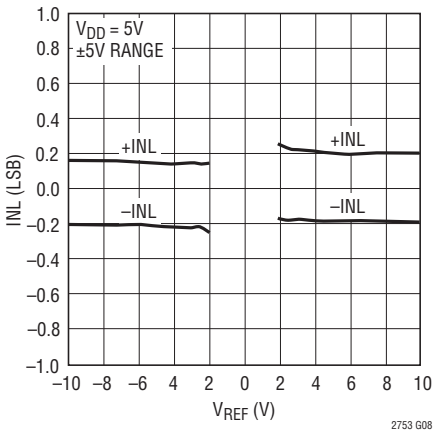
Bipolar Zero vs Temperature



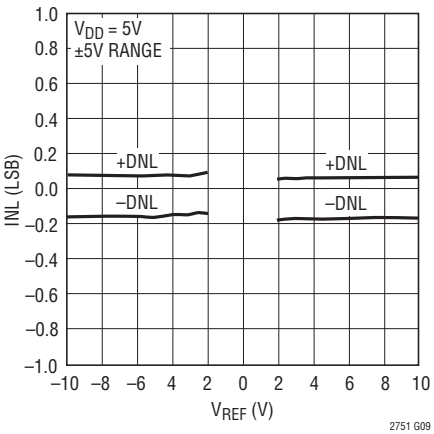
Gain Error vs Temperature



INL vs V_{REF}



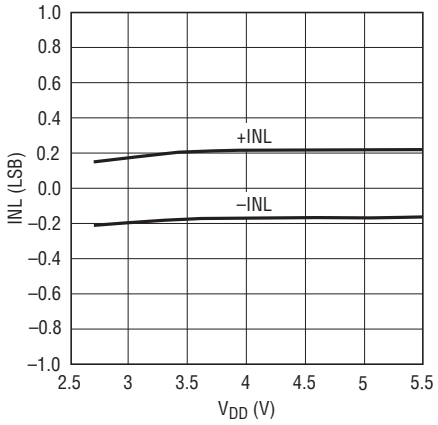
DNL vs V_{REF}



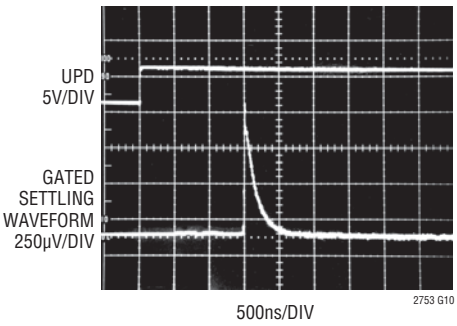
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2753-16

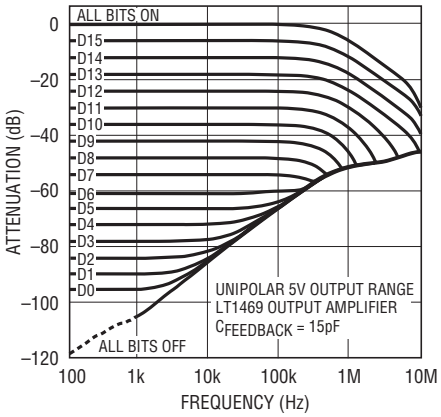
INL vs V_{DD}



Settling 0V to 10V

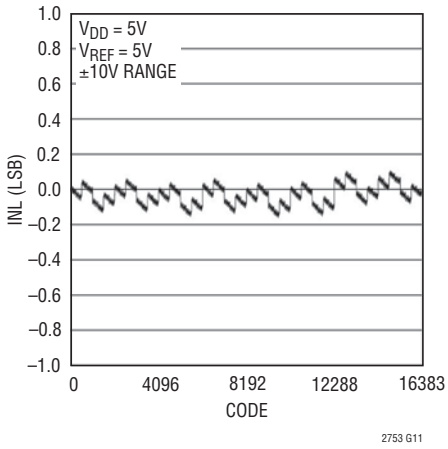


Multiplying Frequency Response vs Digital Code

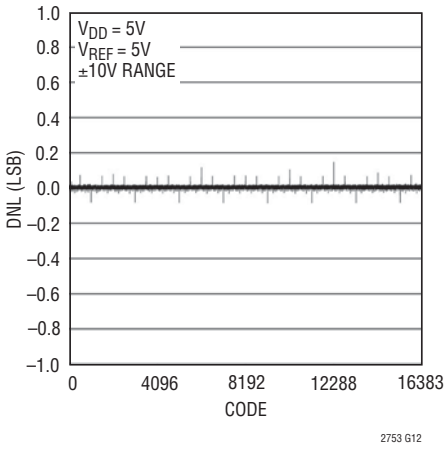


LTC2753-14

Integral Nonlinearity (INL)

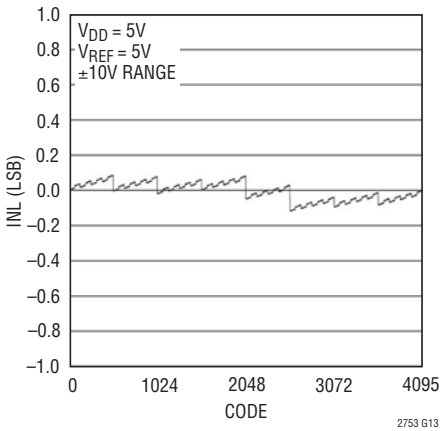


Differential Nonlinearity (DNL)

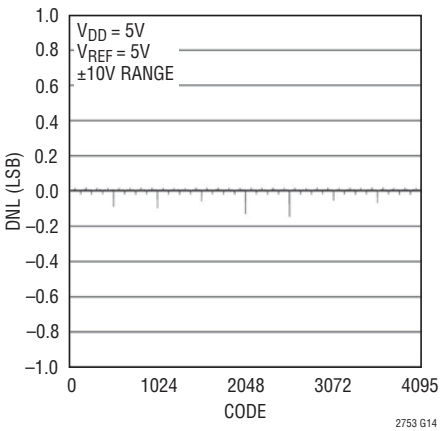


LTC2753-12

Integral Nonlinearity (INL)



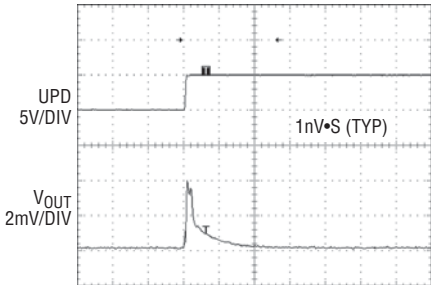
Differential Nonlinearity (DNL)



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

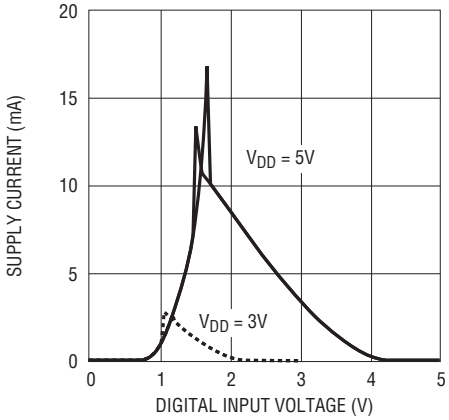
LTC2753-12, LTC2753-14, LTC2753-16

Midscale Glitch

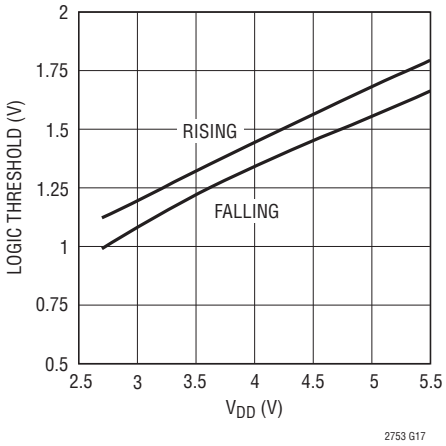


V_{DD} = 5V
V_{REF} = 5V
0V TO 5V RANGE
USING AN LT1469
$C_{FEEDBACK}$ = 27pF

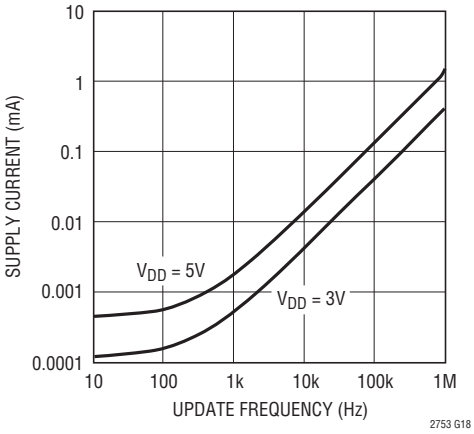
Supply Current vs Logic Input Voltage



Logic Threshold vs Supply Voltage



Supply Current vs Update Frequency



PIN FUNCTIONS

R_{COM} (Pin 1): Center Tap Point for the Reference Inverting Resistors. The 20k reference inverting resistors R1 and R2 are connected internally from R_{IN} to R_{COM} and from R_{COM} to REFA, respectively (see Block Diagram). For normal operation tie R_{COM} to the negative input of the external reference inverting amplifier (see Typical Applications).

R_{IN} (Pin 2): Input Resistor R1 of the Reference Inverting Resistors. The 20k resistor R1 is connected internally from R_{IN} to R_{COM}. For normal operation tie R_{IN} to the external reference voltage V_{REF}. Typically 5V; accepts up to ±15V.

S2 (Pin 3): Span I/O Bit 2. Pins S0, S1 and S2 are used to program and to read back the output ranges of the DACs.

I_{OUT2A} (Pin 4): DAC A Current Output Complement. Tie I_{OUT2A} to ground.

GND (Pin 5): Shield Ground, provides necessary shielding for I_{OUT2A}. Tie to ground.

D3-D11 (Pins 6-14): LTC2753-12 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D11 is the MSB.

D5-D13 (Pins 6-14): LTC2753-14 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D13 is the MSB.

D7-D15 (Pins 6-14): LTC2753-16 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D15 is the MSB.

V_{DD} (Pin 15): Positive Supply Input $2.7V \le V_{DD} \le 5.5V$. Requires a 0.1µF bypass capacitor to GND.

NC (Pin 16): No Internal Connection.

A1 (Pin 17): DAC Address Bit 1. See Table 3.

A0 (Pin 18): DAC Address Bit 0. See Table 3.

GND (Pin 19): Ground. Tie to ground.

$\overline{CLR}$ (Pin 20): Asynchronous Clear. When $\overline{CLR}$ is taken to a logic low, the data registers are reset to the zero-volt code for the present output range (V_{OUT} = 0V).

MSPAN (Pin 21): Manual Span Control Pin. MSPAN is used to configure the LTC2753 for operation in a single, fixed output range. When configured for single-span operation, the output range is set via hardware pin strapping. The input and DAC registers of the span I/O port are transparent and do not respond to write or update commands.

To configure the part for single-span use, tie MSPAN directly to V_{DD}. If MSPAN is instead connected to GND (SoftSpan configuration), the output ranges are set and verified by using write, update and read operations. See Manual Span Configuration in the Operation section. MSPAN must be connected either directly to GND (SoftSpan configuration) or V_{DD} (single-span configuration).

D0-D2 (Pins 22-24): LTC2753-12 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D0 is the LSB.

D0-D4 (Pins 22-26): LTC2753-14 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D0 is the LSB.

D0-D6 (Pins 22-28): LTC2753-16 Only. DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D0 is the LSB.

NC (Pins 25-30): LTC2753-12 Only. No Internal Connection.

NC (Pins 27-30): LTC2753-14 Only. No Internal Connection.

NC (Pins 29, 30): LTC2753-16 Only. No Internal Connection.

GND (Pin 31): Shield Ground, provides necessary shielding for I_{OUT2B}. Tie to ground.

I_{OUT2B} (Pin 32): DAC B Current Output Complement. Tie I_{OUT2B} to ground.

S0 (Pin 33): Span I/O Bit 0. Pins S0, S1 and S2 are used to program and to read back the output range of the DACs.

$\overline{D}$/S (Pin 34): Data/Span Select. This pin is used to select the data I/O pins or the span I/O pins (D0 to D15 or S0 to S2, respectively), along with their respective dedicated registers, for write or read operations. Update operations ignore $\overline{D}$/S, since all updates affect both data and span registers. For single-span operation, tie $\overline{D}$/S to ground.

READ (Pin 35): Read Pin. When READ is asserted high, the data I/O pins (D0-D15) or span I/O pins (S0-S2)

PIN FUNCTIONS

output the contents of the selected register (see Table 1). For single-span operation, readback of the span I/O pins is disabled.

UPD (Pin 36): Update and Buffer Select Pin. When READ is held low and UPD is asserted high, the contents of the addressed DAC's input registers (both data and span) are copied into their respective DAC registers. The output of the DAC is updated, reflecting the new DAC register values.

When READ is held high, the update function is disabled and the UPD pin functions as a buffer selector—logic low to select the input register, high to select the DAC register. See Readback in the Operation section.

$\overline{WR}$ (Pin 37): Active Low Write Pin. A Write operation copies the data present on the data or span I/O pins (D0-D15 or S0-S2, respectively) into the associated input register. When READ is high, the Write function is disabled.

S1 (Pin 38): Span I/O Bit 1. Pins S0, S1 and S2 are used to program and to read back the output ranges of the DACs.

REFB (Pin 39): Reference Input for DAC B. The impedance looking into this pin is 10k to ground. For normal operation tie to the output of the reference inverting amplifier. Typically –5V; accepts up to ±15V.

R_{OFSB} (Pin 40): Bipolar Offset Network for DAC B. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{IN} (Pin 2). The impedance looking into this pin is 20k to ground.

R_{FBB} (Pin 41): DAC B Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC B (see Typical Applications). The DAC output current from I_{OUT1B} flows through the feedback resistor to the R_{FBB} pin. The impedance looking into this pin is 10k to ground.

I_{OUT1B} (Pin 42): DAC B Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC B (see Typical Applications).

R_{VOSB} (Pin 43): DAC B Offset Adjust. Nominal input range is ±5V. The impedance looking into this pin is 1M to ground. If not used, tie R_{VOSB} to ground.

R_{VOSA} (Pin 44): DAC A Offset Adjust. Nominal input range is ±5V. The impedance looking into this pin is 1M to ground. If not used, tie R_{VOSA} to ground.

I_{OUT1A} (Pin 45): DAC A Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC A (see Typical Applications).

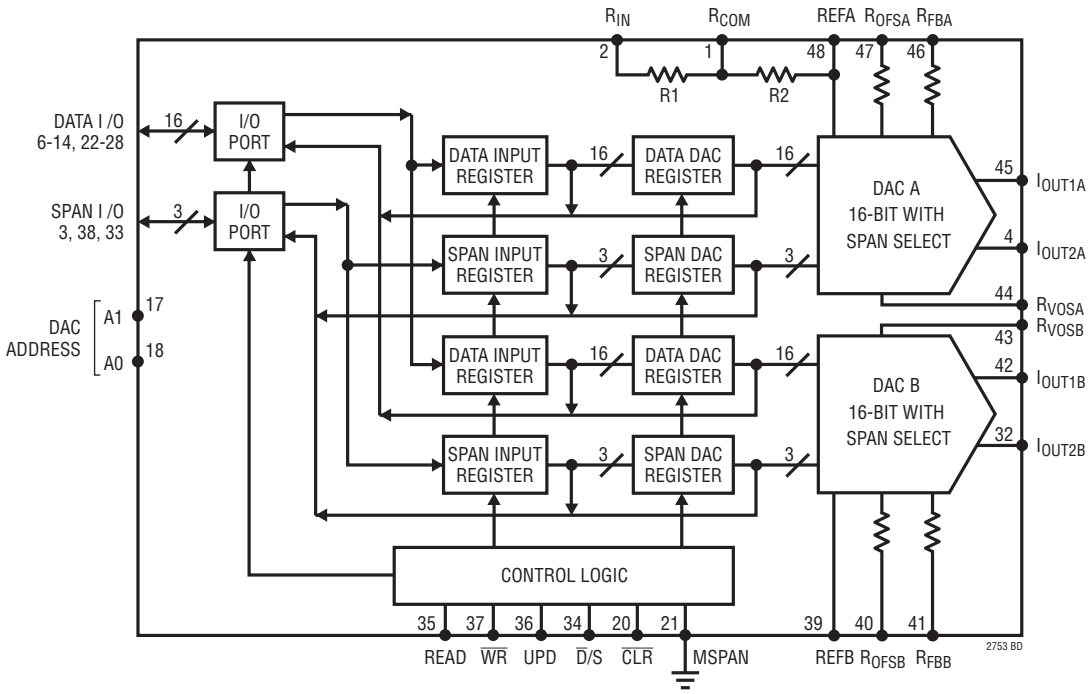
R_{FBA} (Pin 46): DAC A Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC A (see Typical Applications). The DAC output current from I_{OUT1A} flows through the feedback resistor to the RFBA pin. The impedance looking into this pin is 10k to ground.

R_{OFSA} (Pin 47): Bipolar Offset Network for DAC A. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{IN} (Pin 2). The impedance looking into this pin is 20k to ground.

REFA (Pin 48): Reference Input for DAC A, and connection for internal reference inverting resistor R2. The 20k resistor R2 is connected internally from R_{COM} to REFA. For normal operation tie this pin to the output of the reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{IN} and R_{COM} floating).

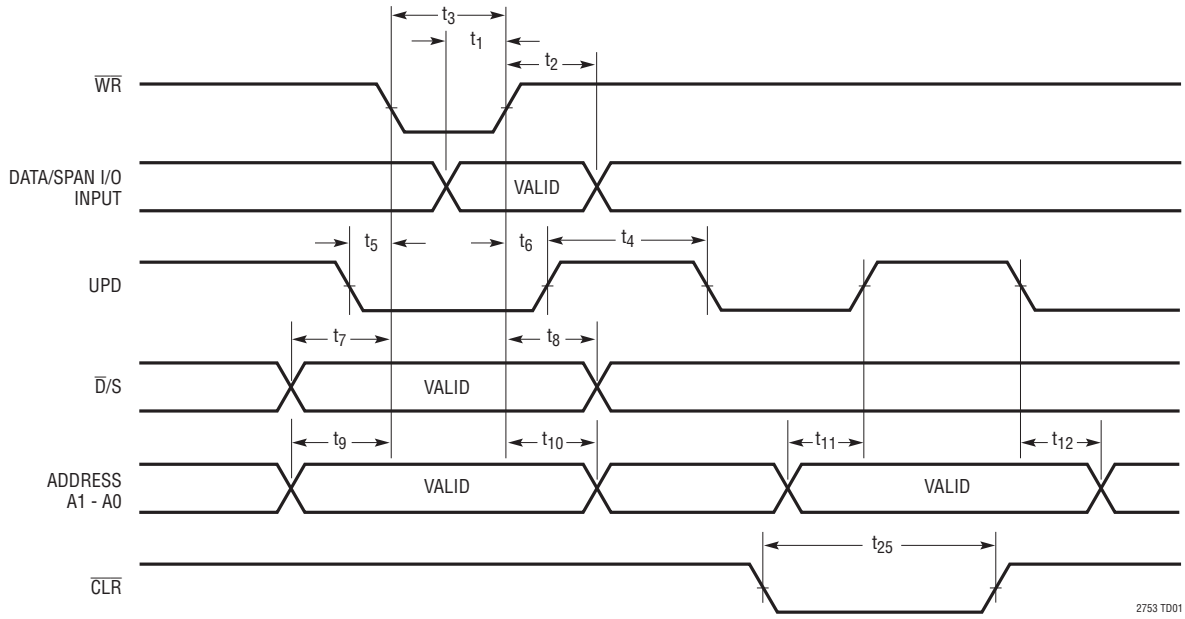
Exposed Pad (Pin 49): Ground. The Exposed Pad must be soldered to the PCB.

BLOCK DIAGRAM

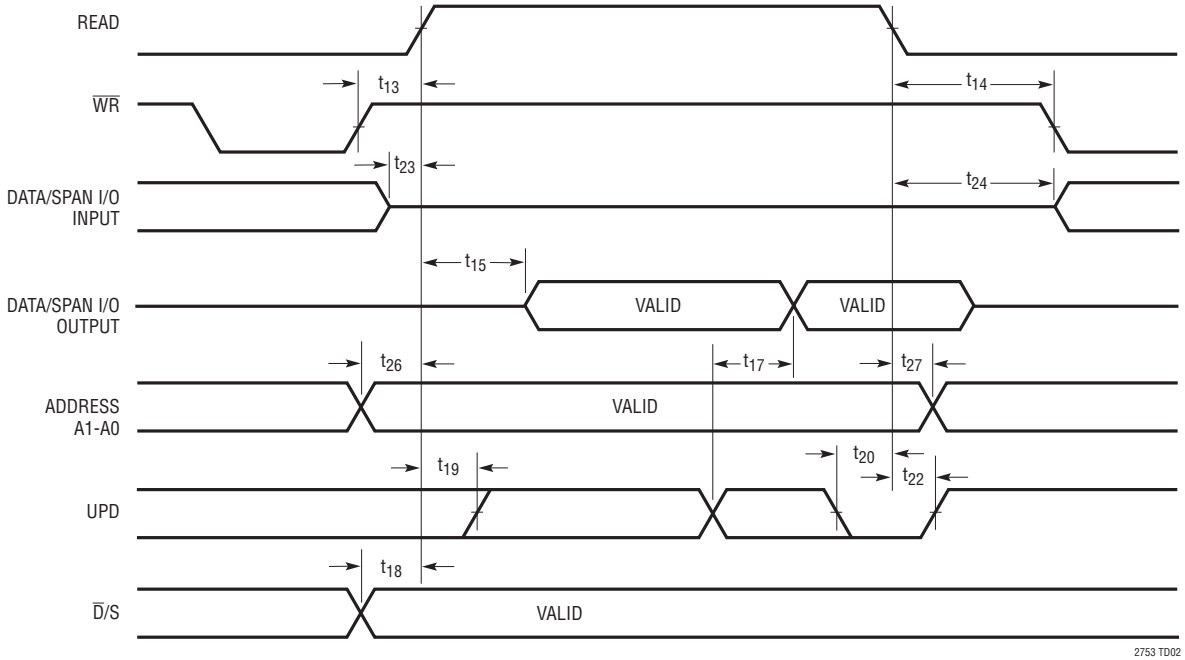


TIMING DIAGRAMS

Write, Update and Clear Timing



Readback Timing



OPERATION

Output Ranges

The LTC2753 is a dual current-output, parallel-input precision multiplying DAC with software-programmable output ranges. SoftSpan provides two unipolar output ranges (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. When a reference voltage of 2V is used, the SoftSpan ranges become: 0V to 2V, 0V to 4V, ±1V, ±2V, ±4V and –1V to 3V. The output ranges are linearly scaled for references other than 2V and 5V.

Digital Section

The LTC2753 has 4 internal registers for each DAC, a total of 8 registers (see Block Diagram). Each DAC channel has two sets of double-buffered registers—one set for the data, and one set for the span (output range) of the DAC. The double-buffered feature provides the capability to simultaneously update the span and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register. The input registers are holding buffers—when data is loaded into an input register via a write operation, the DAC outputs are not affected.

The contents of a DAC register, on the other hand, directly control the DAC output voltage or output range. The contents of the DAC registers are changed by copying the contents of an input register into its associated DAC register via an update operation.

Write and Update Operations

The data input register of the addressed DAC is loaded directly from a 16-bit microprocessor bus by holding the $\overline{D}$/S pin low and pulsing the $\overline{WR}$ pin low (write operation). The DAC register is loaded by pulsing the UPD pin high (update operation), which copies the data held in the input register into the DAC register. Note that updates always include both data and span; but the DAC register values will not change unless the input register values have previously been changed via a write operation.

Loading the span input register is accomplished similarly, holding the $\overline{D}$/S pin high and bringing the $\overline{WR}$ pin low. The span and data register structures are the same except for the number of parallel bits—the span registers have 3 bits, while the data registers have 12, 14, or 16.

To make both registers transparent for flowthrough mode, tie $\overline{WR}$ low and UPD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the UPD pin.

The interface also allows the use of the input and DAC registers in a master-slave, or edge-triggered, configuration. This mode of operation occurs when $\overline{WR}$ and UPD are tied together and driven by a single clock signal. The data bits are loaded into the input register on the falling edge of the clock and then loaded into the DAC register on the rising edge.

It is possible to control both data and span on one 16-bit wide data bus by allowing span pins S2 to S0 to share bus lines with the data LSBs (D2 to D0). No write or read operation includes both span and data, so there cannot be a conflict.

The asynchronous clear pin resets both DACs to 0V in any output range. $\overline{CLR}$ resets all data registers, while leaving the span registers undisturbed.

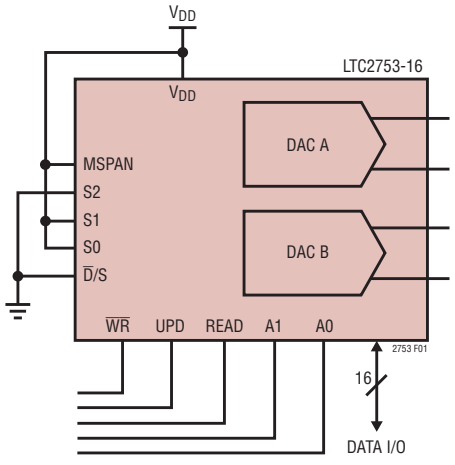


Figure 1. Using MSPAN to Configure the LTC2753 for Single-Span Operation (±10V Range).

OPERATION

These devices also have a power-on reset that initializes both DACs to V_{OUT} = 0V in any output range. The DACs power up in the 0V-5V range if the part is in SoftSpan configuration; for manual span (see Manual Span Configuration below), both DACs power up in the manually-chosen range at the appropriate code.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2753 for single-span operation, tie the MSPAN pin to V_{DD} and the $\overline{D}$/S pin to GND. The desired output range is then specified by the span I/O pins (S0, S1 and S2) as usual, but the pins are programmed by tying directly to GND or V_{DD} (see Figure 1 and Table 2). In this configuration, both DAC channels will initialize to the chosen output range at power-up, with V_{OUT} = 0V.

When configured for manual span operation, span pin readback is disabled.

Readback

The contents of any one of the 8 interface registers can be read back from the I/O ports.

The I/O pins are grouped into two ports: data and span. The data I/O port comprises pins D0-D11, D0-D13 or D0-D15 (LTC2753-12, LTC2753-14 or LTC2753-16, respectively). The span I/O port comprises pins S0, S1 and S2 for all parts.

Each DAC channel has a set of data registers that are controlled and read back from the data I/O port; and a set of span registers that are controlled and read back from the span I/O port. The register structure is shown in the Block Diagram.

A readback operation is initiated by asserting READ to logic high after selecting the desired DAC channel and I/O port. The I/O pins, which are high-impedance digital inputs when READ is low, selectively change to low-impedance logic outputs during readback.

Select the DAC channel with address pins A1 and A0, and select the I/O port (data or span) to be read back with the $\overline{D}$/S pin. The selected I/O port's pins become logic outputs during readback, while the unselected I/O port's pins remain high-impedance inputs.

With the DAC channel and I/O port selected, assert READ high and select the desired input or DAC register using the UPD pin. Note that UPD is a two function pin—the update function is only available when READ is low. When READ is high, the update function is disabled and the UPD pin instead selects the input or DAC register for readback. Table 1 shows the readback functions for the LTC2753.

Table 1. Write, Update and Read Functions

READ	$\overline{D}$/S	$\overline{WR}$	UPD	SPAN I/O	DATA I/O
0	0	0	0	-	Write to Input Register
0	0	0	1	-	Write/Update (Transparent)
0	0	1	0	-	-
0	0	1	1	Update DAC Register	Update DAC Register
0	1	0	0	Write to Input Register	-
0	1	0	1	Write/Update (Transparent)	-
0	1	1	0	-	-
0	1	1	1	Update DAC register	Update DAC Register
1	0	X	0	-	Read Input Register
1	0	X	1	-	Read DAC Register
1	1	X	0	Read Input Register	-
1	1	X	1	Read DAC Register	-

X = Don't Care

The most common readback task is to check the contents of an input register after writing to it, before updating the new data to the DAC register. To do this, hold UPD low and assert READ high. The contents of the selected port's input register are output to its I/O pins.

To read back the contents of a DAC register, hold UPD low and assert READ high, then bring UPD high to select the DAC register. The contents of the selected DAC register are output by the selected port's I/O pins. Note: if no update is desired after the readback operation, UPD must be returned low before bringing READ low; otherwise the UPD pin will revert to its primary function and update the DAC.

OPERATION

System Offset Adjustment

Many systems require compensation for overall system offset. The R_{VOSA} and R_{VOSB} offset adjustment pins are provided for this purpose. For noise immunity and ease of adjustment, the control voltage is attenuated to the DAC output:

$V_{OS} = –0.01 • V(R_{VOSX})$ [0V to 5V, ±2.5V spans]

$V_{OS} = –0.02 • V(R_{VOSX})$ [0V to 10V, ±5V, –2.5V to 7.5V spans]

$V_{OS} = –0.04 • V(R_{VOSX})$ [±10V span]

The nominal input range of this pin is ±5V; other reference voltages of up to 15V may be used if needed. The R_{VOSX} pins have an input impedance of 1MΩ. To preserve the settling performance of the LTC2753, drive this pin with a Thevenin-equivalent impedance of 10k or less. Short any unused system offset adjustment pins to I_{OUT2}.

Table 2. Span Codes

S2	S1	S0	SPAN
0	0	0	Unipolar 0V to 5V
0	0	1	Unipolar 0V to 10V
0	1	0	Bipolar –5V to 5V
0	1	1	Bipolar –10V to 10V
1	0	0	Bipolar –2.5V to 2.5V
1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved and should not be used.

Table 3. Address Codes

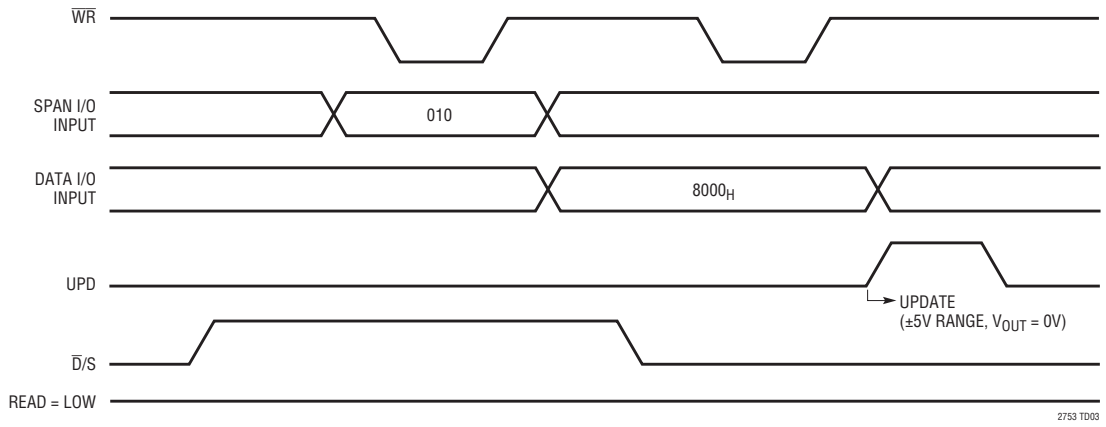
DAC CHANNEL	A1	A0
A	0	0
B	0	1
ALL*	1	1

Codes not shown are reserved and should not be used.

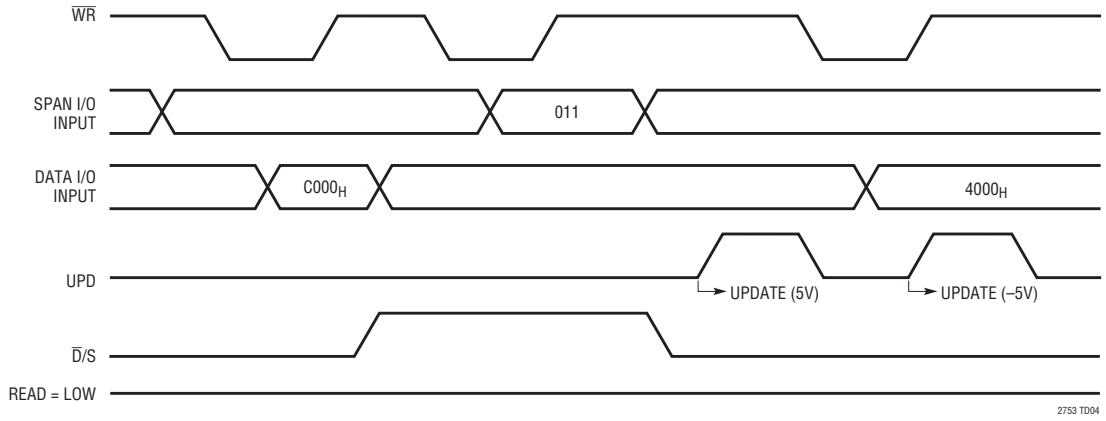
*If readback is taken using the All DACs address, the LTC2753 defaults to DAC A.

OPERATION—EXAMPLES

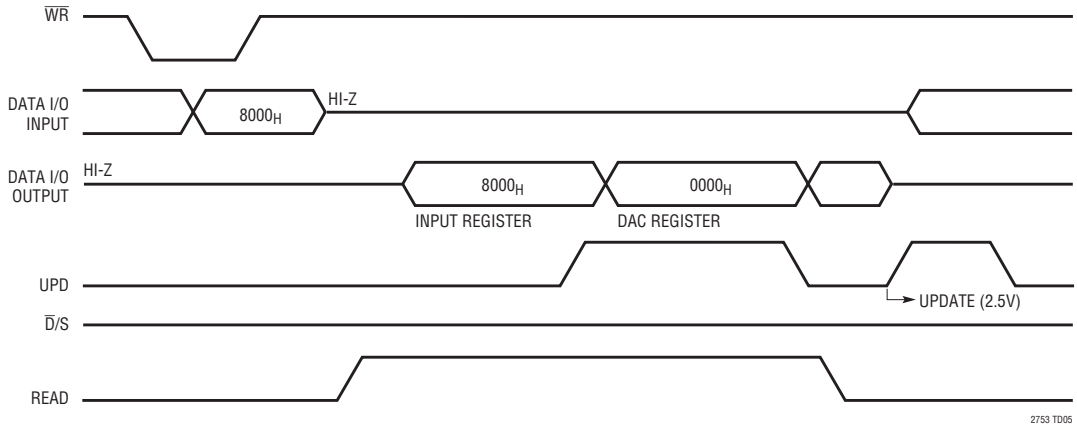
1. Load ±5V range with the output at 0V. Note that since span and code are updated together, the output, if started at 0V, will stay there. The 16-Bit DAC code is shown in hex for compactness.



2. Load ±10V range with the output at 5V, changing to –5V.



3. Write and update midscale code in 0V to 5V range (V_{OUT} = 2.5V) using readback to check the contents of the input and DAC registers before updating.



APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC2753-16, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 4 and 5 contain equations for evaluating the effects of op amp parameters on the LTC2753's accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error. Tables 4 and 5 can also be used to determine the effects of op amp parameters on the LTC2753-14 and the LTC2753-12. However, the results obtained from Tables 4 and 5 are in 16-bit LSBs. Divide these results by 4 (LTC2753-14) and 16 (LTC2753-12) to obtain the correct LSB sizing.

Table 6 contains a partial list of LTC precision op amps recommended for use with the LTC2753. The easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 6 and insert the specified op amp parameters in Table 5. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Table 4. Variables for Each Output Range That Adjust the Equations in Table 5

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1		1
10V	2.2	3	0.5		1.5
±5V	2	2	1	1	1.5
±10V	4	4	0.83	1	2.5
±2.5V	1	1	1.4	1	1
–2.5V to 7.5V	1.9	3	0.7	0.5	1.5

Table 5. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 3.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 0.82 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 19.8 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \bullet 0.0003 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.00008 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/V)	$A1 \bullet \left(\frac{16.5k}{A_{VOL1}}\right)$	$A2 \bullet \left(\frac{1.5k}{A_{VOL1}}\right)$		0	$A5 \bullet \left(\frac{131k}{A_{VOL1}}\right)$ 0	$A5 \bullet \left(\frac{131k}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \bullet \left(V_{OS2} \bullet 13.1 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (mV)	0	0	0	$A4 \bullet \left(I_{B2} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$I_{B2} \bullet 0.26 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 0.26 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/V)	0	0	0	$A4 \bullet \left(\frac{66k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$

Table 6. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2753 with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{VOL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC2753 µs	POWER DISSIPATION mW
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	120	11
LT1112 (Dual)	60	0.25	1500	14	0.008	0.16	0.75	115	10.5/Op Amp
LT1124 (Dual)	70	20	4000	2.7	0.3	4.5	12.5	19	69/Op Amp
LT1468	75	10	5000	5	0.6	22	90	2	117
LT1469 (Dual)	125	10	2000	5	0.6	22	90	2	123/Op Amp

APPLICATIONS INFORMATION

Op amp offset will contribute mostly to output offset and gain error, and has minimal effect on INL and DNL. For example, for the LTC2753-16 with a 5V reference in 5V unipolar mode, a 250µV op amp offset will cause a 3.3LSB zero-scale error and a 3.3LSB gain error; but only 0.8LSB of INL degradation and 0.2LSB of DNL degradation.

While not directly addressed by the simple equations in Tables 4 and 5, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers in the V_{OS} and I_B equations from Table 5 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time, offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2753 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2753 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's apparent INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Table 7. Partial List of LTC Precision References Recommended for Use with the LTC2753 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05%	5ppm/°C	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05%	5ppm/°C	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075%	10ppm/°C	$20\mu V_{P-P}$
LT1790A-2.5	±0.05%	10ppm/°C	$12\mu V_{P-P}$

APPLICATIONS INFORMATION

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding techniques should be used. I_{OUT2} must be tied to the star ground with as low a resistance as possible. When it is not possible to locate star ground close to I_{OUT2}, a low resistance trace should be used to route this pin to star ground. This minimizes the voltage drop from this pin to ground caused by the code dependent current flowing to ground. When the resistance of this circuit board trace becomes greater than 1Ω, a force/sense amplifier configuration should be used to drive this pin (see Figure 2). This preserves the excellent accuracy (1LSB INL and DNL) of the LTC2753-16.

APPLICATIONS INFORMATION

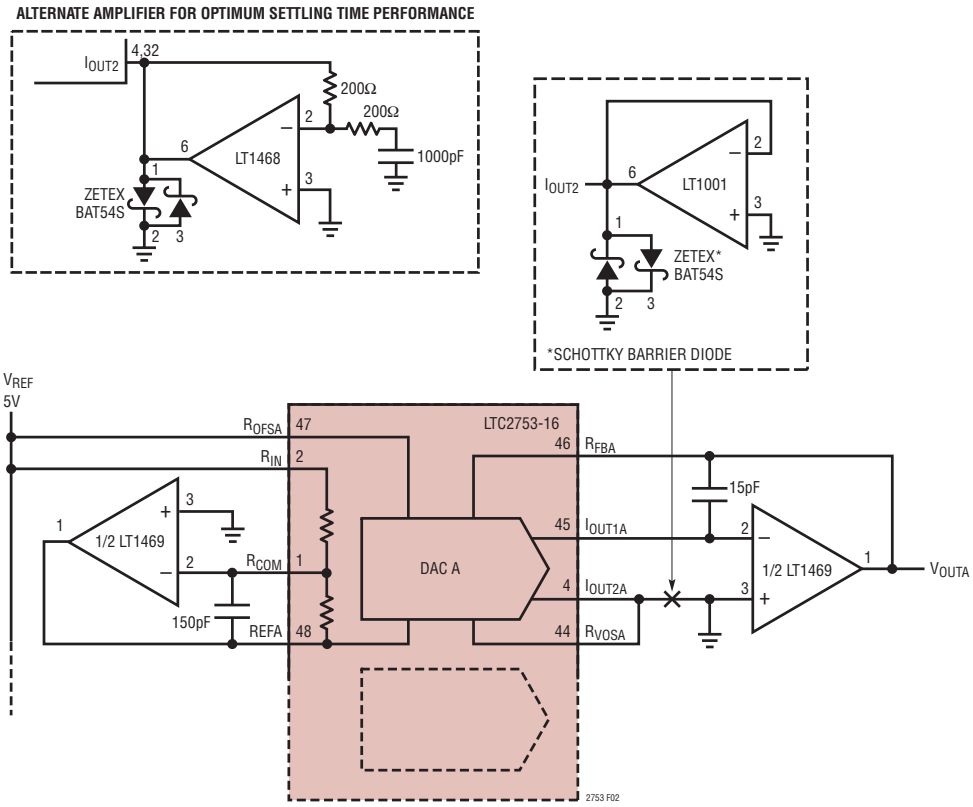
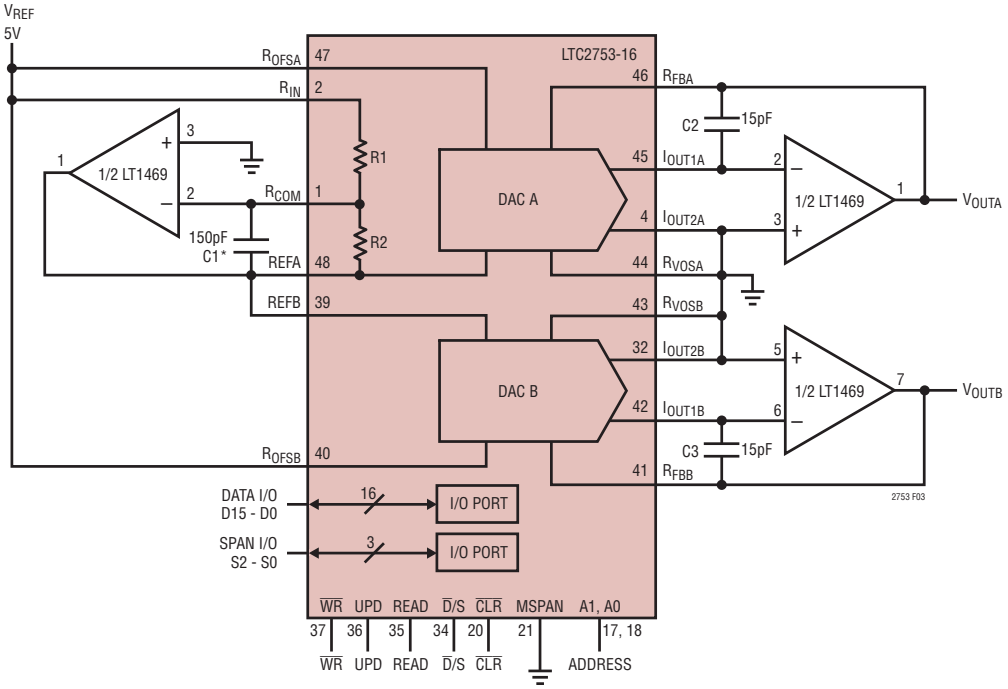


Figure 2. Optional Circuits for Driving I_{OUT2} from GND with a Force/Sense Amplifier.

TYPICAL APPLICATIONS

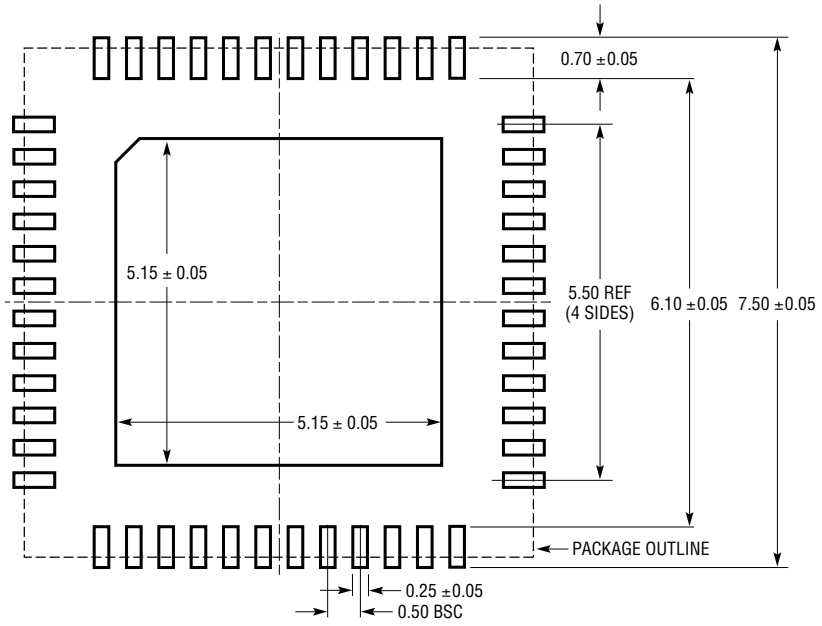
Dual 16-Bit V_{OUT} DAC with Software-Selectable Ranges



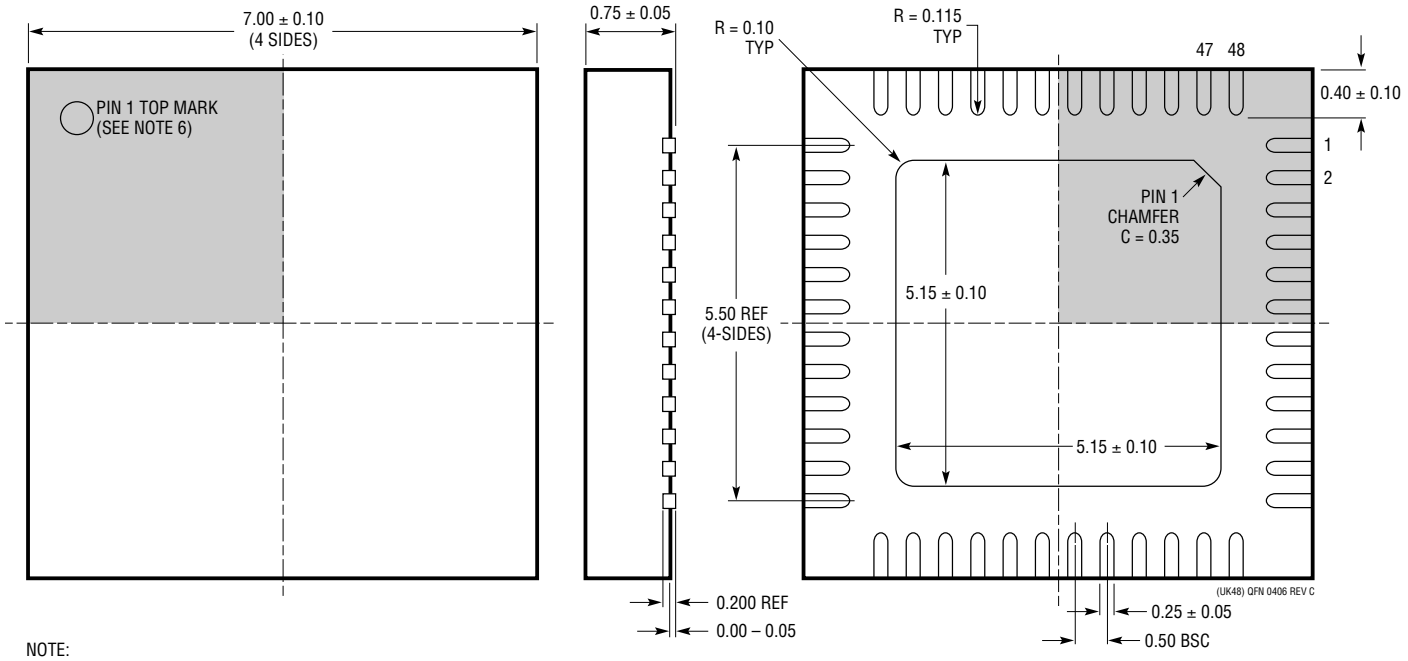
*FOR MULTIPLYING APPLICATIONS C1 = 15pF

PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

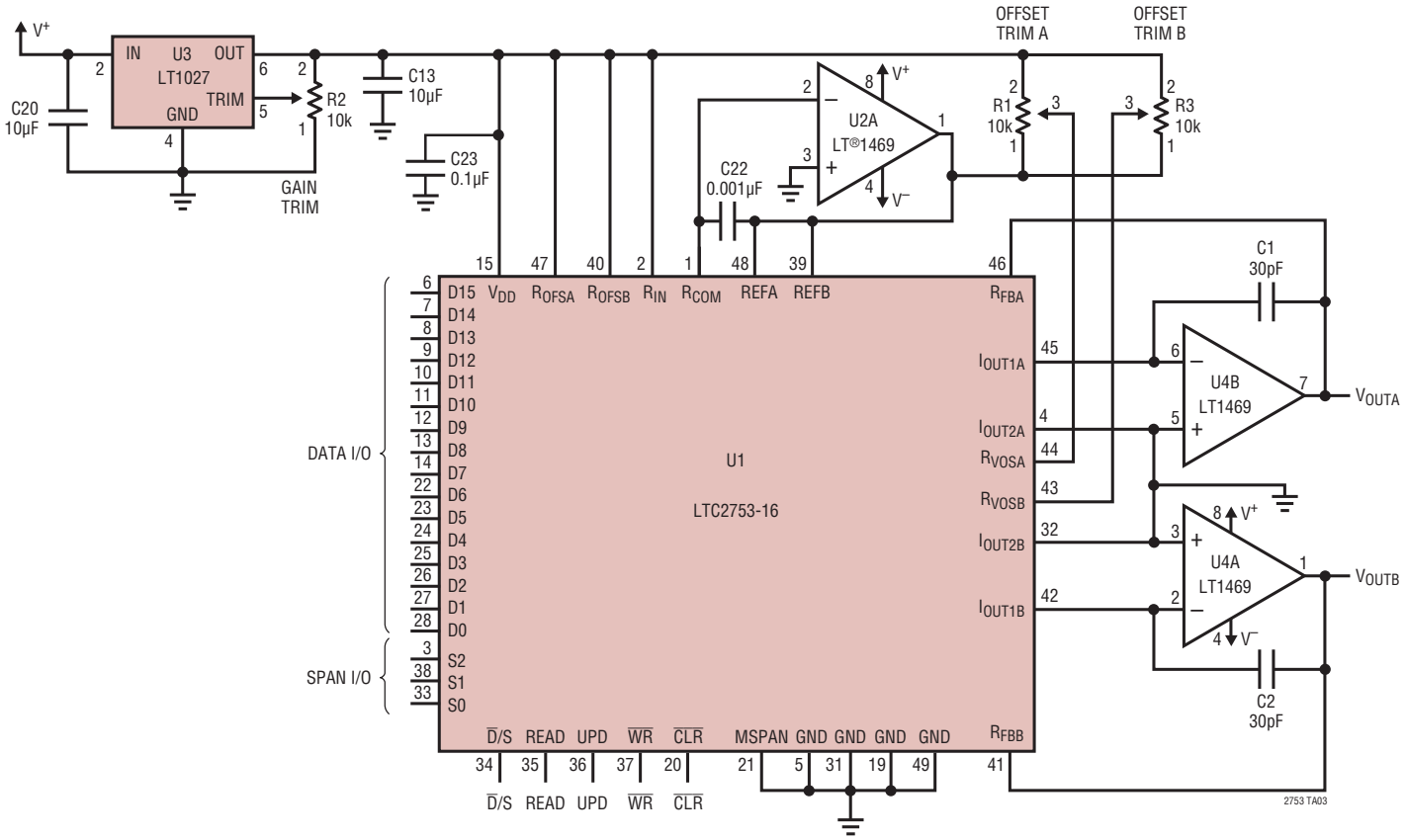


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Offset and Gain Trim Circuits. Powering V_{DD} from LT1027 Ensures Quiet Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1027	Precision Reference	1ppm/°C Maximum Drift
LT1236A-5	Precision Reference	0.05% Maximum Tolerance, 1ppm 0.1Hz to 10Hz Noise
LT1468	16-Bit Accurate Op-Amp	90MHz GBW, 22V/µs Slew Rate
LT1469	Dual 16-Bit Accurate Op-Amp	90MHz GBW, 22V/µs Slew Rate
LTC1588/LTC1589/ LTC1592	Serial 12-/14-/16-Bit I_{OUT} Single DAC	Software-Selectable (SoftSpan) Ranges, ±1LSB INL, DNL, 16-Lead SSOP Package
LTC1591/LTC1597	Parallel 14-/16-Bit I_{OUT} Single DAC	Integrated 4-Quadrant Resistors
LTC1821	Parallel 16-Bit V_{OUT} Single DAC	±1LSB INL, DNL, 0V to 10V, 0V to –10V, ±10V Output Ranges
LTC2601/LTC2611/ LTC2621	Serial 12-/14-/16-Bit V_{OUT} Single DACs	Single DACs, SPI-Compatible, Single Supply, 0V to 5V Outputs in 3mm × 3mm DFN-10 Package
LTC2606/LTC2616/ LTC2626	Serial 12-/14-/16-Bit V_{OUT} Single DACs	Single DACs, I^2C-Compatible, Single Supply, 0V to 5V Outputs in 3mm × 3mm DFN-10 Package
LTC2641/LTC2642	Serial 12-/14-/16-Bit Unbuffered V_{OUT} Single DACs	±2LSB INL, ±1LSB DNL, 1µs Settling, Tiny MSOP-10, 3mm × 3mm DFN-10 Packages
LTC2704	Serial 12-/14-/16-Bit V_{OUT} Quad DACs	Software-Selectable (SoftSpan) Ranges, Integrated Amplifiers, ±2LSB INL
LTC2751	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Single DACs	±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 5mm × 7mm QFN-38 Package

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