

FEATURES

CMOS 10-bit, 40 MSPS sampling analog-to-digital converter

Power dissipation: 74 mW (3 V supply, 40 MSPS)

17 mW (3 V supply, 5 MSPS)

Operation between 2.7 V and 3.6 V supply

Differential nonlinearity: -0.25 LSB

Power-down (standby) mode: 0.65 mW

ENOB: 9.55 at $f_{IN} = 20$ MHz

Out-of-range indicator

Adjustable on-chip voltage reference

IF undersampling up to $f_{IN} = 130$ MHz

Input range: 1 V to 2 V p-p differential or single-ended

Adjustable power consumption

Internal clamp circuit

Qualified for automotive applications

APPLICATIONS

Automotive

GENERAL DESCRIPTION

The [AD9203W](#) is a monolithic low power, single supply, 10-bit, 40 MSPS analog-to-digital converter, with an on-chip voltage reference. The [AD9203W](#) uses a multistage differential pipeline architecture and guarantees no missing codes over the full operating temperature range. Its input range may be adjusted between 1 V and 2 V p-p.

The [AD9203W](#) has an onboard programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of an application.

An external resistor can be used to reduce power consumption when operating at lower sampling rates. This yields power savings for users who do not require the maximum sample rate. This feature is especially useful at sample rates far below 40 MSPS. Excellent performance is still achieved at reduced power. For example, 9.7 ENOB performance may be realized with only 17 mW of power, using a 5 MHz clock.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary or twos complementary output format by using the DFS pin. An out-of-range signal (OTR) indicates an overflow condition that

FUNCTIONAL BLOCK DIAGRAM

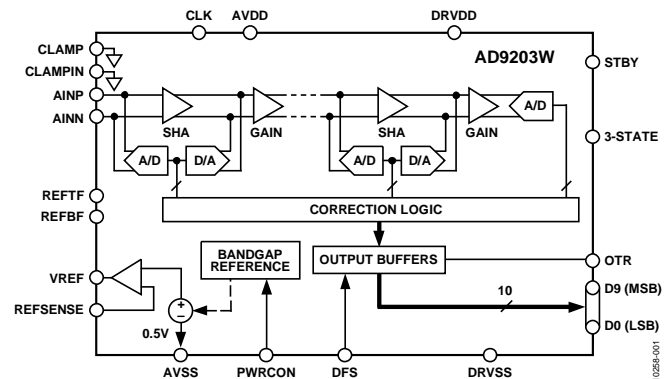


Figure 1.

can be used with the most significant bit to determine over- or underrange.

The [AD9203W](#) can operate with a supply range from 2.7 V to 3.6 V, an attractive option for low power operation in high speed portable applications.

The [AD9203W](#) is specified over industrial (-40°C to $+85^{\circ}\text{C}$) temperature ranges and is available in a 28-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Low Power. The [AD9203W](#) consumes 74 mW on a 3 V supply operating at 40 MSPS. In standby mode, power is reduced to 0.65 mW.
2. High Performance. Maintains better than 9.55 ENOB at 40 MSPS input signal from dc to Nyquist.
3. Very Small Package. The [AD9203W](#) is available in a 28-lead TSSOP.
4. Programmable Power. The [AD9203W](#) power can be further reduced by using an external resistor at lower sample rates.
5. Built-In Clamp Function. Allows dc restoration of video signals.

Rev. 0

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REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3 V, DRVDD = 3 V, F_S = 40 MSPS, input span from 0.5 V to 2.5 V, internal 1 V reference, PWRCON = AVDD, 50% clock duty cycle, T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|--|--------------------|------|-------|--------|--------------|--|
| RESOLUTION | | | 10 | | Bits | |
| MAX CONVERSION RATE | F _S | 40 | | | MSPS | |
| PIPELINE DELAY | | | | 5.5 | Clock Cycles | |
| DC ACCURACY | | | | | | |
| Differential Nonlinearity | DNL | | ±0.25 | ±0.7 | LSB | |
| Integral Nonlinearity | INL | | ±0.65 | ±1.4 | LSB | |
| Offset Error | E _{ZS} | | ±0.6 | ±2.8 | % FSR | |
| Gain Error | E _{FS} | | ±0.7 | ±4.0 | % FSR | |
| ANALOG INPUT | | | | | | |
| Input Voltage Range | A _{IN} | 1 | | 2 | V p-p | |
| Input Capacitance | C _{IN} | | 1.4 | | pF | |
| Aperture Delay | T _{AP} | | 2.0 | | ns | |
| Aperture Uncertainty (Jitter) | T _{AJ} | | 1.2 | | ps rms | |
| Input Bandwidth (−3 dB) | BW | | 390 | | MHz | |
| Input Referred Noise | | | 0.3 | | mV | Switched, single-ended |
| INTERNAL REFERENCE | | | | | | |
| Output Voltage (0.5 V Mode) | VREF | | 0.5 | | V | REFSENSE = VREF |
| Output Voltage (1 V Mode) | VREF | | 1 | | V | REFSENSE = GND |
| Output Voltage Tolerance (1 V Mode) | | | ± 5 | ± 30 | mV | |
| Load Regulation | | | 0.65 | 1.2 | mV | 1.0 mA load |
| POWER SUPPLY | | | | | | |
| Operating Voltage | AVDD | 2.7 | 3.0 | 3.6 | V | |
| | DRVDD | 2.7 | 3.0 | 3.6 | V | |
| Analog Supply Current | I _{AVDD} | | 20.1 | 22.0 | mA | f _{IN} = 4.8 MHz, output bus load = 10 pF |
| Digital Supply Current | I _{DRVDD} | | 4.4 | 6.0 | mA | f _{IN} = 20 MHz, output bus load = 20 pF |
| | | | 9.5 | 14.0 | mA | f _{IN} = 4.8 MHz, output bus load = 10pF |
| Power Consumption | | | 74 | 84.0 | mW | f _{IN} = 20 MHz, output bus load = 20 pF |
| | | | 88.8 | 108.0 | mW | |
| Power-Down | P _D | | 0.65 | 1.2 | mW | |
| Power Supply Rejection Ratio | PSRR | | 0.04 | ± 0.25 | % FSR | |
| DYNAMIC PERFORMANCE (A _{IN} = 0.5 dBFS) | | | | | | |
| Signal-to-Noise and Distortion ¹ | SINAD | | | | | |
| f = 4.8 MHz | | | 59.7 | | dB | |
| f = 20 MHz | | 57.2 | 59.3 | | dB | |
| Effective Bits | ENOB | | | | | |
| f = 4.8 MHz ¹ | | | 9.6 | | Bits | |
| f = 20 MHz | | 9.2 | 9.55 | | Bits | |
| Signal-to-Noise Ratio | SNR | | | | | |
| f = 4.8 MHz ¹ | | | 60.0 | | dB | |
| f = 20 MHz | | 57.5 | 59.5 | | dB | |
| Total Harmonic Distortion | THD | | | | | |
| f = 4.8MHz | | | −76.0 | | dB | |
| f = 20 MHz | | | −74.0 | −65.0 | dB | |
| Spurious-Free Dynamic Range | SFDR | | | | | |
| f = 4.8 MHz ¹ | | | 80 | | dB | |
| f = 20 MHz | | 67.8 | 78 | | dB | |

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|--|------------------|-------|-----|-------|--------|-----------------------------|
| Two-Tone Intermodulation Distortion | IMD | | 68 | | dB | f = 44.49 MHz and 45.52 MHz |
| Differential Phase | DP | | 0.2 | | Degree | NTSC 40 IRE ramp |
| Differential Gain | DG | | 0.3 | | % | |
| DIGITAL INPUTS | | | | | | |
| High Input Voltage | V _{IH} | 2.0 | | | V | |
| Low Input Voltage | V _{IL} | | | 0.4 | V | |
| Clock Pulse Width High | | 11.25 | | | ns | |
| Clock Pulse Width Low | | 11.25 | | | ns | |
| Clock Period ² | | | 25 | | ns | |
| DIGITAL OUTPUTS | | | | | | |
| High-Z Leakage | I _{oZ} | | | ± 5.0 | μA | Output = 0 to DRVDD |
| Data Valid Delay | t _{OD} | | 5 | | ns | C _L = 20 pF |
| Data Enable Delay | t _{DEN} | | 6 | | ns | C _L = 20 pF |
| Data High-Z Delay | t _{DHZ} | | 6 | | ns | C _L = 20 pF |
| LOGIC OUTPUT (with DRVDD = 3 V) | | | | | | |
| High Level Output Voltage (I _{OH} = 50 μA) | V _{OH} | 2.95 | | | V | |
| High Level Output Voltage (I _{OH} = 0.5 mA) | V _{OH} | 2.80 | | | V | |
| Low Level Output Voltage (I _{OL} = 1.6 mA) | V _{OL} | | | 0.3 | V | |
| Low Level Output Voltage (I _{OL} = 50 μA) | V _{OL} | | | 0.05 | V | |

¹ Differential Input (2 V p-p).

² The AD9203W converts at clock rates as low as 20 kHz.

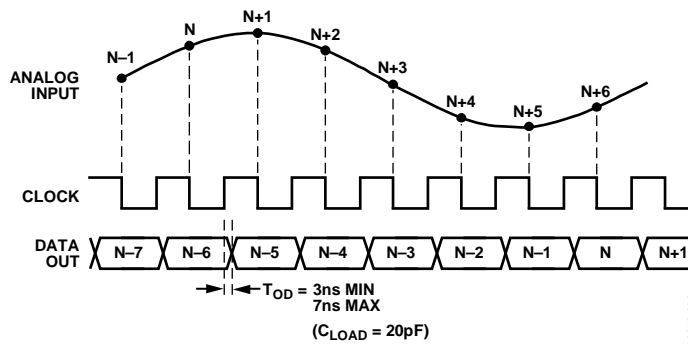


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | With Respect to | Rating | Unit |
|-------------------------|-----------------|--------------------------|------|
| AVDD | AVSS | -0.3 to +3.9 | V |
| DRVDD | DRVSS | -0.3 to +3.9 | V |
| AVSS | DRVSS | -0.3 to +0.3 | V |
| AVDD | DRVDD | -3.9 to +3.9 | V |
| REFCOM | AVSS | -0.3 to +0.3 | V |
| CLK | AVSS | -0.3 to AVDD + 0.3 | V |
| Digital Outputs | DRVSS | -0.3 to DRVDD + 0.3 | V |
| AINP | AINN | AVSS - 0.3 to AVDD + 0.3 | V |
| VREF | AVSS | -0.3 to AVDD + 0.3 | V |
| REFSENSE | AVSS | -0.3 to AVDD + 0.3 | V |
| REFTF, REFBF | AVSS | -0.3 to AVDD + 0.3 | V |
| STBY | AVSS | -0.3 to AVDD + 0.3 | V |
| CLAMP | AVSS | -0.3 to AVDD + 0.3 | V |
| CLAMPIN | AVSS | -0.3 to AVDD + 0.3 | V |
| PWRCON | AVSS | -0.3 to AVDD + 0.3 | V |
| DFS | AVSS | -0.3 to AVDD + 0.3 | V |
| 3-STATE | AVSS | -0.3 to AVDD + 0.3 | V |
| Junction Temperature | | 150 | °C |
| Storage Temperature | | +150 | °C |
| Lead Temperature (10 s) | | 300 | °C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

28-Lead TSSOP

$J_A = 97.9^\circ\text{C/W}$

$J_C = 14.0^\circ\text{C/W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

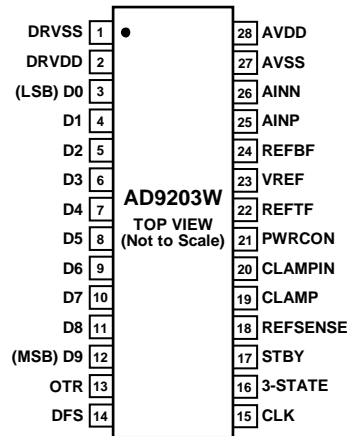
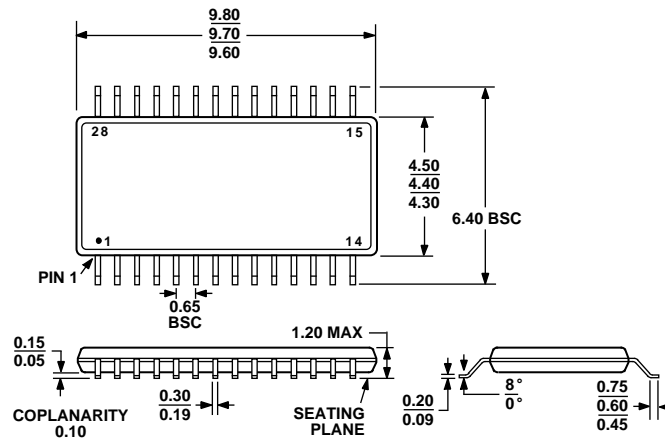


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin | Name | Description |
|-----|----------|--|
| 1 | DRVSS | Digital Ground. |
| 2 | DRVDD | Digital Supply. |
| 3 | D0 | Bit 0, Least Significant Bit. |
| 4 | D1 | Bit 1. |
| 5 | D2 | Bit 2. |
| 6 | D3 | Bit 3. |
| 7 | D4 | Bit 4. |
| 8 | D5 | Bit 5. |
| 9 | D6 | Bit 6. |
| 10 | D7 | Bit 7. |
| 11 | D8 | Bit 8. |
| 12 | D9 | Bit 9, Most Significant Bit. |
| 13 | OTR | Out-of-Range Indicator. |
| 14 | DFS | Data Format Select HI: Twos Complement; LO: Straight Binary. |
| 15 | CLK | Clock Input. |
| 16 | 3-STATE | HI: High Impedance State Output; LO: Active Digital Output Drives. |
| 17 | STBY | HI: Power-Down Mode; LO: Normal Operation. |
| 18 | REFSENSE | Reference Select. |
| 19 | CLAMP | HI: Enable Clamp; LO: Open Clamp. |
| 20 | CLAMPIN | Clamp Signal Input. |
| 21 | PWRCON | Power Control Input. |
| 22 | REFTF | Top Reference Decoupling. |
| 23 | VREF | Reference In/Out. |
| 24 | REFBF | Bottom Reference Decoupling. |
| 25 | AINP | Noninverting Analog Input. |
| 26 | AINN | Inverting Analog Input. |
| 27 | AVSS | Analog Ground. |
| 28 | AVDD | Analog Supply. |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 4. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ^{1,2} | Temperature Range | Package Description | Package Option |
|----------------------|-------------------|---|----------------|
| AD9203WARUZ | −40°C to +85°C | 28-Lead Thin Shrink Small Outline [TSSOP] | RU-28 |
| AD9203WARUZRL7 | −40°C to +85°C | 28-Lead Thin Shrink Small Outline [TSSOP] | RU-28 |

¹Z = RoHS Compliant Part.

²W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD9203W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES