Blackfin A-V EZ-Extender Manual

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ANALOG DEVICES

Copyright Information

Printed in the USA.

Limited Warranty

The A-V EZ-Extender is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The Blackfin A-V EZ-Extender has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The Blackfin A-V EZ-Extender had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

CE

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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A-V EZ-EXTENDER HARDWARE REFERENCE

PREFACE

Thank you for purchasing the Blackfin® A-V EZ-Extender, Analog Devices, Inc. (ADI) extension board to the EZ-KIT Lite® evaluation system for ADSP-BF533, ADSP-BF537, and ADSP-BF561 Blackfin processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing characteristics towards delivering signal processing performance in a microprocessor-like environment.

The EZ-KIT Lite and A-V EZ-Extender are designed to be used in conjunction with the VisualDSP++® development environment. VisualDSP++ offers a powerful programming tool with new flexibility that significantly decreases the time required to port software code to a processor, reducing time-to-market.

To learn more about Analog Devices development software, go to `http://www.analog.com/processors/tools/`.

Product Overview

The Blackfin A-V EZ-Extender is a separately sold extension board that plugs onto the expansion interface of the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite evaluation system. The extension board aids the design and prototyping phases of ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor targeted applications.

The board extends the capabilities of the evaluation system by providing a connection to a video decoder, a video encoder, multiple camera evaluation boards, a flat panel display, and a 3-stereo input channel, 2-stereo output channel audio codec.

The following is a list of the Blackfin A-V EZ-Extender interfaces.

- Analog Audio Interface
  - AD1836A Analog Devices 96 kHz audio codec
  - five 3.5 mm audio jacks, stacked in one connector
- Analog Video Interface
  - ADV7183B video decoder with three input RCA phono jacks
  - ADV7179 video encoder with three output RCA phono jacks
- OmniVision Camera Module Interface
  - Connection to OmniVision Camera Evaluation Modules, for example: OV6630AA
  - 32-pin, right angle, 0.1 in. spacing, female socket
- Micron Camera Module Interface
  - Connection to Micron Camera Evaluation Modules, for example: MT9V022
  - 26-pin, right angle, 0.1 in. spacing, female socket
- Kodak Camera Module Interface
  - Connection to Kodak Camera Evaluation Modules, for example: KAC-9628
  - 28-pin, right angle, 0.1 in. spacing, female socket

- Flat Panel Display Interface
  - Connection to Flat Panel Displays, for example, NL6448BC20-08E
  - DF9B-31S-1V connector

Before using any of the interfaces, follow the setup procedure in "A-V EZ-Extender Setup" on page 1-1.

Example programs are available to demonstrate the capabilities of the Blackfin A-V EZ-Extender board.

Purpose of This Manual

The *Blackfin A-V EZ-Extender Manual* describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Intended Audience

This manual is a user's guide and reference to the Blackfin A-V EZ-Extender. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and development tools are the primary audience for this manual.

Programmers who are unfamiliar with VisualDSP++ or EZ-KIT Lite evaluation software should refer to the *ADSP-BF533*, *ADSP-BF537*, or *ADSP-BF561 Evaluation System Manual*, VisualDSP++ online Help, and user's or getting started guides. For the locations of these documents, refer to "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "A-V EZ-Extender Interfaces" on page 1-1
  Provides basic board information.
- Chapter 2, "A-V EZ-Extender Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the board.
- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-Extender board.
- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the *Blackfin A-V EZ-Extender Manual* located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This is the first edition of the *Blackfin A-V EZ-Extender Manual*.

Technical or Customer Support

You can reach processor Tools Support in the following ways.

- Visit the Embedded Processing and processor products Web site at
  `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to
  `dsptools.support@analog.com`
- E-mail processor questions to
  `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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  One Technology Way
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  Norwood, MA 02062-9106
  USA
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Supported Products

The Blackfin A-V EZ-Extender is designed as an extension board to the ADSP-BF533, ADSP-BF537, and ADSP-BF561 EZ-KIT Lite evaluation systems.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at `www.analog.com`. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
• *ADSP-BF533 Embedded Processor Datasheet* • *ADSP-BF536/ADSP-BF537 Embedded Processor Datasheet* • *ASP-BF561 Blackfin Embedded Symmetric Multi-Processor Datasheet*	General functional description, pinout, and timing.
• *ADSP-BF533 Blackfin Processor Hardware Reference* • *ADSP-BF537 Blackfin Processor Hardware Reference* • *ASP-BF561 Blackfin Processor Hardware Reference*	Description of internal processor architecture and all register functions
Blackfin Processor Instruction Set Reference	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
• *ADSP-BF533 EZ-KIT Lite Evaluation System Manual* • *ADSP-BF537 EZ-KIT Lite Evaluation System Manual* • *ADSP-BF561 EZ-KIT Lite Evaluation System Manual*	Description of the EZ-KIT Lite features and usage. Note: For the ADSP-BF537 EZ-KIT Lite, there is additional *Getting Started with ADSP-BF537 EZ-KIT Lite*.
VisualDSP++ User's Guide	Description of VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manual	Description of the assembler function and commands
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands
VisualDSP++ Loader Manual	Description of the loader function and commands

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 A-V EZ-EXTENDER INTERFACES

After a setup procedure for a custom system utilizing the Blackfin A-V EZ-Extender, a ADSP-BF533, ADSP-BF537 or ADSP-BF561 EZ-KIT Lite, and an evaluation module, the chapter describes each of the evaluation interfaces the extender supports.

The information is presented in the following order.

A-V EZ-Extender Setup

It is very important to set up all of the components of the system containing the A-V EZ-Extender before applying power to that system. The following procedure is recommended for the correct setup.

Power your system when these steps are completed:

1. Read the applicable design interface section in this chapter—the text provides an overview of the capabilities of the interface.
2. Read "System Architecture" on page 2-2 to understand the physical connections of the extension board. For detailed information, refer to "Schematics on page B-1".

3. Set the jumpers on A-V EZ-Extender board. Use the block diagram in Figure 2-1 on page 2-3 in conjunction with "Jumpers" on page 2-7.
4. Set the switches and jumpers on EZ-KIT Lite board. If not already, familiarize yourself with the documentation and schematics of the EZ-KIT Lite (see "Related Documents" on page -xiv). Compare the expansion interface signals of the A-V EZ-Extender board with the signals of the EZ-KIT Lite board to ensure there is no contention. For example, it may be necessary to disable other devices connected to the Parallel Peripheral Interface (PPI) of the processor, change the routing of the PPI clocks, and disable the push buttons.
5. Configure any other interfacing boards, for example, another EZ-Extender or camera evaluation board.

Analog Audio Interface

For an audio application, the A-V EZ-Extender uses the AD1836A multichannel 96 kHz audio codec. The AD1836A is a high-performance, single-chip codec that provides three stereo digital-to-analog converters (outputs) and two stereo analog-to-digital converters (inputs) using ADI's patented multi-bit sigma-delta architecture. The board includes an SPI port, allowing the processor to adjust volume and other parameters. For a general overview of the audio interface connections, see Figure 2-1 on page 2-3. For more detailed information, see "Schematics on page B-1".

SPORT0 of the expansion interface interfaces with the serial port of the AD1836A codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or I^2S mode. The I^2S mode allows the codec to operate at a 96 kHz sample rate but allows only two channels of output. TDM mode can operate at a maximum of 48 kHz

sample rate but allows simultaneous use of all input and output channels. To operate in I^2S mode, the JP7.1/2 jumper must be installed. For more information, see "I2S Enable Jumper (JP7.1/2)" on page 2-13.

The internal registers of the AD1836A audio codec can be programmed via the SPI port of the processor. (For information on how to program the configuration registers, refer to the AD1836A datasheet.) The AD1836A codec reset comes either from a flag pin located at PPI1_D11 of the expansion interface or from the EZ-KIT Lite reset signal. For information on how to configure the reset, see "AV_RESET Source Jumper (JP9.1/3/5)" on page 2-14.

Before using the interface, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Example programs demonstrating the capabilities of the audio interface are included in the A-V EZ-Extender installation directory.

For more information about AD1836A, go to http://www.analog.com and search for AD1836A.

Analog Video Interface

The A-V EZ-Extender supports video input and output applications with an on-board video encoder and decoder. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183B video decoder provides up to three input channels of analog video. Both the encoder and the decoder connect to the PPI0 of the expansion interface, while the encoder also can connect to the PPI1 (if the processor has two PPI ports). For a general overview of the analog video interface connectors, see Figure 2-1 on page 2-3. For more detailed information, see "Schematics on page B-1".

To use ADV7179 and ADV7183B, set up all of the jumpers related to the PPI data signals, frame sync signals, and clock signal. To program the internal register of the video devices, configure the Two Wire Interface signals (see "TWI Source Selection Jumpers (JP3.3/5/7, JP3.4/6/8)" on page 2-7). Finally, determine the source of the encoder or decoder reset (see "AV_RESET Source Jumper (JP9.1/3/5)" on page 2-14.)

Before using the interface, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Example programs demonstrating the capabilities of the analog video interface are included in the A-V EZ-Extender installation directory.

For more information about ADV7179 and ADV7183B, go to `http://www.analog.com` and search for `ADV7179` or `ADV7183B`.

Camera Module Interfaces

The A-V EZ-Extender has three right-angle connectors (`J4`, `J6`, and `P4`) with the control signals necessary to interface with three different manufactures camera evaluation modules. For a general overview of the camera module interface connections, see Figure 2-1 on page 2-4. For more detailed information, see "Schematics on page B-1". Figure 1-1 shows the orientation of the camera modules, as each camera connects to the board.

The `J6` connector is designated for a Micron camera sensor evaluation module. The interface has been tested with the Micron MT9V022 camera evaluation module. For information about Micron camera sensors and evaluation boards, go to `http://www.micron.com`.

The `J4` connector is designated for an OmniVision camera sensor evaluation module. The interface has been tested with the OmniVision OV6630AA camera evaluation module. For information about OmniVision camera sensors and evaluation boards, go to `http://www.ovt.com`.

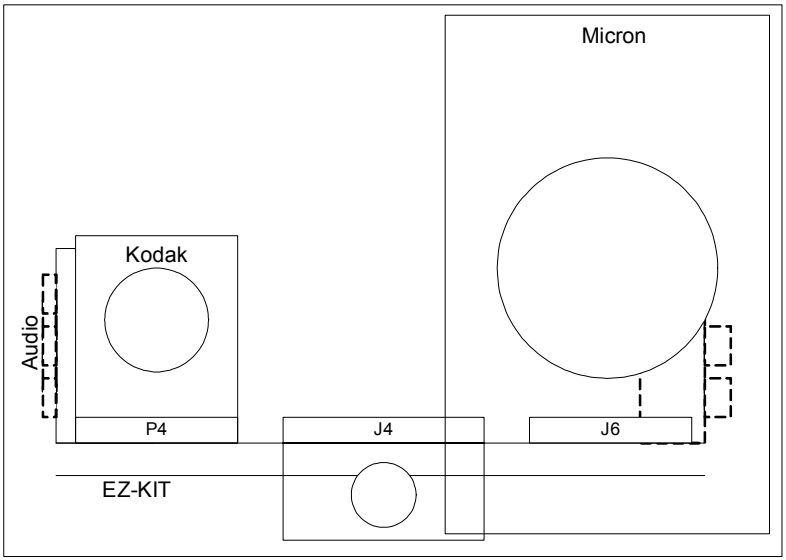


Figure 1-1. Camera Orientation

The P4 connector is designated for a Kodak camera sensor evaluation module. The interface has been tested with the Kodak KAC-9628 camera evaluation module. For information about Kodak camera sensors and evaluation boards, go to http://www.kodak.com.

To connect the Blackfin A-V EZ-Extender to a camera module, first determine the source of the PPI clock. To learn about possible clock settings, refer to "PPI Clock Setup Jumpers (JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8)" on page 2-10. Then set the direction of the data and the frame sync signals, which depend upon the camera's configuration. The data must be set as an input to the PPI port. For more information, refer to "System Architecture" on page 2-2 and "Jumpers" on page 2-7.

Before using these interfaces, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Example programs demonstrating the capabilities of the camera module interface are included in the A-V EZ-Extender installation directory.

Flat Panel Display Interface

The Flat Panel Display (FPD) interface consists of a 31-pin, DF9 connector linked to the PPI port and frame sync signals of the processor. For a general overview of the display interface connections, see Figure 2-1 on page 2-4. For more detailed information, see the "Schematics on page B-1".

A timing and functional analysis is required to determine if a specific LCD module can connect to the Blackfin A-V EZ-Extender. An example of a display that can connect to the extender is the NEC NL6448BC20-08 display (http://www.ee.nec.de/).

Please note that the power for the backlight feature of the LCD module must be provided by the customer (use the backlight inverter recommended by the manufacturer). It is also necessary to purchase a cable to connect the A-V EZ-Extender to the display. An example of such a cable is FDC31/xxxxAFF03 from Axon Cable (http://www.axon-cable.com, part number FDC31/xxxxAFF03). Different length cables are available.

Before using the interface, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Example programs demonstrating the capabilities of the flat panel display interface are included in the A-V EZ-Extender installation directory.

2 A-V EZ-EXTENDER HARDWARE REFERENCE

This chapter describes the hardware design of the A-V EZ-Extender.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the extension board and explains how the board components interface with the processor and EZ-KIT Lite.
- "Jumpers" on page 2-7
  Describes the function of the configuration jumpers.

System Architecture

A block diagram of the Blackfin A-V EZ-Extender is shown in Figure 2-1.

Not shown in the diagram is the analog audio interface, which is a simple connection between the serial port of the processor and the AD1836A audio codec. The audio interface connects directly to SPORT0 of the expansion interface.

In Figure 2-1, unidirectional buffers are show as triangle symbols, while bidirectional buffers are shown as two overlapping triangles. For both types of buffers, the output-enable signal comes out of the top and is active LOW. For the bidirectional buffers, a second signal for the direction is shown. When this net is pulled HIGH, the buffer is driving in the direction of the arrow in the center, when LOW, the buffer is driving in the opposite direction.

Before applying power to the system, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Video interfaces can be split into two main signal sets: VID_IN and VID_OUT. Both signal sets consist of a 16-bit data bus, two frame sync signals, and data clock. VID_IN connects to the video decoder and all of the camera interfaces. VID_IN connects only to PPI0 of the EZ-KIT Lite. VID_OUT connects to the video encoder and the flat panel display interface. On the expansion interface, VID_OUT connects to either PPI0 or PPI1 of the EZ-KIT Lite.

Table 2-1 summarizes the signals coming and going on the expansion interface connectors.

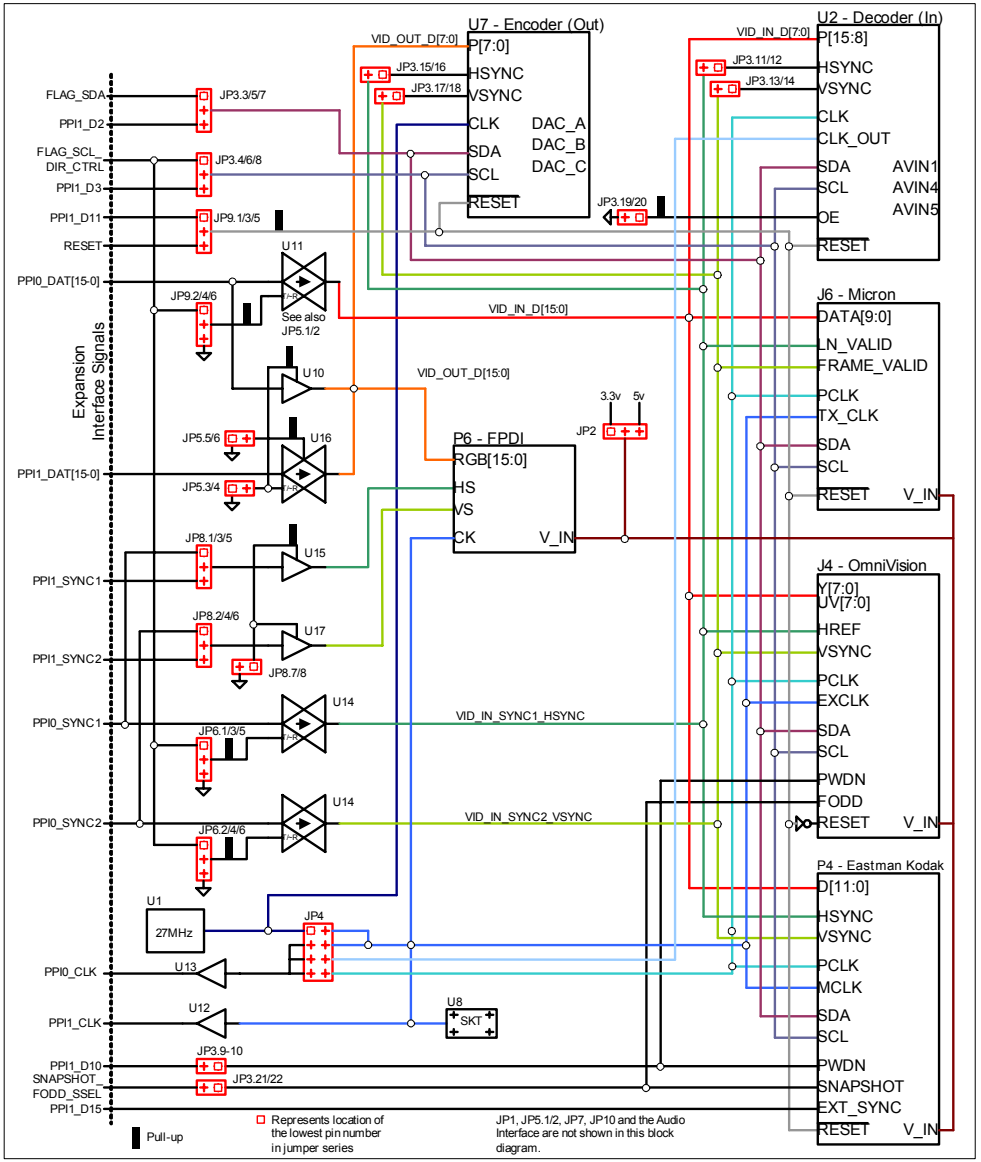

U7 - Encoder (Out)
P[7:0]
HSYNC
VSYNC
CLK
SDA
SCL
RESET
DAC_A
DAC_B
DAC_C
VID_OUT_D[7:0]
JP3.15/16
JP3.17/18
U2 - Decoder (In)
P[15:8]
HSYNC
VSYNC
CLK
CLK_OUT
SDA
SCL
OE
RESET
AVIN1
AVIN4
AVIN5
VID_IN_D[7:0]
JP3.11/12
JP3.13/14
JP3.19/20
FLAG_SDA
PPI1_D2
FLAG_SCL_
DIR_CTRL
PPI1_D3
PPI1_D11
RESET
JP3.3/5/7
JP3.4/6/8
JP9.1/3/5
PPI0_DAT[15-0]
JP9.2/4/6
See also
JP5.1/2
U11
U10
VID_IN_D[15:0]
VID_OUT_D[15:0]
Expansion
Interface Signals
JP5.5/6
JP5.3/4
U16
PPI1_DAT[15-0]
P6 - FPDI
RGB[15:0]
HS
VS
CK
V_IN
3.3v
5v
JP2
J6 - Micron
DATA[9:0]
LN_VALID
FRAME_VALID
PCLK
TX_CLK
SDA
SCL
RESET
V_IN
JP8.1/3/5
U15
PPI1_SYNC1
JP8.2/4/6
U17
PPI1_SYNC2
JP8.7/8
J4 - OmniVision
Y[7:0]
UV[7:0]
HREF
VSYNC
PCLK
EXCLK
SDA
SCL
PWDN
FODD
RESET
V_IN
PPI0_SYNC1
U14
JP6.1/3/5
VID_IN_SYNC1_HSYNC
PPI0_SYNC2
U14
JP6.2/4/6
VID_IN_SYNC2_VSYNC
P4 - Eastman Kodak
D[11:0]
HSYNC
VSYNC
PCLK
MCLK
SDA
SCL
PWDN
SNAPSHOT
EXT_SYNC
RESET
V_IN
U1
27MHz
JP4
PPI0_CLK
U13
U12
PPI1_CLK
U8
SKT
JP3.9-10
JP3.21/22
PPI1_D10
SNAPSHOT_
FODD_SSEL
PPI1_D15
Pull-up
Represents location of
the lowest pin number
in jumper series
JP1, JP5.1/2, JP7, JP10 and the Audio
Interface are not shown in this block
diagram.

Table 2-1. Signals of Expansion Interface Connectors

Net/Bus Name (Direction)	A-V EZ-Extender Function	Relevant Configuration Jumpers
PPI0_D[0:15] (Bi)	Connects the processor's PPI0 data pins to the VID_IN_D[0:15] or the VID_OUT_D[0:15] busses, depending on the jumper settings. This allows PPI0 to interface with all of the possible video interfaces on the board. This bus can be bidirectional, where the direction can be fixed with a jumper or controlled by a flag pin.	JP5.3/4, JP9.2/4/5
PPI0_CLK (Output)	The clock related to the data on PPI0. This can come from an onboard oscillator, from one of the video interfaces, or from a socket that allows a user-supplied oscillator.	JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8
PPI0_SYNC1 (Bi)	The frame sync signal going to the processor's PPI0_SYNC1 pin. The signal behaves as the HSYNC or HREF for the video interfaces. The signal also can be used to drive the FPDI HS signal. The signal can be bidirectional, where the direction is fixed with a jumper or is controlled by a flag pin.	JP6.1/3/5, JP8.1/3/5, JP8.7/8
PPI0_SYNC2 (Bi)	The frame sync signal going to the processor's PPI0_SYNC2 pin. The signal behaves as the VSYNC or VREF for the video interfaces. The signal also can be used to drive the FPDI VS signal. This signal can be bidirectional, where the direction can be fixed with a jumper or is controlled by a flag pin.	JP6.2/4/6, JP8.2/4/6, JP8.7/8
PPI1_D[0:15] (Bi)	Connects the processors PPI1 data pins to the VID_OUT_D[0:15] bus. The VID_OUT_D[0:15] bus interfaces with the output video interfaces (FPDI and the video encoder). The bus can be bidirectional but intended to be an input. Changing the direction is necessary only for test purposes and allows PPI0 to loop-back to PPI1. D2, D3 and D10 of the bus have other functionality (see below).	JP5.3/4, JP5.5/6, JP3.9/10, JP3.3/5/7 JP3.4/6/8
PPI1_D10 (Bi)	Multifunction net that typically functions as the D10 pin of PPI1 but, with a jumper, also can connect to the PDWN input of the OmniVision interface and the Kodak interface.	JP3.9/10, JP5.3/4, JP5.5/6

Table 2-1. Signals of Expansion Interface Connectors (Cont'd)

Net/Bus Name (Direction)	A-V EZ-Extender Function	Relevant Configuration Jumpers
PPI1_D2 (Bi)	Multifunction net typically functions as the D2 pin of PPI1 but also can function as the data signal for the processor's Two Wire Interface (TWI). Used to program the internal configuration registers of most video interfaces.	JP3.3/5/7, JP5.3/4, JP5.5/6
PPI1_D3 (Bi)	Multifunction net typically functions as the D2 pin of PPI1 but also can function as the data signal for the processor's TWI. Used to program the internal configuration registers of most video interfaces.	JP3.4/6/8, JP5.3/4, JP5.5/6
FLAG_SDA (Bi)	In systems whose processor does not have a TWI, the signal connects to one of the processor's flag pins to emulate the data pin of the TWI and to configure the internal configure registers of most video interfaces.	JP3.3/5/7
FLAG_SCL_DIR_CTRL (Input)	In systems whose processor does not have a TWI, the signal connects to one of the processor's flag pins to emulate the clock signal of the TWI and to configure the internal configure registers of most video interfaces.	JP3.4/6/8
PPI1_CLK (Output)	The clock driving the EZ-KIT Lite's PPI1 clock input. The source of this clock can be the PPIO_CLK, the onboard 27 MHz oscillator, or a socket accepting oscillators of other frequencies.	JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8
PPI1_FS1 (Input)	The signal driven to the HS signal of the FPDI. The output going to the FPDI can be disabled by a jumper.	JP8.1/3/5, JP8.7/8
PPI1_FS2 (Input)	The signal driven to the VS signal of the FPDI. The output going to the FPDI can be disabled by a jumper.	JP8.2/4/6, JP8.7/8
SNAPSHOT_FODD_SSEL (Bi)	Audio codec SPI slave select signal; also can connect to the SNAPSHOT input of the Kodak interface or the FODD output of the OmniVision interface.	JP3.21/22
SCK (Input)	The SPI serial clock used to program the control register of AD1836A audio codec.	
MOSI (Output)	The SPI serial output data signal used to program the control register of AD1836A audio codec.	

Table 2-1. Signals of Expansion Interface Connectors (Cont'd)

Net/Bus Name (Direction)	A-V EZ-Extender Function	Relevant Configuration Jumpers
MISO (Output)	The SPI serial input data signal used to read the control register of the AD1836A audio codec.	
RSCLK0 (Bi)	Processor's SPORT0 receive clock signal connected to the serial clock on the digital side of the audio codec analog input. In I^2S mode, the signal can connect to the TSCLK0 net.	JP7.1/2
RFS0 (Bi)	Processor's SPORT0 receive frame sync signal connected to the frame sync on the digital side of the audio codec analog input. In I^2S mode, the signal can connect to the TFS0 net.	JP7.1/2
DR0PRI (Output)	Connection to the data output of the audio codec. Can be disconnected with a jumper if the signal is needed for another purpose.	JP7.3/4
DR0SEC (Output)	Secondary connection to the data output of the audio codec. Can be disconnected with a jumper if the signal is needed to be used for another purpose.	JP7.5/6
TSCLK0 (Bi)	Processor's SPORT0 transmit clock signal. Connects to the serial clock on the digital side of the audio codec's analog output. In I^2S mode, the signal can connect to the RSCLK0 net.	JP7.1/2
TFS0 (Bi)	Processor's SPORT0 transmit frame sync signal. Connects to the frame sync on the digital side of the audio codec analog output. In I^2S mode, the signal can connect to the RFS0 net.	JP7.1/2
DT0PRI (Input)	Connection to the data input of the audio codec.	
DT0SEC (Input)	Secondary connection to the data input of the audio codec.	

Jumpers

Before using the Blackfin A-V EZ-Extender, follow the steps in "A-V EZ-Extender Setup" on page 1-1.

Figure 2-2 shows the locations of all of the jumper headers. The jumper headers are divided to show the placement and rotation of each jumper. The jumpers are described by the pins of the header on which the jumpers can be placed. For example, JP3.4/6/8 refers to a single jumper that can be placed across pins 4 and 6, or pins 6 and 8, of JP3. The dark pin indicates pin 1 of each header.

Video Test Loopback Jumpers (JP1.1/2, JP1.3/4, JP1.5/6)

For test purposes only, the video test jumpers are used to loop-back the video encoder's output signals to the video decoder's input signals. By default, none of these jumpers are installed.

Connector Voltage Selection Jumper (JP2)

The camera module and LCD display interfaces can be powered via the extender. The actual voltage of these interfaces, 3.3V or 5V, is determined by the placement of the JP2 jumper (see Table 2-2).

TWI Source Selection Jumpers (JP3.3/5/7, JP3.4/6/8)

Due to the fact that some Blackfin processors feature a built-in Two Wire Interface (TWI), while others need to emulate the interface with programmable flags, the two jumpers are provided to plug on the A-V EZ-Extender to both sources (see Table 2-3).

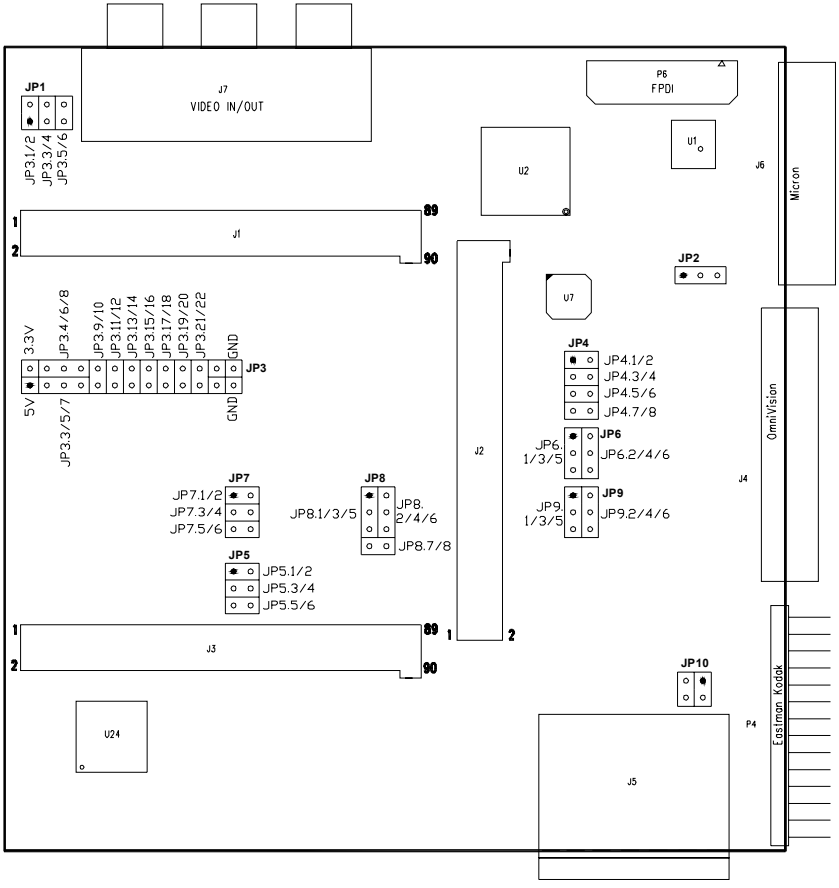


Figure 2-2. Jumper Locations

Table 2-2. Jumper Locations and their Connector Voltages

Jumper Location	Connector Voltage
JP2.1/2	3.3V
JP2.2/3	5V
Not installed	No power

Table 2-3. Jumper Locations and TWI Interface Sources

Jumper Pin Locations	TWI Interface Source
JP3.3/5 and JP3.4/6	Programmable Flags
JP3.5/7 and JP3.6/8	Processor's TWI

PDWN Connection Jumper (JP3.9/10)

Depending on the application, the PDWN pin of the OmniVision and Kodak cameras can be left floating or can be controlled by a flag pin (see Table 2-4).

Table 2-4. PWDN Pin Connections

JP3.9/10	PDNW Connection
Uninstalled	PDWN is not used, and by default, the cameras function in standard mode.
Installed	The PDWN functionality of the cameras is controlled by a processor flag pin.

Decoder HSync Disconnect Jumper (JP3.11/12)

To connect the horizontal sync signal of the video decoder to the PPI0 frame sync signal of the processor, install the JP3.11/12 jumper; otherwise, the decoder's horizontal sync is disconnected.

Decoder VSync Connection Jumper (JP3.13/14)

To connect the vertical sync signal of the video decoder to the PPI0 frame sync signal of the processor, install the JP3.13/14 jumper; otherwise, the decoder's vertical sync is disconnected.

Encoder HRef Connection Jumper (JP3.15/16)

To connect the horizontal sync signal of the video encoder to the PPI0 frame sync signal of the processor, install the JP3.15/16 jumper; otherwise, the encoder's horizontal reference is disconnected.

Encoder VSync Connection Jumper (JP3.17/18)

To connect the vertical sync signal of the video encoder to the PPI0 frame sync signal of the processor, install the JP3.17/18 jumper; otherwise, the encoder's vertical sync is disconnected.

Decoder Output Enable Jumper (JP3.19/20)

When installed, the JP3.19/20 jumper enables the video decoder's data output signals on the VID_IN bus.

SNAPSHOT_FODD Disconnect Jumper (JP3.21/22)

The SNAPSHOT_FODD net of the A-V EZ-Extender is a general-purpose flag pin. The flag pin connects to both the SNAPSHOT signal of the Kodak camera evaluation board and the FODD control signal of the OmniVision camera evaluation board. Do not install the jumper unless the processor needs to control the signals. The flag pin also connects to the SPI select pin of the AD1836A audio codec—when the audio interfaces is being used, do not install this jumper.

PPI Clock Setup Jumpers (JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8)

The PPI_CLK signals of PPI0 and PPI1 are setup using the clock setup jumpers. Table 2-5 shows the results of the jumper connections. For more information about the clock settings, refer to Figure 2-1 on page 2-4.

Table 2-5. Jumper Results

Jumper	Result
JP4.1/2	Connects EXT_VID_CLK to an onboard 27 MHz oscillator. For more information about the EXT_VID_CLK signal, see the description of JP4.3/4.
JP4.3/4	Connects PPI0_CLK to the EXT_VID_CLK net. The EXT_VID_CLK net is the external clock, which drives the input clock of all the camera module interface connectors, plus the flat panel display connector. Depending on the installation of the other JP4 jumpers, EXT_VID_CLK can be generated by the PIXEL_CLK net, the VDEC_CLKOUT net, a socket (U8), or the onboard 27 MHz oscillator.
JP4.5/6	Connects VDEC_CLKOUT to PPI0_CLK. VDEC_CLKOUT drives the PPI0 clock when the video decoder is used.
JP4.7/8	Connects the PIXEL_CLK net, which is an output from the three camera module interfaces, to PPI0_CLK.

PPI0 D8–15 Enable Jumper (JP5.1/2)

The JP5.1/2 jumper, when not installed, disables the upper 8-bits of the PPI0 data bus. This allows the signals connected to the upper 8-bits of the PPI data bus on the EZ-KIT Lite to be used for another purpose.

To disable and reuse the upper 8-bits of the VID_IN and PPI0 data busses, install the JP5.1/2 jumper.

VID_OUT Data Bus Control Jumpers (JP5.3/4, JP5.5/6)

The JP5.3/4 and JP5.5/6 jumpers are used together to set the direction of as well as to enable or disable the drivers driving the VID_OUT data bus. Table 2-6 shows the results of different combinations of the JP5.3/4 and JP5.5/6 jumpers.

Table 2-6. Jumper Combinations

JP5.3/4	JP5.5/6	VID_OUT Status
Uninstalled	Uninstalled	VID_OUT, PPI1 are all not driven; PPI0 depends on the state of JP9.2/4/6
Uninstalled	Installed	PPI1 drives VID_OUT
Installed	Uninstalled	PPI0 drives VID_OUT
Installed	Installed	PPI0 drives VID_OUT, and VID_OUT drives PPI1 (loopback mode)

PPI0_SYNC1 Direction Setup Jumper (JP6.1/3/5)

The direction of the PPI0_SYNC1 signal can be either fixed or programmed, depending on the state of a general-purpose flag. Table 2-7 shows how to set the direction of PPI0_SYNC1.

Table 2-7. Setting Direction of PPI0_SYNC1 (JP6.1/3/5)

Jumper Location	PPI0_SYNC1 Direction
JP6.1/3	Controlled by flag pin
JP6.3/5	Input to processor
Uninstalled	Output from processor

PPI0_SYNC2 Direction Setup Jumper (JP6.2/4/6)

The direction of the PPI0_SYNC2 signal can either be fixed or programmed, depending on the state of a general-purpose flag. Table 2-8 shows how to set the direction of PPI0_SYNC2.

Table 2-8. Setting Direction of PPI0_SYNC2 (JP6.2/4/6)

Jumper Location	PPI0_SYNC2 Direction
JP6.2/4	Controlled by flag pin
JP6.4/6	Input to processor
Uninstalled	Output from processor

I²S Enable Jumper (JP7.1/2)

When the JP7.1/2 jumper is installed, the SPORT signals are routed for I²S SPORT communication protocol mode. To accomplish this, the receive and transmit clocks of the processor are routed to be driven by the output clock of the AD1836A. The same is done for the frame sync signals.

SPORT Data Connection Jumpers (JP7.3/4, JP7.5/6)

The JP7.3/4 and JP7.5/6 jumpers connect data output pins (ASDATA1 and ASDATA2) of the audio codec to the primary and secondary SPORT data input pins of the processor. The audio codec is driving these pins—with the help of the JP7.3/4 and JP7.5/6 jumpers, the processor's pins can be reused when the audio codec is not used.

VID_OUT Bus Sync Source Select Jumpers (JP8.1/3/5, JP8.2/4/6)

The source of the PPI frame sync signals depends on the PPI port driving the VID_OUT bus. When using PPI0, place the jumpers at JP8.1/3 and JP8.2/4. When using PPI1, place the jumpers at JP8.3/5 and JP8.4/6.

VID_OUT Bus Sync Enable Jumper (JP8.7/8)

To enable the VID_OUT frame sync signals, install the JP8.7/8 jumper.

AV_RESET Source Jumper (JP9.1/3/5)

The source of the ICs reset on the A-V EZ-Extender is controlled by either a flag pin or a system reset, the latter also resetting the Blackfin processor (see Table 2-9).

Table 2-9. Jumper Reset Sources

Jumper Location	Reset Source
JP9.1/3	Flag pin multiplexed with PPI1_D11
JP9.3/5	System reset generator
Uninstalled	ICs are not reset

PPI0_D Direction Setup Jumper (JP9.2/4/6)

The direction of the PPI0_D[15:0] signal can be a fixed direction or can be programmed, depending on the state of a general-purpose flag. Table 2-10 shows how to set the direction of PPI0_D[15:0].

Table 2-10. Setting Direction of PPI0_D[15:0] (JP9.2/4/6)

Jumper Location	PPI0_D[15:0] Direction
JP9.2/4	Controlled by flag pin
JP9.4/6	Input to processor
Uninstalled	Output from processor

Audio Loopback Jumpers (JP10.1/2, JP10.3/4)

The JP10.1/2 and JP10.3/4 jumpers loop back the audio input to the output for test purposes and should not be installed.

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	57	0.1UF 16V 10%603	C1,C4,C7–8,C10–15,C17, C19	AVX	0603YC104KAT2A
2	6	2200pF 50V 5% 0603	C102,C113–114,C116, C140,C142	PANASONIC	ECJ–1VB1H222K
3	12	330PF 50V 5% 0603	C18,C20–21,C28,C31,C35, C98	AVX	06035A331JAT2A
4	11	0.01UF 16V 10% 0603	C2–3,C6,C16,C25,C29,C36, C41	KEMET	
5	2	1UF 16V 10% 0603	C27,C39	PANASONIC	ECJ–1VB1C105K
6	5	10UF 10V +80/–20% 0805	C42,C45,C59,C79–80	PANASONIC	ECJ–2FF1A106Z
7	1	82NF 50V 5% 805 X7R	C5	AVX	08055C823JAT2A
8	8	120PF 50V 5% 0603	C71,C74,C82–83,C127–128, C141	PANASONIC	ECJ–1VC1H121J
9	8	0.22uF 25V 10% 805 CERM	C73,C85,C101,C112, C120–121	AVX	08053C224FAT
10	12	100PF 50V 5% 0603	C77,C91–92,C97,C105–106, C109	PANASONIC	ECJ–1VC1H101J
11	6	680pF 50V 5% 0603	C84,C88–90,C122–123	PANASONIC	ECJ–1VC1H681J

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
12	6	220PF 50V 5% 0603	C87,C94–96,C125–126	PANASONIC	ECJ–1VC1H221J
13	10	0.001UF 50V 5% 0603	C9,C24,C72,C86,C93,C100, C103	PANASONIC	ECJ–1VC1H102J
14	6	10uF 16V 10% B TANT	CT1–4,CT12–13	AVX	TAJB106K016R
15	10	10uF 16V 20% CAP002 ELEC	CT5–11,CT14–16	DIG01	PCE3062TR–ND
16	1	10MA AD1580BRT SOT23D 1.2V–SHUNT–REF	D1	ANALOG DEVICES	AD1580BRT
17	4	600 100MHZ 500MA 1206 0.70 BEAD	FER1–3,FER9	DIGIKEY	240–1019–1–ND
18	5	600 100MHZ 200MA 603 0.50 BEAD	FER4–8	MURATA	BLM11A601SPT
19	3	0.05 45X2 CON019 SMT SOCKET	J1–3	SAMTEC	SFC–145–T2–F–D–A
20	1	IDC 16X2 IDC16X2RASOC SOCKET RA	J4	SAMTEC	SSW–116–02–F–D–RA
21	1	3.5MM 5xAUDIO_JACK CON035 5X 3.5MM AUDIO JACK	J5	FOXCONN	JA33331–R55

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
22	1	IDC 13x2RA IDC13x2_F_RA 13x2 IDC RA FEMALE	J6	SAMTEC	SSW–113–02–F–D–RA
23	1	RCA 3X2 CON024 RA	J7	SWITCHCRAFT	PJRAS3X2S01
24	5	IDC 3X2 IDC3X2_SMT	JP1,JP5–7,JP9	SAMTEC	TSM–103–01–T–DV
25	1	IDC 2X2 IDC2X2 GOLD	JP10	DIGI–KEY	S2011–02–ND
26	1	IDC 3X1 IDC3X1 GOLD	JP2	DIGI–KEY	S1011–03–ND
27	1	IDC 13X2 IDC13X2_M_SMT	JP3	SAMTEC	TSM–113–01–T–DV
28	2	IDC 4X2 IDC4X2_M_SMT	JP4,JP8	SAMTEC	TSM–104–01–T–DV
29	6	0.68UH 0.72 10% 805	L1–3,L7–9	MURATA	LQG21NR68K10T1
30	3	2.2UH 0.63 10% 805	L4–6	MURATA	LQG21N2R2K10
31	1	GREEN–SMT LED001 GULL–WING	LED1	PANASONIC	LN1361C
32	3	0.05 45x2 CON018 HEADER	P1–3	SAMTEC	TFC–145–32–F–D

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
33	1	IDC 14x2RA IDC14x2_M_RA 14X2 IDC RA MALE	P4	SULLINS	PTC14DBAN
34	1	FPDI 31PIN CON034 FLAT PANEL DISP CON- NECTOR	P6	HIROSE	DF9–31P–1V
35	1	1.5K 100MW 5% 805	R1	AVX	CR21–1501F–T
36	12	75.0 1/10W 1% 0603 85X	R11–12,R16–17,R21–22, R26–31	DIGI–KEY	9T06031A75R0FBHFT
37	1	680 1/8W 5% 1206	R114	AVX	CR32–681J–T
38	6	1K 1/10W 5% 0603	R13–14,R18–19,R23–24	YAGEO	9C06031A1001JLHFT
39	7	0 1/10W 5% 0603	R15,R20,R25,R111,R115, R130	PHYCOMP	9C06031A0R00JLHFT
40	21	10K 1/10W 5% 0603	R2–4,R10,R32,R37,R44–48, R51	VISHAY	CRCW0603103JRT1
41	1	147K 100MW 1% 805	R36	DIGIKEY	311–147KCCT–ND
42	1	76.8K 100MW 1% 805	R38	DIGIKEY	311–76.8KCCT–ND
43	2	100K 1/10W 5% 0603	R39–40	VISHAY	CRCW0603104JRT1
44	1	150 1/8W 1% 1206	R41	PANASONIC	ERJ–8ENF1500V

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
45	1	1.2K 1/16W 5% 402	R42	PANASONIC	ERJ–2GEJ122X
46	2	33 100MW 5% 805	R49,R52	AVX	CR21–330JTR
47	8	33 1/10W 1% 0603	R5,R8,R33,R68,R142–145	DIG01	311–33.0HTR–ND
48	4	22 1/10W 5% 0603	R50, R146–148	VISHAY	CRCW0603220JRT1
49	2	22 1/10W 5% 805	R53,R55	VISHAY/DALE	CRCW0805220JRT1
50	16	5.76K 1/10W 1% 0603 74B	R61–63,R67,R72–73,R76–77, R105	DIGI–KEY	311–5.76KHTR–ND
51	4	237 1/10W 1% 0603	R64,R70,R106,R110	DIGI–KEY	311–237HTR–ND
52	4	750K 1/10W 1% 0603 85D	R65,R69,R127,R129	DIGI–KEY	311–750KHTR–ND
53	6	2.74K 1/10W 1% 0603 43B	R71,R78–80,R112–113	DIGI–KEY	311–2.74KHTR–ND
54	6	1.65K 1/10W 1% 0603	R74,R84–85,R88,R117–118	DIGI–KEY	311–1.65KHTR–ND
55	12	5.49K 1/10W 1% 0603	R75,R83,R86–87,R89, R99–101	DIGI–KEY	311–5.49KHTR–ND
56	6	3.32K 1/10W 1% 0603 51B	R81,R91–92,R95,R124–125	DIGI–KEY	311–3.32KHTR–ND
57	6	11K 1/10W 1% 0603	R82,R90,R93–94,R123,R126	DIGI–KEY	311–11KHTR–ND

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
58	6	49.9K 1/10W 1% 0603 68C	R96–97,R108–109,R137–138	DIGI–KEY	311–49.9KHTR–ND
59	6	604 1/10W 1% 0603	R98,R102–104,R133,R136	DIGI–KEY	311–604HTR–ND
60	4	22 125MW 5% RNS001	RN1–4	DIGIKEY	744C083220JCT–ND
61	1	27MHZ SMT OSC003	U1	EPSON	SG–8002CA MP
62	1	74LVTH16244MTD TSSOP48 16BIT–BUFFER–DRIVER	U10	FAIRCHILD	74LVTH16244MTD
63	3	74LVTH16245MTD TSSOP48 16BIT–BUFFER–TXRX	U11,U14,U16	FAIRCHILD	74LVTH16245MTD
64	7	SN74LVC1G125 SOT23–5 SINGLE–3STATE–BUFFER	U12–13,U15,U17,U19, U29–30	TI	SN74LVC1G125DBVR
65	1	12.288MHZ SMT OSC003 TS201/21262	U18	DIG01	SG–8002CA–PCC–ND
66	1	ADV7183BKSTZ LQFP80 VID–DECODER	U2	ANALOG DEVICES	ADV7183BKSTZ
67	8	AD8606AR SOIC8 OPAMP	U20–23,U25–28	ANALOG DEVICES	AD8606AR

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
68	1	AD1836AASMQFP52 MULTI–CHANNEL–96KHZ–CODEC	U24	ANALOG DEVICES	AD1836AAS
69	3	AD8061ART SOT23–5 300MHZ–AMP	U3–5	ANALOG DEVICES	AD8061ART–REEL
70	1	SN74LVC1G32 SOT23–5 SINGLE–2 INPUT OR GATE	U6	TI	SN74LVC1G32DBVR
71	1	ADV7179 LFCSP40 VIDEO ENCODER	U7	ANALOG DEVICES	ADV7179KCP
72	1	8 PIN DIP TH–TH CARRIER SOCKETED PIN	U8	MILL–MAX	614–93–308–31–007
73	1	SN74AHC1G00 SOT23–5 SINGLE–2–INPUT–NAND	U9	TI	SN74AHC1G00DBVR
74	1	ADP3336ARM MSOP8 ADJ 500MA REGULATOR	VR1	ANALOG DEVICES	ADP3336ARM–REEL

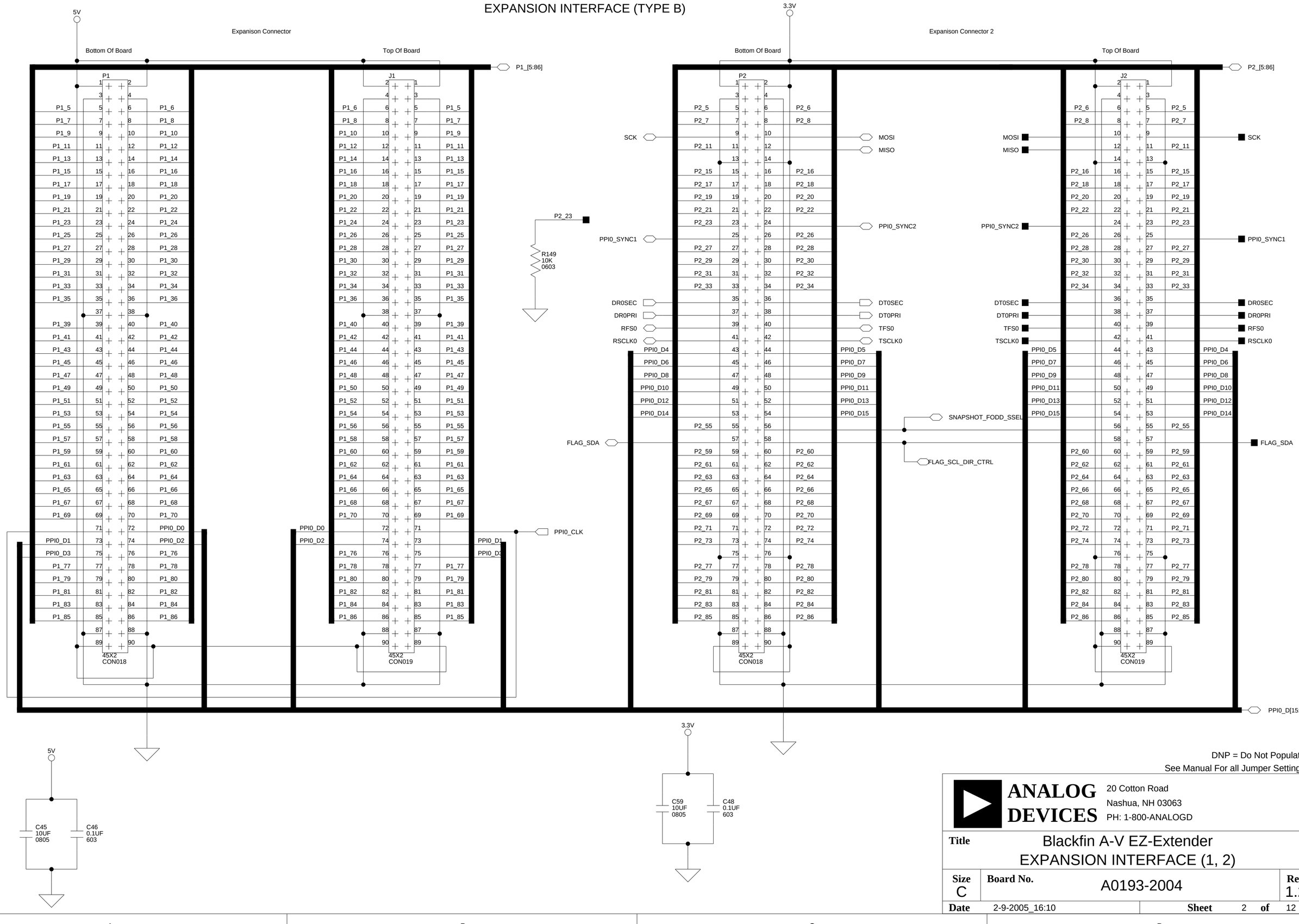
Blackfin A-V EZ-Extender Schematic

DNP = Do Not Populate
See Manual For all Jumper Settings

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender TITLE		
Size C	**Board No.** A0193-2004		**Rev** 1.2
Date 12-1-2004_18:50		**Sheet** 1 **of** 12	

EXPANSION INTERFACE (TYPE B)



DNP = Do Not Populate

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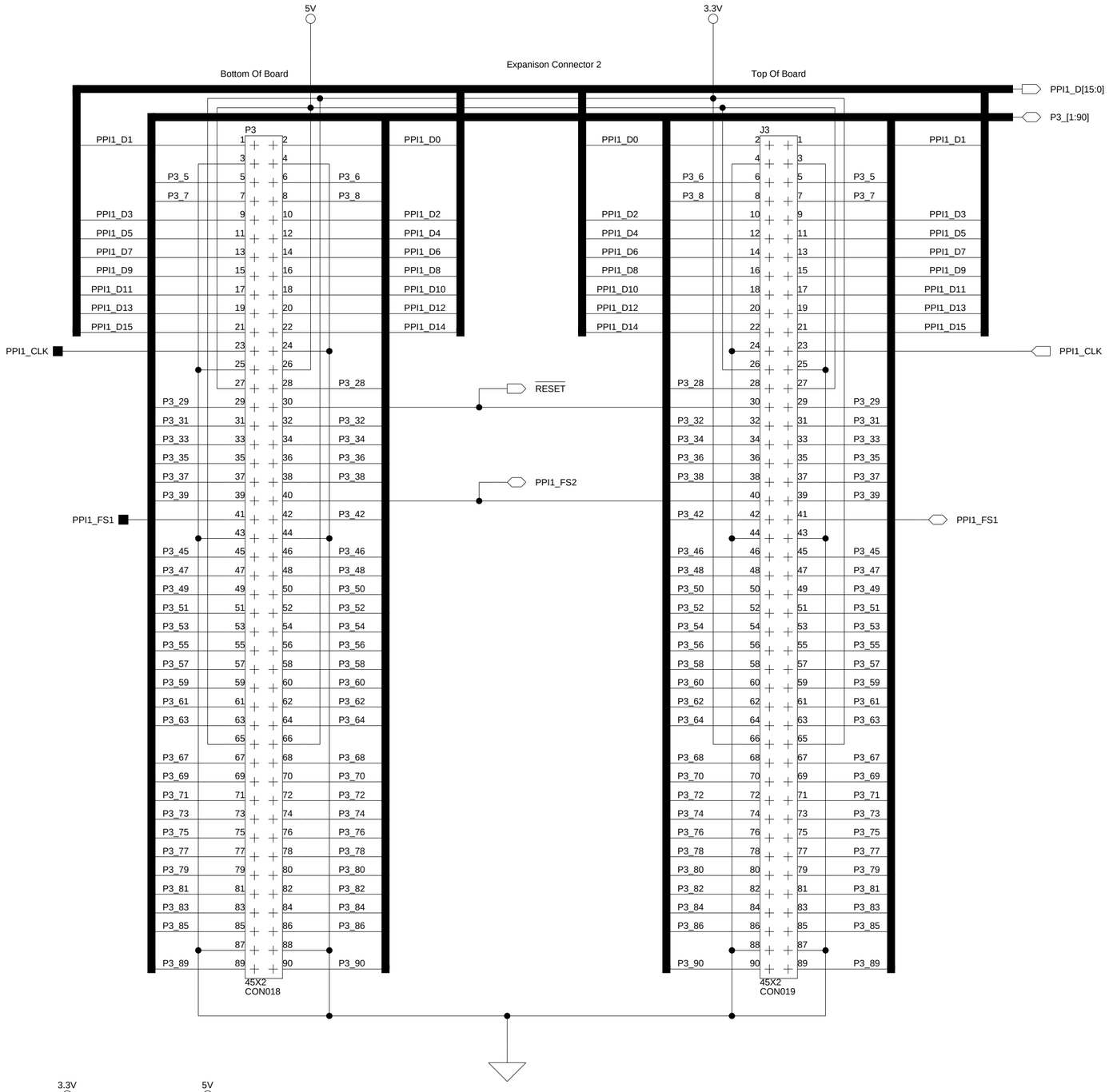
Title	Blackfin A-V EZ-Extender EXPANSION INTERFACE (1, 2)		
Size C	**Board No.** A0193-2004		**Rev** 1.2
Date 2-9-2005_16:10		**Sheet** 2 **of** 12	

EXPANSION INTERFACE (TYPE B)



DNP = Do Not Populate
See Manual For all Jumper Settings

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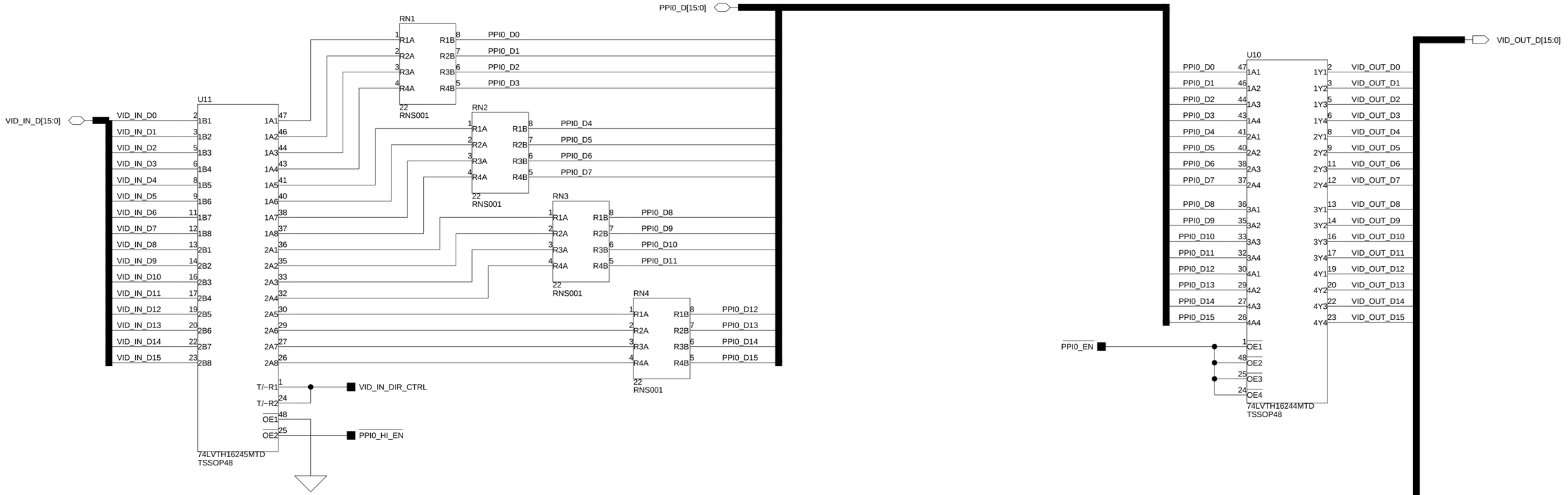
Title	Blackfin A-V EZ-Extender EXPANSION INTERFACE (3)	
Size C	**Board No.** A0193-2004	**Rev** 1.2
Date 1-6-2005_16:35	**Sheet** 3 **of** 12	



DNP = Do Not Populate

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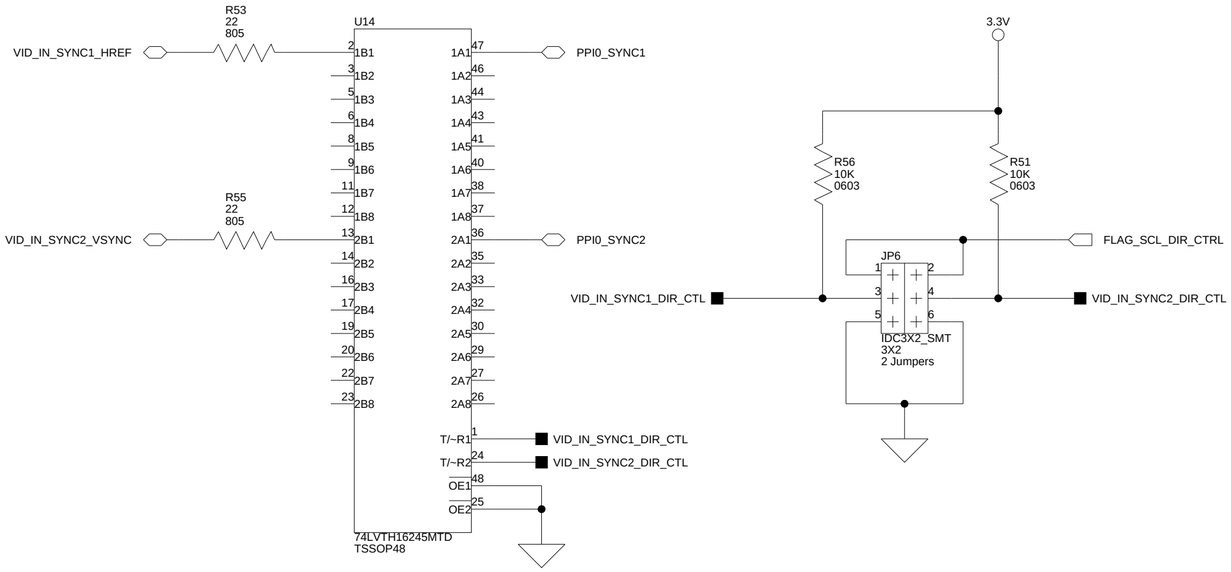
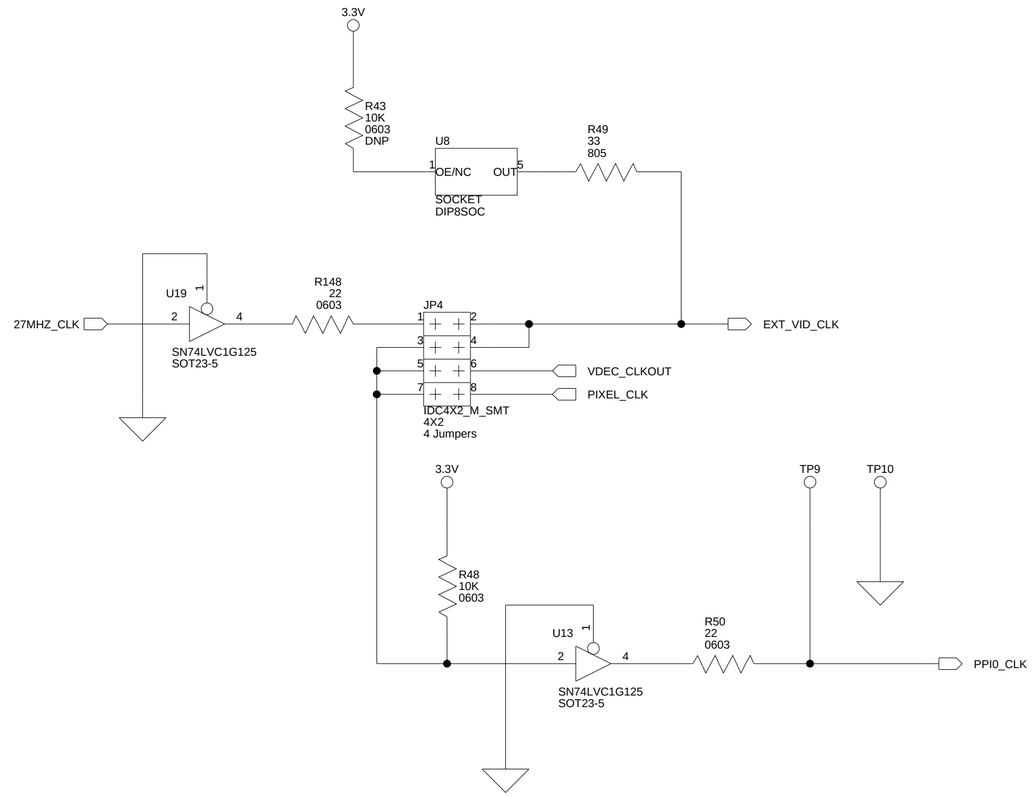
Title	Blackfin A-V EZ-Extender DATA ROUTING		
Size C	**Board No.** A0193-2004		**Rev** 1.2
Date 12-1-2004_14:50		**Sheet** 4 **of** 12	

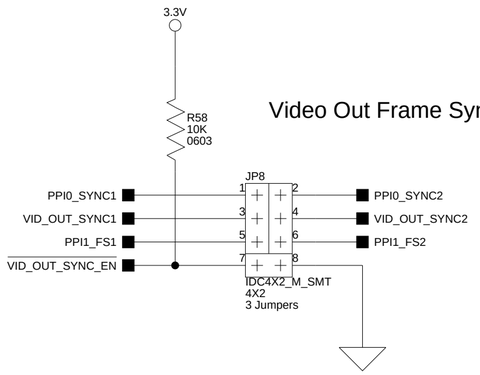
Video In Frame Sync Setup

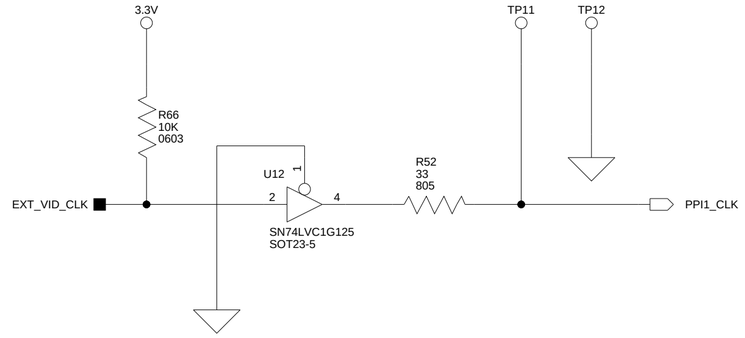


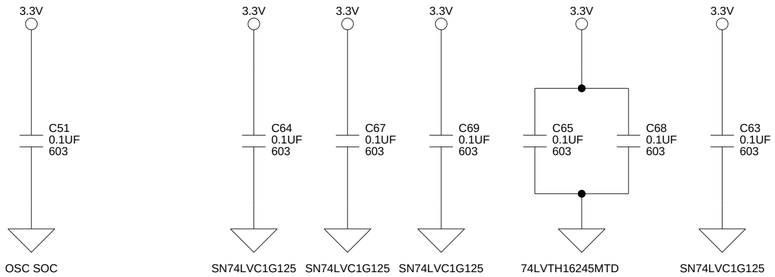
PPI Clock Setup



Video Out Frame Sync Setup







DNP = Do Not Populate
See Manual For all Jumper Settings

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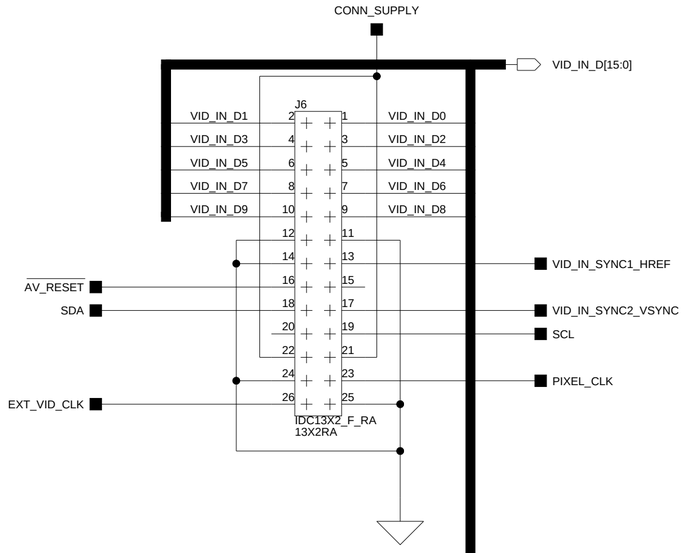
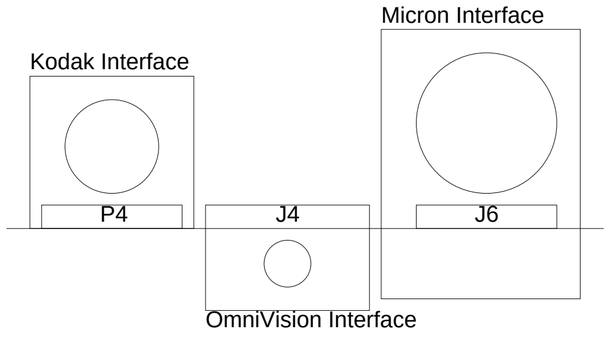
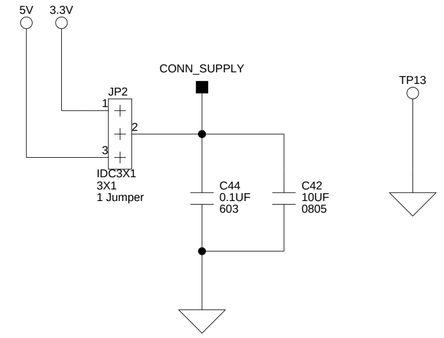
PH: 1-800-ANALOGD

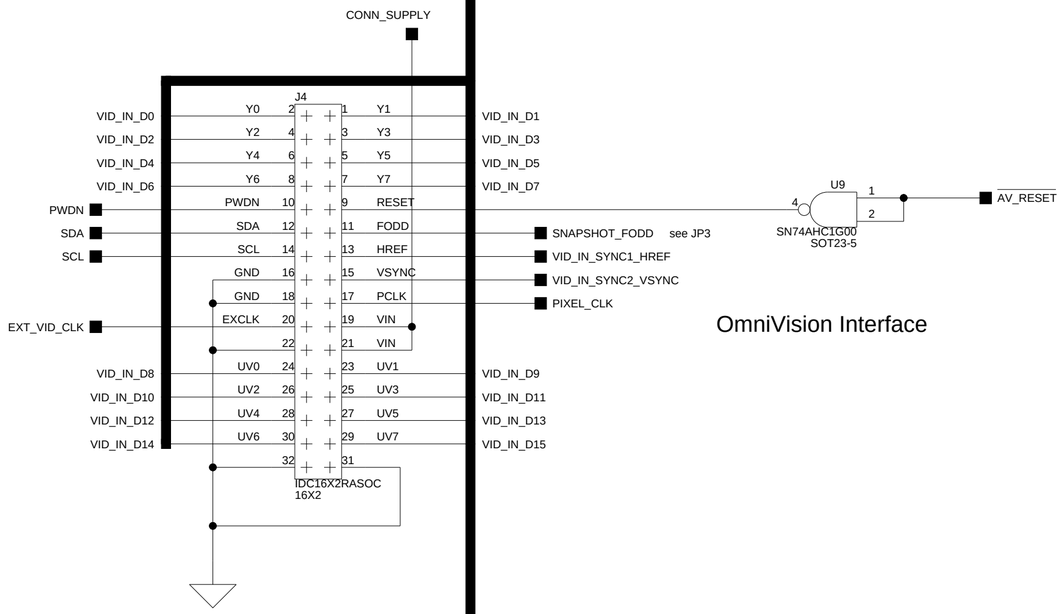
Title	Blackfin A-V EZ-Extender FS/CLK CONFIG		
Size C	**Board No.** A0193-2004		**Rev** 1.2
Date 1-18-2005_9:12		**Sheet** 5 **of** 12	



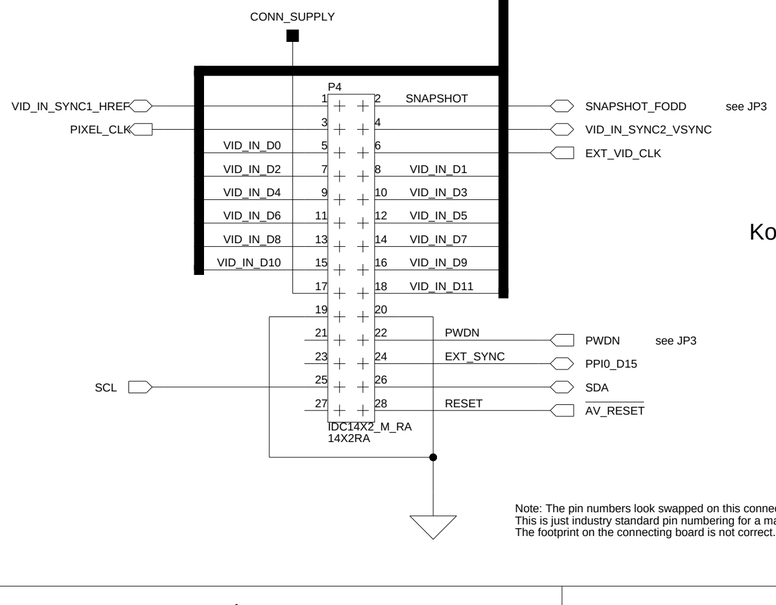
Micron Interface







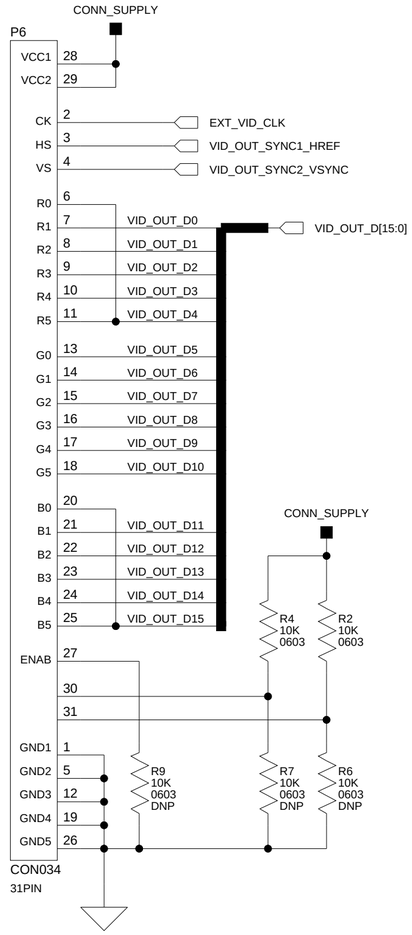
OmniVision Interface



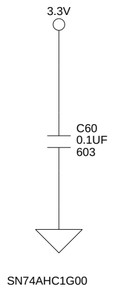
Kodak Interface

Note: The pin numbers look swapped on this connector
This is just industry standard pin numbering for a male connector
The footprint on the connecting board is not correct.

Flat Panal Display Interface



DNP = Do Not Populate
See Manual For all Jumper Settings



ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender PPI0 SETUP	
Size: C	Board No.: A0193-2004	Rev: 1.2
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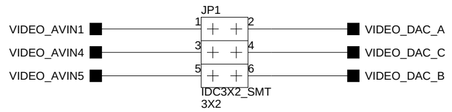
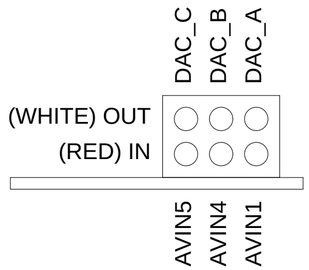
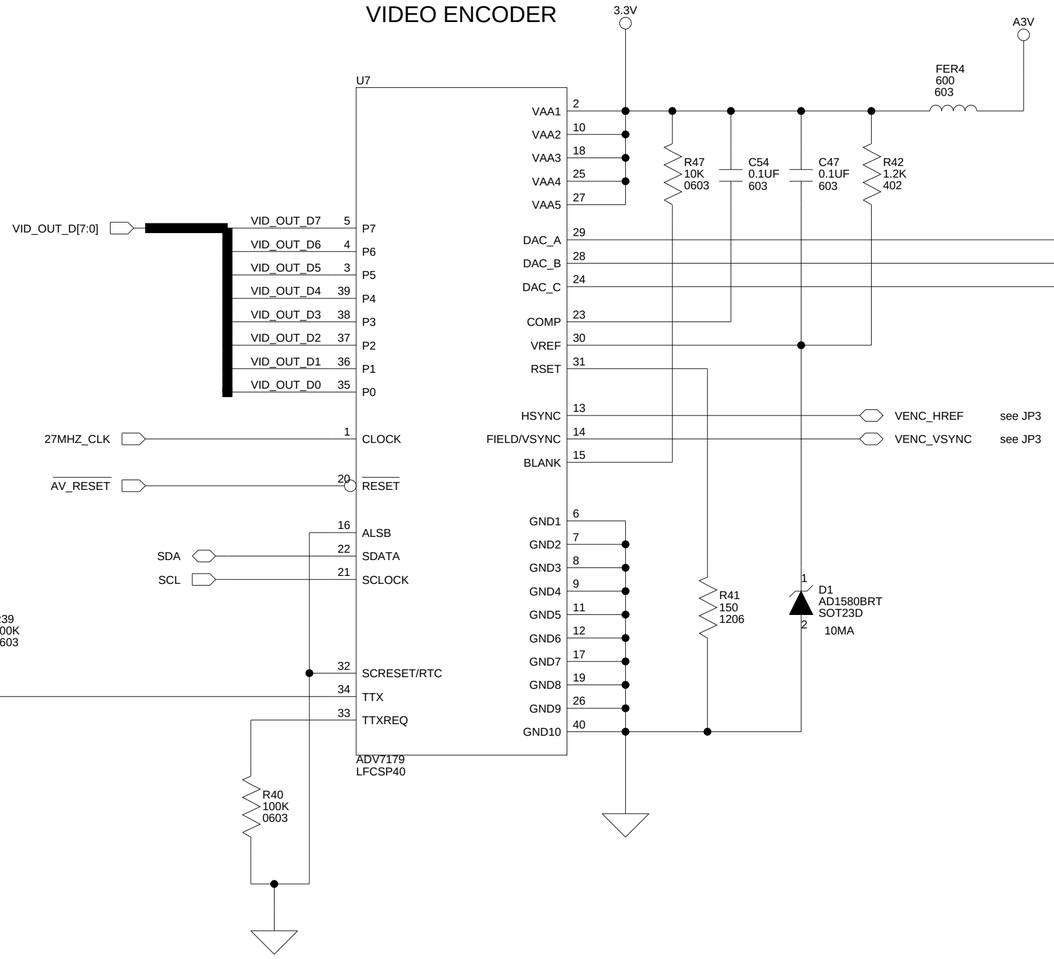
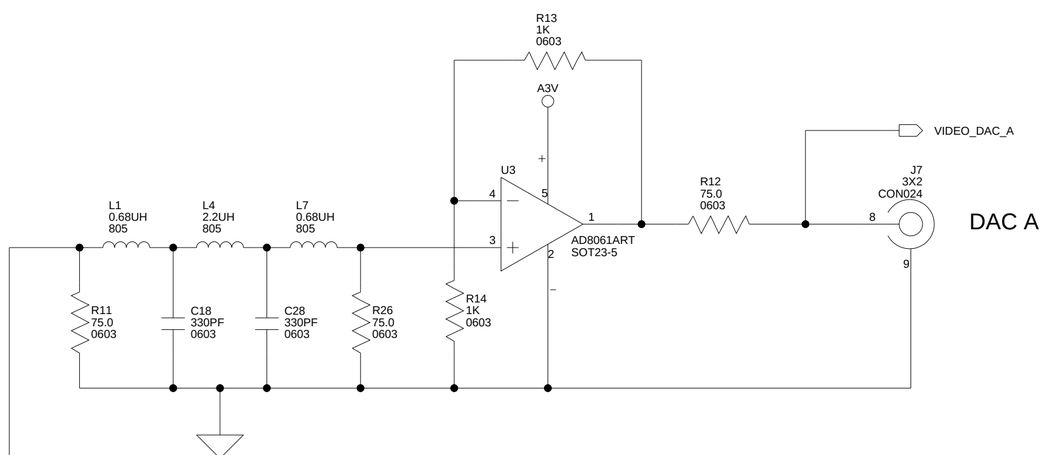
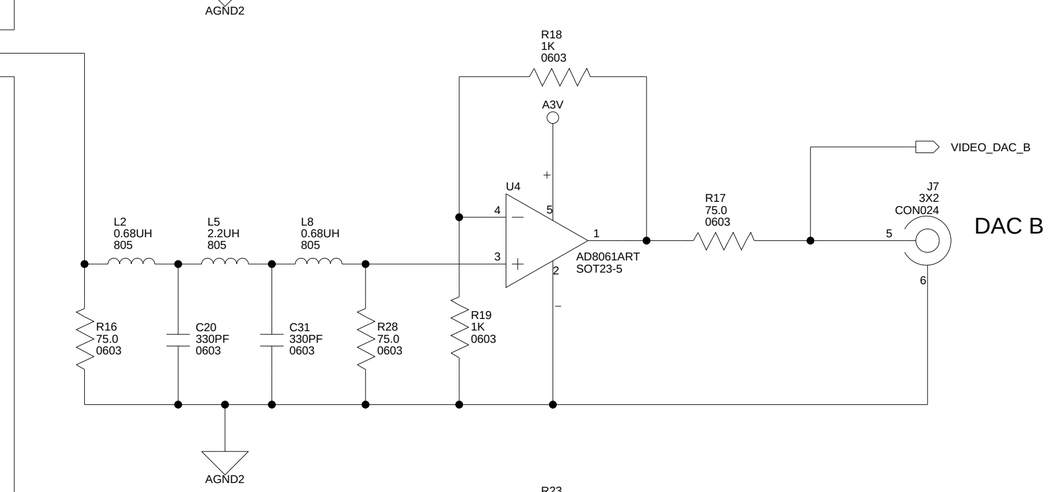


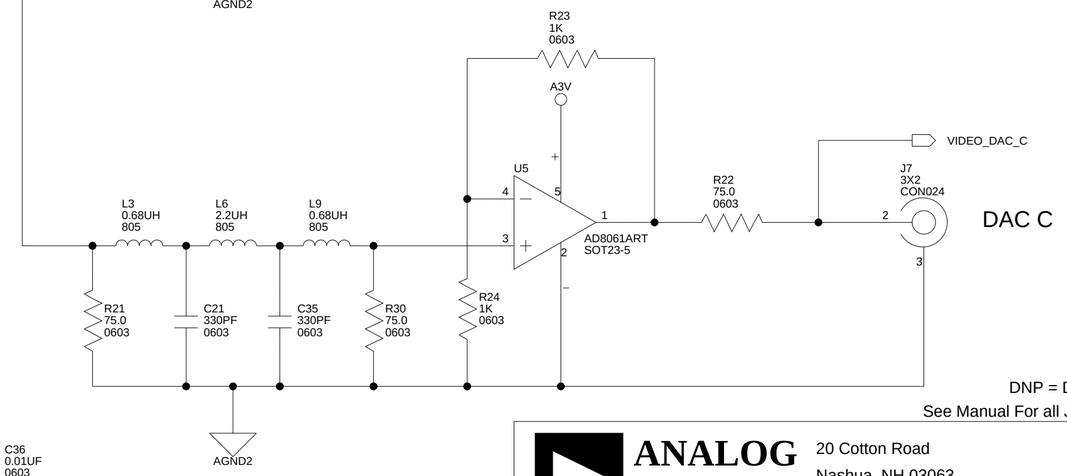


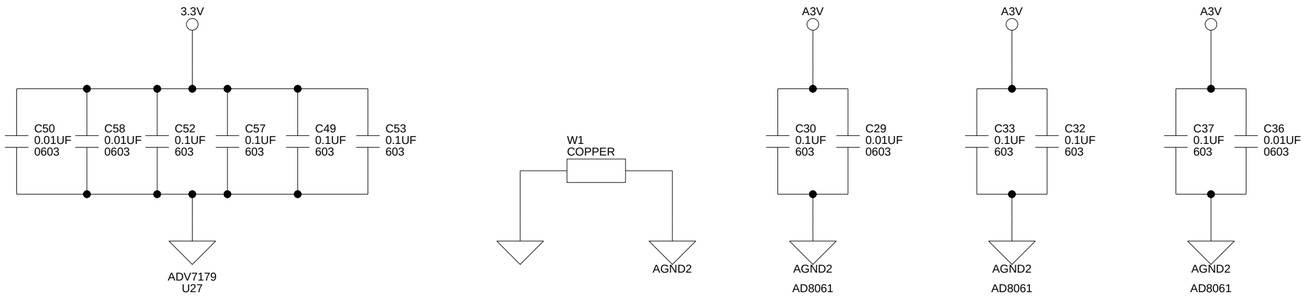
	DAC A	DAC B	DAC C
Composite Video	CVSB	CVSB	C
Component Video	G	B	R
Differential Component Video	Y	U	V
S Video	Y		C











DNP = Do Not Populate

See Manual For all Jumper Settings

ANALOG DEVICES

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender VIDEO ENCODER (OUT)		
Size C	**Board No.** A0193-2004		**Rev** 1.2
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VIDEO DECODER

	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	V	U
S Video	Y	C	

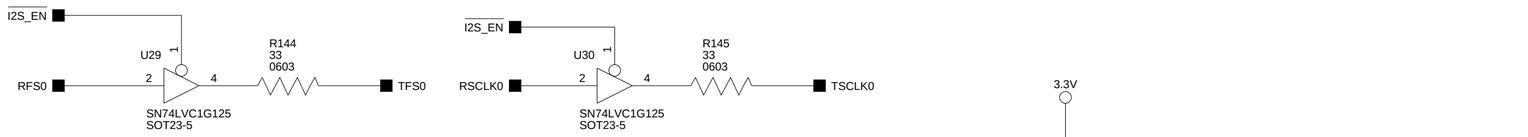
3.3V
R10 10K 0603
U1
OE
OUT
27MHZ OSC003
R5 33 0603
27MHZ_CLK
R34 10K 0603 DNP
R35 10K 0603 DNP
R45 10K 0603
R3 10K 0603
U2
XTAL
XTAL1
ALSB
SDA
SCL
SDA
SCLK
AV_RESET
RESET
PWRDN
NC[ISO]
AIN1
AIN7
AIN2
AIN8
AIN3
AIN9
AIN4
AIN10
AIN5
AIN11
AIN6
AIN12
REFOUT
CML
CAPY1
CAPY2
CAPC1
CAPC2
AVDD
PVDD
AGND1
AGND2
AGND3
AGND4
AGND5
NC[AGND6]
ADV7183BKSTZ
LQFP80
P15 P14 P13 P12 P11 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0
VID_IN_D7 VID_IN_D6 VID_IN_D5 VID_IN_D4 VID_IN_D3 VID_IN_D2 VID_IN_D1 VID_IN_D0
VID_IN_D[7:0]
LLC1
LLC2
NC[LLCREF]
ELPF
HS
VS
FIELD
NC[VREF]
NC[HREF]
NC[CLKIN]
NC[AFF]
SFL[HFF]
NC[AEF]
NC[DV]
NC[RD]
OE
DEC_DATA_OE
NC[GPO3]
NC[GPO2]
NC[GPO1]
NC[GPO0]
DVDD1
DVDD2
DVDD3
DVDDIO1
DVDDIO2
DGND1
DGND2
DGND3
DGND4
DGND5
VDEC_HS
VDEC_VS
VDEC_FIELD
VDEC_VREF
VDEC_HREF
see JP3
see JP3
R8 33 0603
U6
SN74LVC1G32 SOT23-5
R33 33 0603
VDEC_CLKOUT
PVDD_ADV7183
C2 0.01UF 0603
R1 1.5K 805
C5 82NF 805
TP4 TP5 TP6
DVDD_ADV7183
FER3 600 1206
1.8V 3.3V
3.3V 3.3V 1.8V
R32 10K 0603
VR1
IN1 IN2 SD GND
OUT1 OUT2 OUT3 FB
ADP3336ARM MSOP8
R38 76.8K 805
R36 147K 805
C27 1UF 0603
C39 1UF 0603

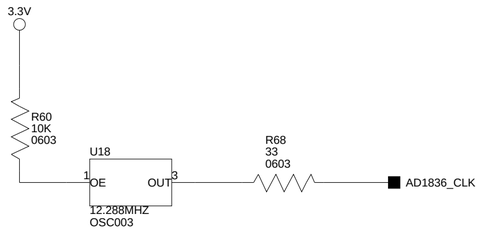
J7 3X2 CON024
AVIN1
VIDEO_AVIN1
R15 0 0603
C19 0.1UF 603
TP1
AVIN4
VIDEO_AVIN4
R20 0 0603
C34 0.1UF 603
TP2
AVIN5
VIDEO_AVIN5
R25 0 0603
C22 0.1UF 603
TP3
R27 75.0 0603
R29 75.0 0603
R31 75.0 0603
CT3 10UF B
C12 0.1UF 603
CT2 10UF B
C14 0.1UF 603
AGND2
CT1 10UF B
C8 0.1UF 603
C9 0.001UF 0603
C1 0.1UF 603
C11 0.1UF 603
CT4 10UF B
C23 0.1UF 603
C24 0.001UF 0603
C15 0.1UF 603
C38 0.1UF 603
FER2 600 1206
FER1 600 1206
PVDD_ADV7183
C4 0.1UF 603
C3 0.01UF 0603
C7 0.1UF 603
C6 0.01UF 0603
C17 0.1UF 603
C41 0.01UF 0603
C40 0.1UF 603
C13 0.1UF 603
C16 0.01UF 0603
C25 0.01UF 0603
C26 0.1UF 603
C43 0.1UF 603
C10 0.1UF 603
27MHZ OSC
SN74LVC1G32
ADV7183 U28

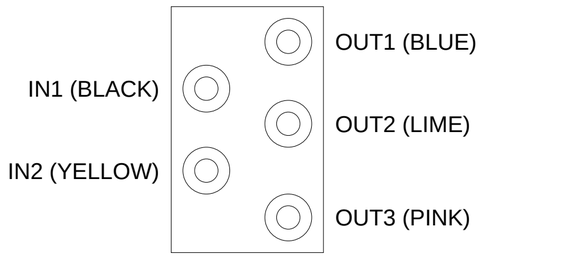
DNP = Do Not Populate
See Manual For all Jumper Settings

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

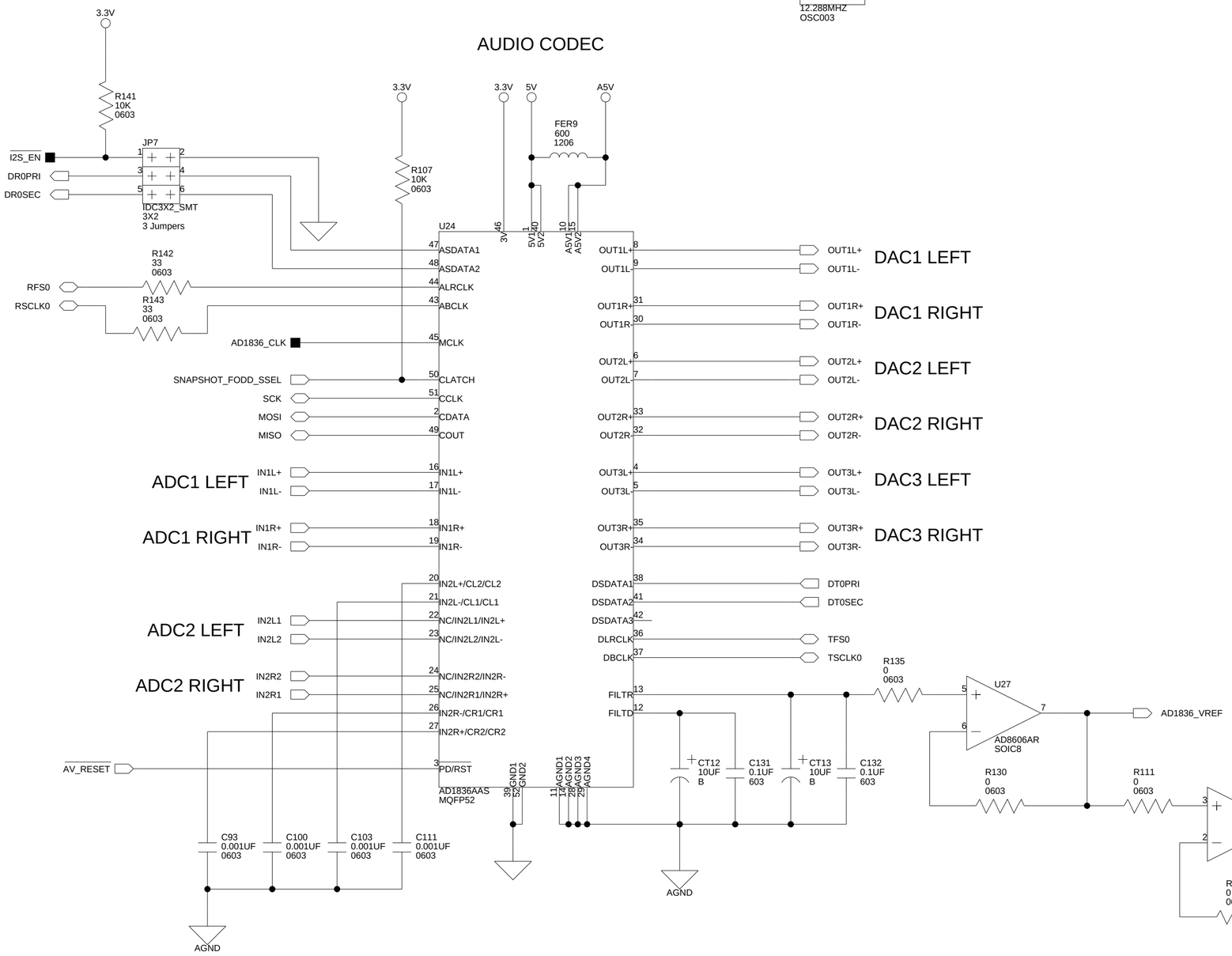
Title	Blackfin A-V EZ-Extender VIDEO DECODER (IN)		
Size C	Board No. A0193-2004		Rev 1.2
Date 1-6-2005_16:35		Sheet 8 of 12	

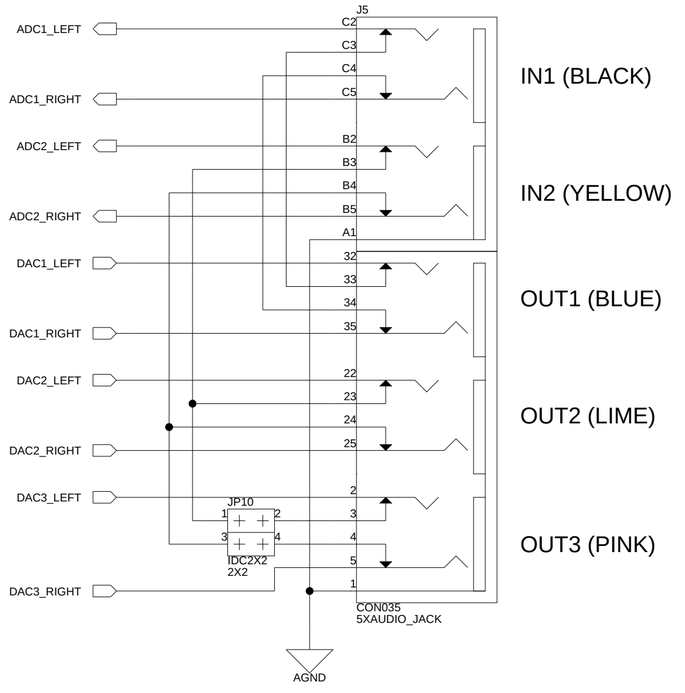


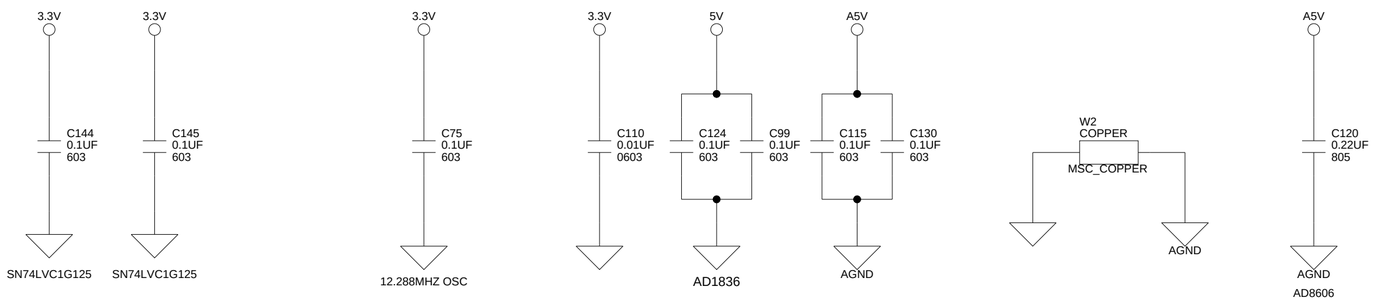




AUDIO CODEC







DNP = Do Not Populate
See Manual For all Jumper Settings

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	Blackfin A-V EZ-Extender AUDIO	
Size C	**Board No.** A0193-2004	**Rev** 1.2
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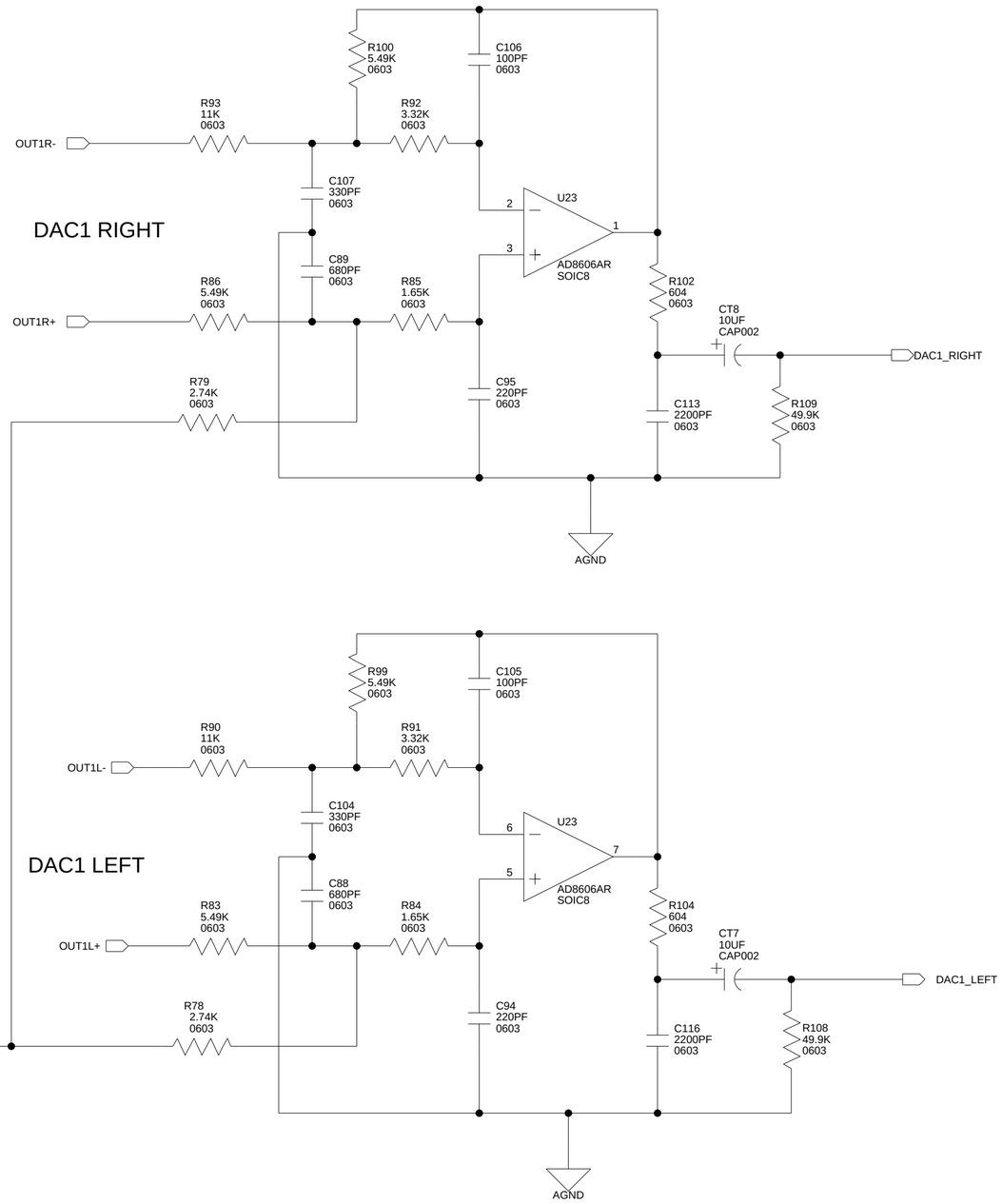
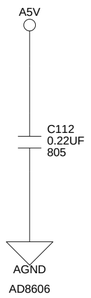


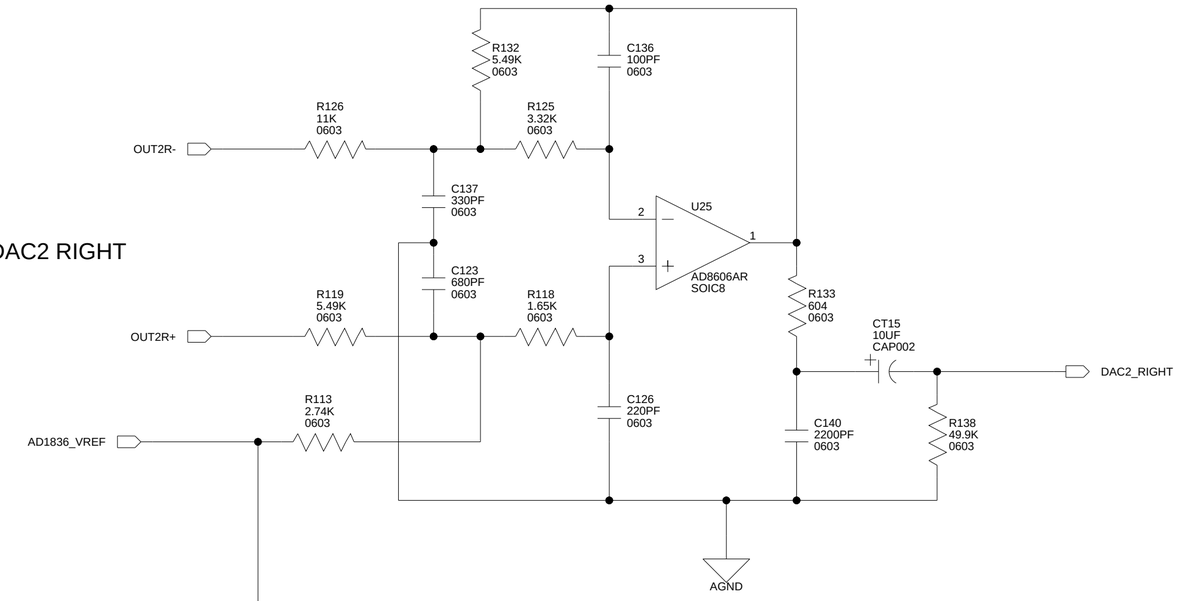


DNP = Do Not Populate
See Manual For all Jumper Settings

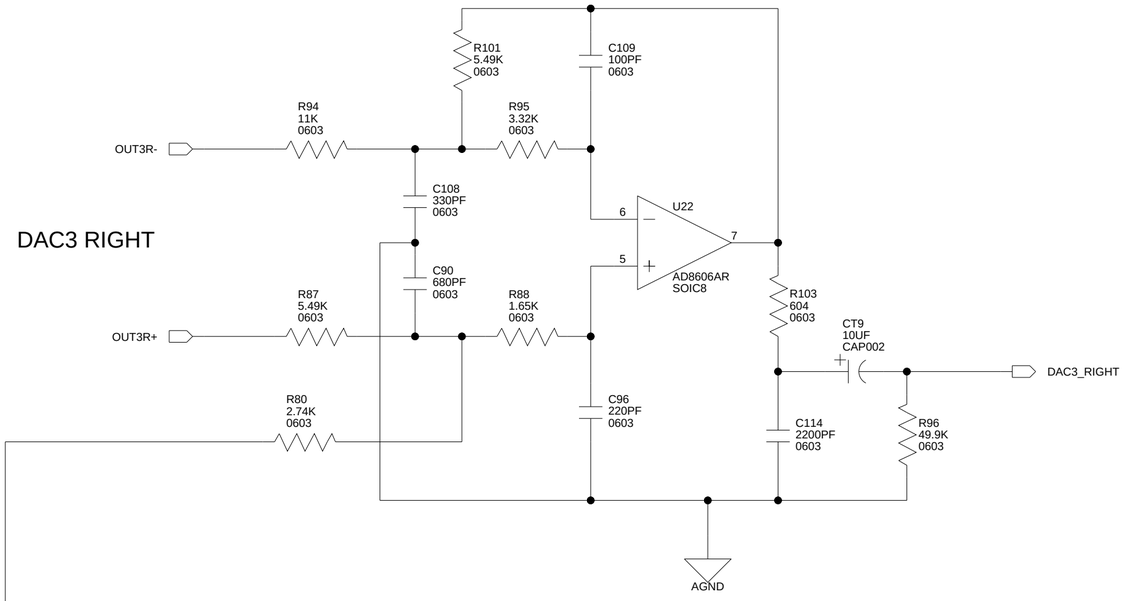
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender AUDIO OUT(CH1)	
Size C	**Board No.** A0193-2004	**Rev** 1.2
Date 12-1-2004_18:50	**Sheet** 10 **of** 12	

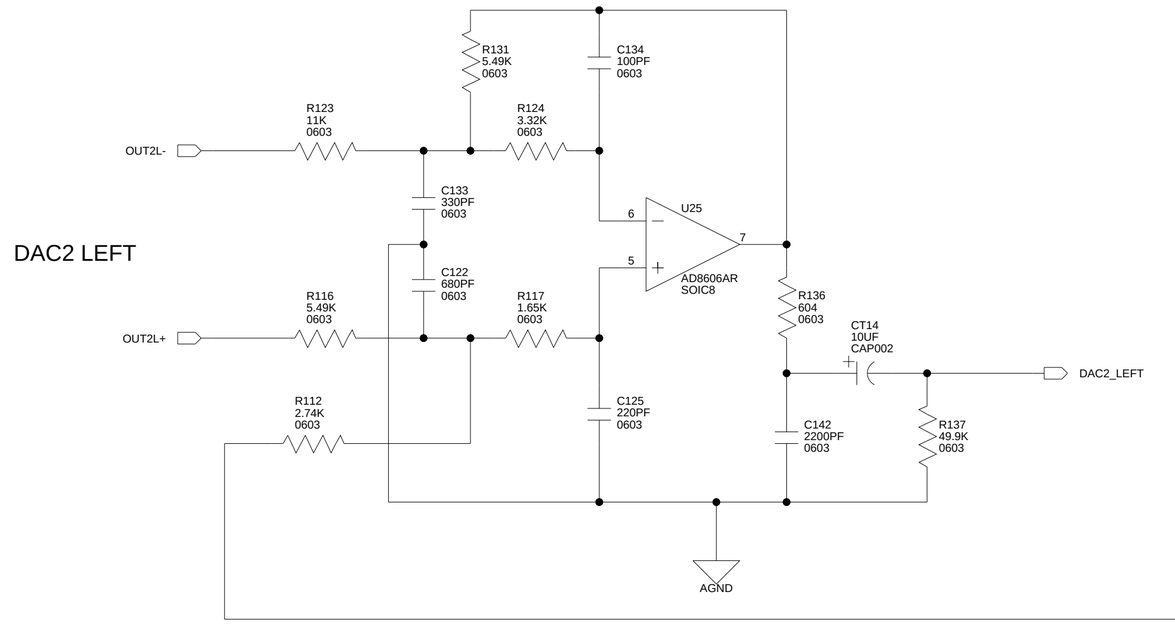
DAC2 RIGHT



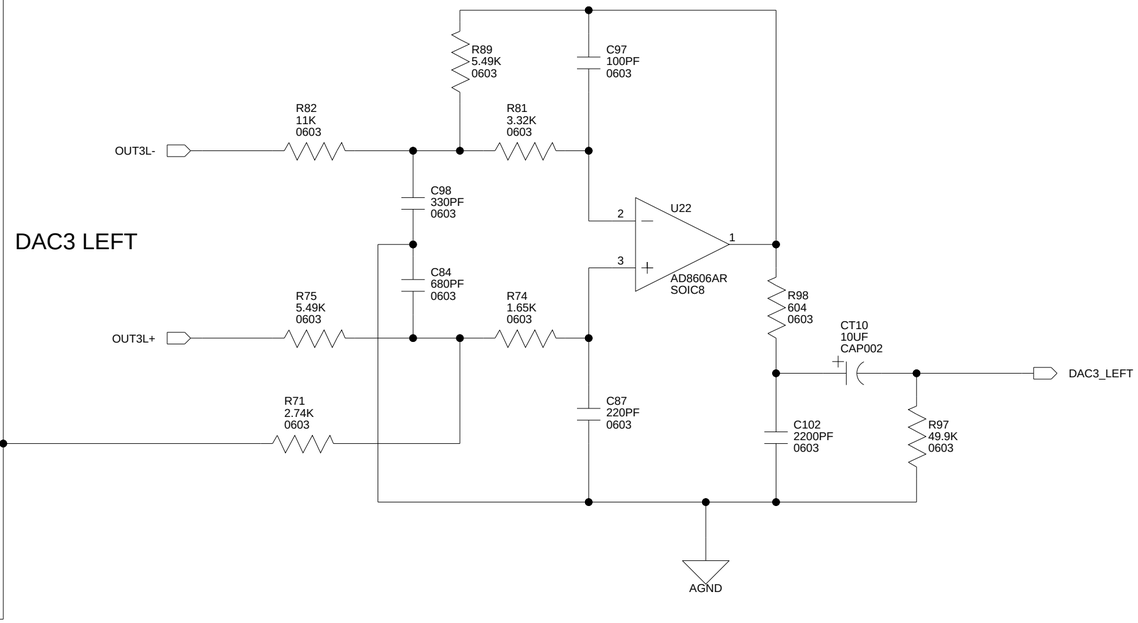
DAC3 RIGHT

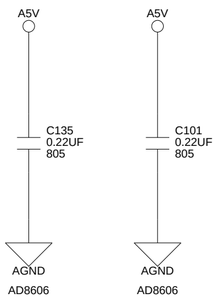


DAC2 LEFT



DAC3 LEFT





DNP = Do Not Populate

See Manual For all Jumper Settings

ANALOG DEVICES

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender AUDIO OUT(CH2, CH3)		
Size C	**Board No.** A0193-2004		**Rev** 1.2
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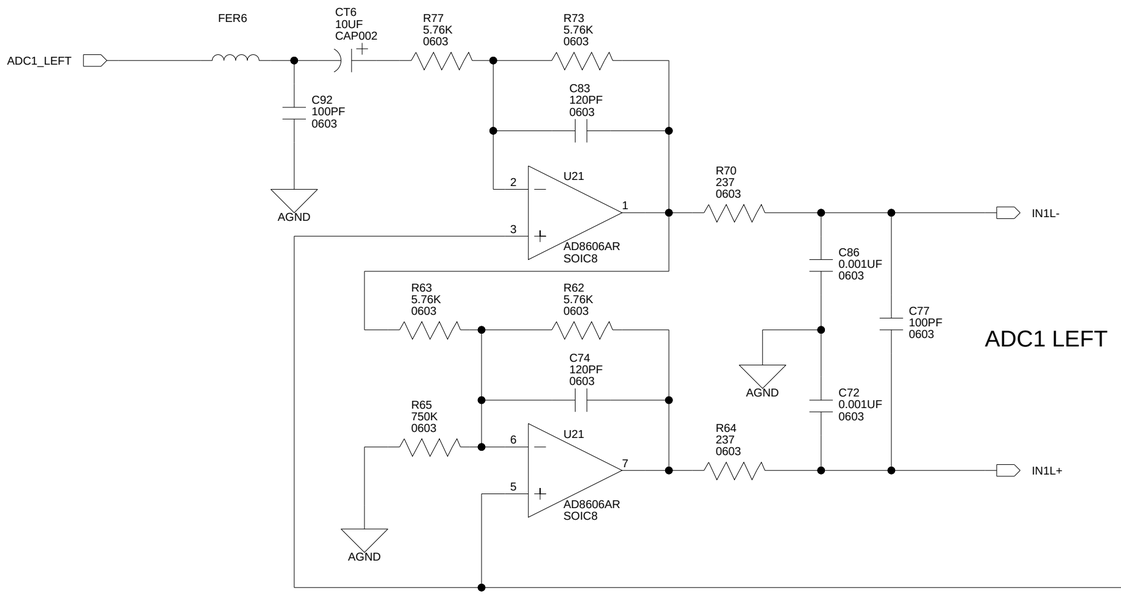
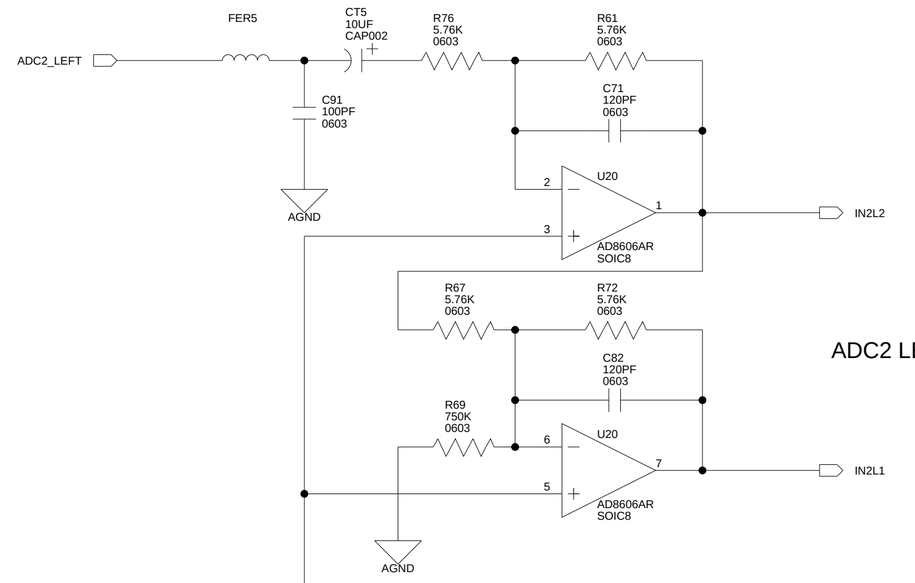
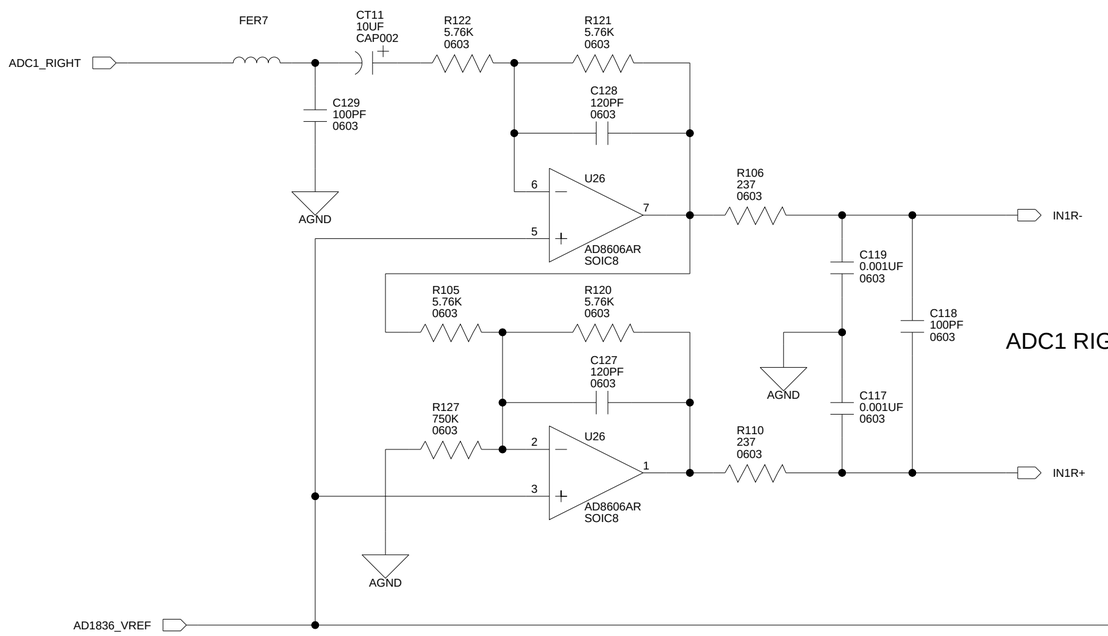


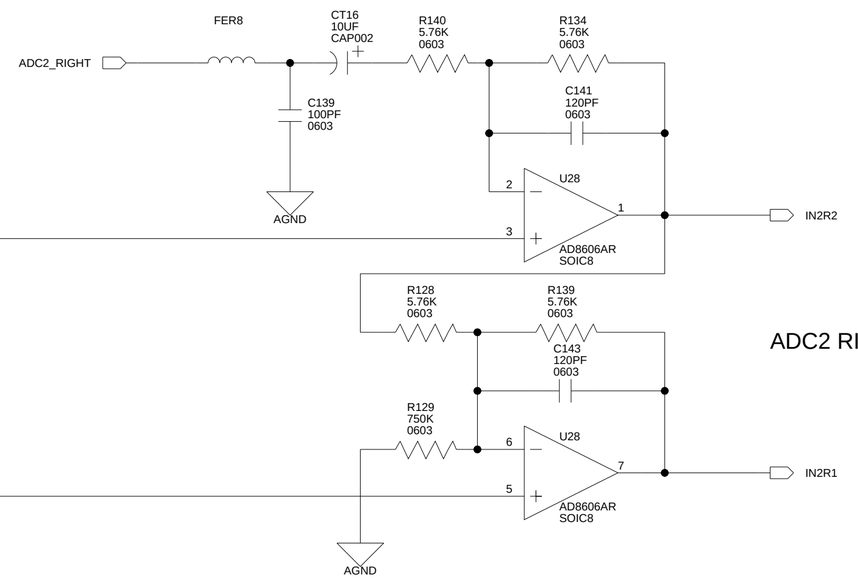
ADC1 LEFT



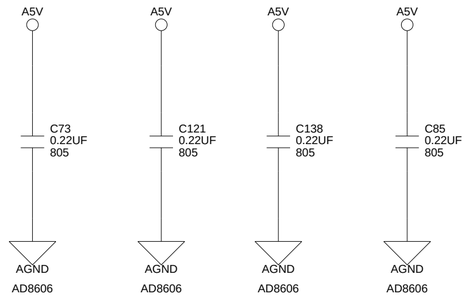
ADC2 LEFT



ADC1 RIGHT



ADC2 RIGHT



DNP = Do Not Populate
See Manual For all Jumper Settings

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	Blackfin A-V EZ-Extender AUDIO IN(CH1, CH2)	
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