Preliminary

Am2085

ISDN Subscriber Access Controller (ISAC-S)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- S-Bus transceiver according to CCITT I.430
- Recovery of clock and frame
- Frame alignment for trunk line termination
- Access to Echo bit
- Implementation of activation/deactivation procedure according to CCITT I.430
- Support of LAPD protocol
- FIFO buffer (2 × 64 byte) for efficient transfer of D-channel packets
- Serial interfaces for various types of B-channel sources/destinations (SLD, SSI)
- Switching functions for B-channels
- Watchdog timer
- Switching of test loops
- 8-bit microprocessor interface
- Advanced CMOS technology
- Low power consumption

GENERAL DESCRIPTION

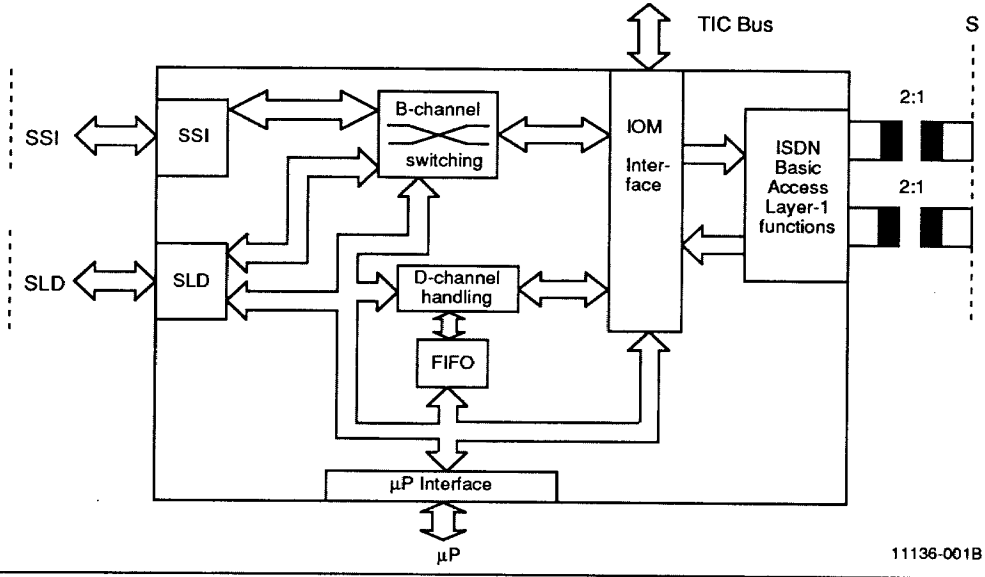
The Am2085 ISAC-S™ is a transceiver circuit able to interface voice/data communication equipment to the four-wire CCITT S-bus. It supports the LAPD protocol in hardware. For an efficient transfer of D-channel packets, FIFO structures are used.

The device is mounted in a 40-pin CMOS package.

The power consumption of the device in the active state is 80 mW (8 mW in Power Down State).

1

BLOCK DIAGRAM

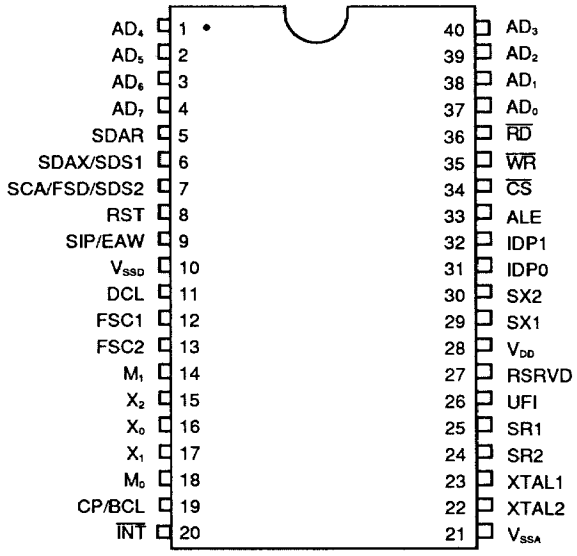


11136-001B

Publication # 11136 Rev. C & /1 Amendment
Issue Date: July 1989

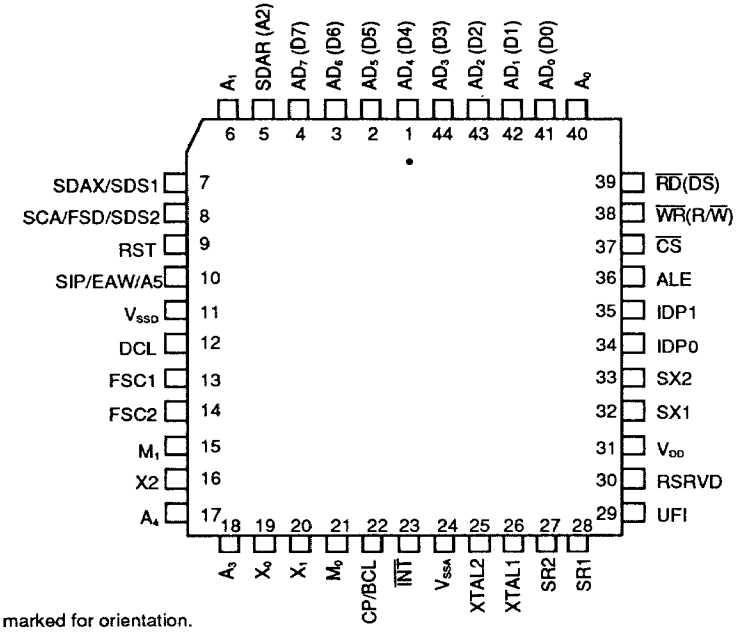
CONNECTION DIAGRAMS
Top View

40-Pin DIP



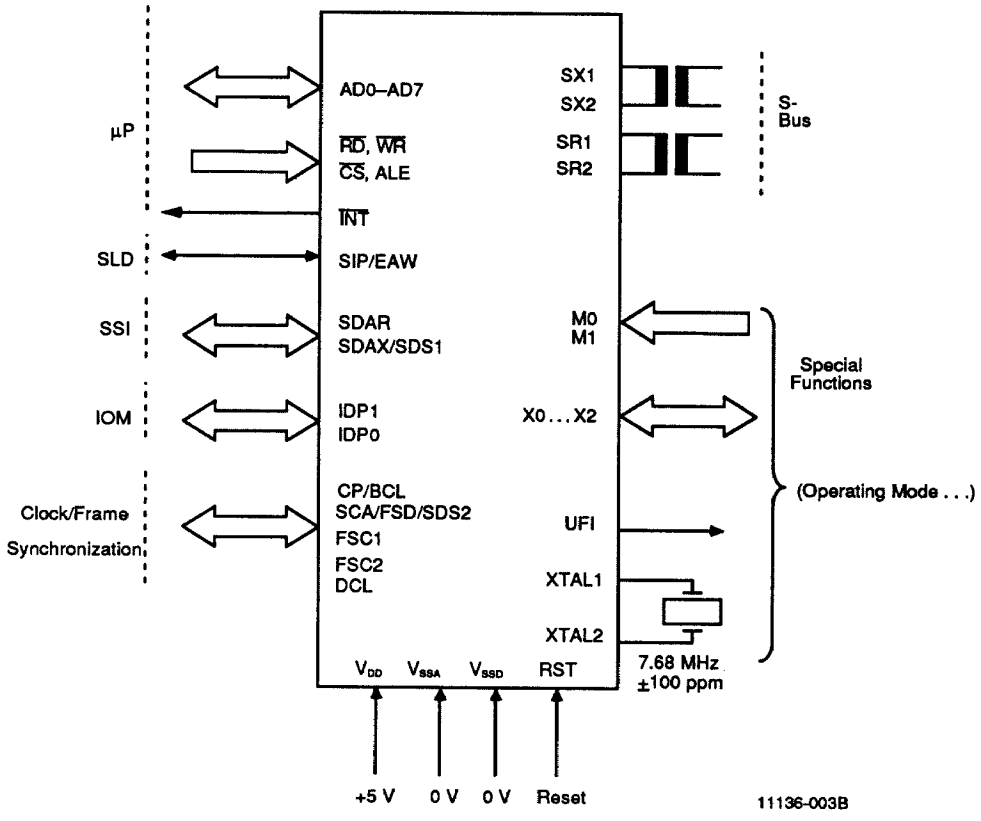
11136-002B

44-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



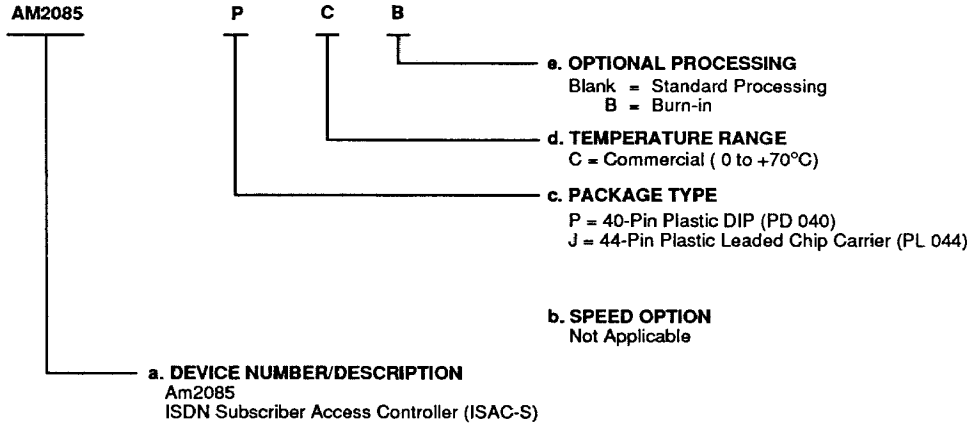
1

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2085	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

AD_0–AD_7

Address Bus (Input)

The multiplexed Address/Data Bus transfers data and commands between the microprocessor System and the ISAC-S.

ALE

Address Latch Enable (Input)

A High on this line indicates an address on the external address/data bus, selecting one of the ISAC-S internal sources or destinations.

CP

(Output)

Synchronized clock output.

$\overline{CS}$

Chip Select (Input; Active Low)

A Low on this line selects the ISAC-S for a read/write operation.

DCL

Clock (Input/Output)

This pin supplies the device clock.

FSC1

Frame Sync 1 (Input/Output)

Supplies the synchronization signal 1: input (LT-S/NT) or output (TE/LT-S).

FSC2

Frame Sync 2 (Input/Output)

Supplies the synchronization signal 2: input (LT-S/NT) or output (TE/LT-T).

$\overline{INT}$

Interrupt (Output; Active Low)

The signal is activated when the ISAC-S requests an interrupt. It is an open-drain output.

M_1, M_0

(Input)

Setting of operating mode.

$\overline{RD}$

Read (Input; Active Low)

This signal indicates a read operation.

$\overline{RST}$

Reset (Input; Acitve High)

A High on this input focus forces the ISAC-S into reset state.

SCA/FSD

Serial Clock Port A/Frame Sync. Delayed (Output)

Depending on the programmed timing mode, this output supports either a 128-kHz clock signal for the SSI port or a delayed 8-kHz frame synchronization signal for IOM interface.

SDAR

Serial Data Port A Receive (SSI) (Input)

This line receives serial data at standard TTL or CMOS levels. An integrated pull-up circuit enables connection of an open-drain/open-collector driver without an external pull-up resistor.

SDAX

Serial Data Port A Transmit (SSI) (Output)

This line transmits serial data at standard TTL or CMOS levels.

SDI

(Input/Output)

Serial Data In, IOM interface.

SDO

(Output)

Serial Data Out, IOM interface.

SIP/EAW

SLD Interface Port (Input/Output)

This line transmits and receives serial data at standard TTL or CMOS levels. When the terminal-specific functions are selected, this line serves as the subscriber awake line.

SR1

(Output)

S-bus receiver, 2.5 V reference output.

SR2

(Input)

S-bus receiver, signal input.

SX1

(Output)

Positive output S-bus transmitter.

SX2

(Output)

Negative output S-bus transmitter.

UFI
(Output)

Connection for an optional external RC circuit.

V_{DD}

Power supply (+5 V ±5%).

V_{SSA}

Analog ground.

V_{SSD}

Digital ground.

$\overline{WR}$

Write (Input; Active Low)

This signal indicates a write operation.

X_2, X_1, X_0

(Input/Output)

Operating mode-specific functions.

XTAL1
(Input)

Connection for crystal or external clock input.

XTAL2
(Output)

Connection for external crystal. Left unconnected if external clock is used.

OPERATIONAL DESCRIPTION

The ISAC-S, designed for the user area of the ISDN basic access, can be used for the following applications corresponding to the appropriate basic operating mode of the ISAC-S:

• **Terminal equipment type 1**	
ISDN feature telephone, extended ISDN terminal	TE Mode
• **Network termination 2**	
PABX, including the functions for the following:	
–line termination on S(LT-S), just as in a digital subscriber line module	LT-S mode (INFO 2 and 4 will be generated automatically)
	NT mode (Info 2 and 4 must be initiated by software)
–line termination on T(LT-T), just as in a digital line trunk module	LT-T mode

The operating mode of the ISAC-S must be selected by pin-strapping, as described in Operating Modes, before Power On Reset.

Reset

After Reset, Layer 1 will have reached the following state:

- G1 deactivated in LT-S/(NT) mode
- F3 standby in TE/LT-T mode

according to CCITT I.430 (see Control of Layer 1). F3 standby state means that the internal oscillator is active, and the DCL clock and the FSC1/FSC2 frame signals are delivered as output signals. The F3 power down state, with a minimum power consumption of not more than 8 mW, can be achieved by programming the CFS-bit = "1" in the ADFR register.

1

Table 1. Subset of ISAC-S Registers with Defined Reset Values (in Hex)

Register	Value After Reset	Meaning
ISTA	00	No interrupts
MASK	00	All interrupts enabled
EXIR	00	No interrupts
STAR	48	XFIFO is ready to be written to RFIFO is ready to receive at least 16 octets of a new message
CMDR	00	No command
MODE	00	Auto mode 1-octet address field External timer mode Receiver inactive IOM interface, monitor channel not used (TE: pt-pt, LT-S/(NT): point-to-multipoint)
RFBC	00	No frame bytes received
SPCR	00	SDI pin = High SIP/SAW pin "High Impedance" (SLD interface deactivated) Timing mode 0 (terminal) IOM interface test loop deactivated SLD B-channel loop is selected SDAX pin = High
STCR	00	Serial interface port for the SLD interface selected TIC bus address 0 No Synchronous Transfer
CIXR	BF	C/I code = 1111 TE-channel data = 1 TIC bus is not requested for transmitting a C/I code
ADFR	00	No prefilter Active clock signals (Standby) in TE mode Adaptive timing (point-to-multipoint) in NT/LT-S FSC1/FSC2 frame signals are not inverted in TE mode Interframe time fill = consecutive 1

Initialization

During initialization phase the appropriate registers must be programmed according to the application and the desired features, as listed in Table 2.

Table 2. Programming for Initialization Phase

Function	Register	Effect
Special Functions	ADFR	Prefilter Disabled Layer-1 functions Standby/power-down selection in TE mode, fixed (point-to-point, S interface), adaptive (S-bus) timing in LT-S mode B1/B2-channel assignment (SSI) in TE mode Interframe time fill in HDLC port mode
Masking Interrupts	MASK	Masking of selective interrupt sources
D-channel (HDLC port)	MODE	Message transfer mode 2-octet/(1-octet) address Timer mode: external/internal (auto mode only) IOM interface mode: IOM: point-to-point and point-to-multipoint (LT-S,NT) IOM: point-to-multipoint (TE) HDLC port: (TEM-bit 1)
	TIMR	N1 and T1 in internal timer mode (TDM-bit in mode) T2 in external timer mode
	XAD1	SAPI: LAPD transmit address octet (auto mode only)
	XAD2	TEI:
	SAP1/SAP2	SAPI: LAPD receive address octet for the internal address recognition
	TEI1/TEI2	TEI:
Serial interface B-channel switching, Terminal-specific functions	SPCR	SLD port inactive/active Timing mode 0, 1 IOM interface loop (reduced timer resolution) B-channel switching
	STCR	Terminal-specific functions/SLD interface TIC bus address
	CIXR	Subscriber/Exchange Awake, Watchdog Timer

Table 3. Characteristics and Typical ISDN Applications of the Message Transfer Modes

	Message Transfer Modes				
	Auto Mode	Non-Auto Mode	Transparent Mode	Ext. Transparent Mode 1	Ext. Transparent Mode 0
Characteristics	One logical link (SAP1, TEI1) can be handled autonomously Window Size (WZ) = 1 Full address recognition (SAPI, TEI)	Full address recognition (SAPI, TEI)	SAPI address recognition	SAPI address recognition	No address recognition fully transparent
Typical Application	Terminal: WZ = 1 Exchange: point-to-point configuration WZ = 1	Terminal: WZ ≥ 1 Exchange: point-to-point configuration WZ ≥ 1	Exchange: bus configuration	Exchange: bus configuration	Diagnostic

Processing

Assuming the ISAC-S has been initialized for typical applications in the user area of the ISDN basic access, the ISAC-S is now ready to transmit and receive messages in the D-channel (LAPD support). As a prerequisite for that, the Layer 1 must be previously activated. The control of the data transfer phase is mainly done by commands from microprocessor to ISAC-S via the CMDR register and by interrupt indications from ISAC-S to microprocessor (ISTA and EXIR register).

The two B-channels (B1/B2) can be switched in a highly flexible manner between the S interface (IOM interface) and the SSI and SLD interface.

Control of Layer 1

The management commands of Layer 2, programmed in the CIXR register, trigger certain procedures in Layer 1. The responses from Layer 1 can be read from CIRR register after a CIC interrupt (ISTA). An example of activation and deactivation with the respective commands and indications is depicted in Figure 4.

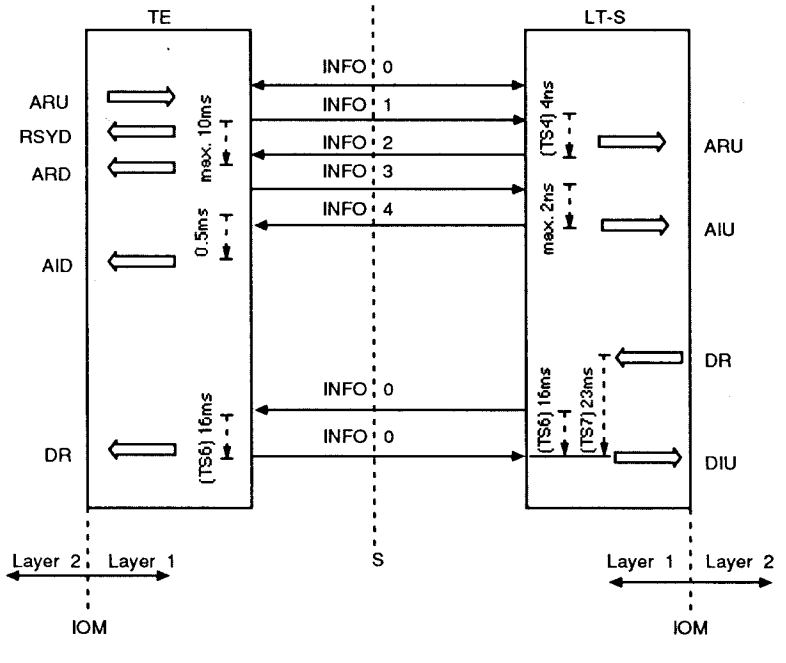


Figure 4. Example of Activation/Deactivation

Tables 4 to 6 contain the command/indication codes in the different operating modes:

Table 4. Commands and Indications in LT-S Mode

Command (downstream)	Abbr.	Code	Remark
Deactivate request	DR	0000	(x)
Send continuous zeros	SCZ	0001	Transmission of AMI pulses at a frequency of 96 kHz (x)
Send single zeros	SSZ	0010	Transmission of AMI pulses at a frequency of 2 kHz (x)
Activate request	ARD	1000	
Activate request loop	ARL	1010	Activate request for loop 2
Deactivate indication	DID	1111	Deactivation acknowledgment, quiescent state
Indication (upstream)			
Lost signal level	LSL	0001	No receive signal
Lost framing	RSYU	0100	Receiver is not synchronous
Activate request	ARU	1000	Info 1 received
Activate indication	AIU	0100	Synchronous receiver
Deactivate indication	DIU	1111	Timer TS6 or TS7 expired after deactivation command

Note: (x) = unconditional commands

Table 5. Commands and Indications in NT Mode

Command (downstream)	Abbr.	Code	Remark
Deactivate request	DR	0000	(x)
Send continuous zeros	SCZ	0100	Transmission of AMI pulses at a frequency of 96 kHz
Activate request	ARD	1000	Transmission of info 2
Activate request loop	ARL	1010	Transmission of info 2, switching of test loop 2
Deactivate indication	DID	1111	Deactivation acknowledgment, quiescent state
Activate indication	AID	1100	Transmission of info 4
Activate indication loop	AIL	1110	
Indication (upstream)			
Timing	TIM	0000	Clocks are required
Lost signal level	LSL	0001	No receive level
Lost framing	RSYU	0100	Receiver is not synchronous
Error indication	EI	0110	RST and SCZ both active
Activate request	ARU	1000	Info 1 received
Activate indication	AIU	1100	Synchronous receiver
Deactivate indication	DIU	1111	Timer TS6 or TS7 expired after deactivation command

Note: (x) = unconditional commands

Table 6. Commands and Indications TE/LT-T

Command (downstream)	Abbr.	Code	Remark
Timing	TIM	0000	Clocks are required
Reset	RS	0001	(x)
Send single zeros	SSZ	0010	Transmission of AMI pulses at a frequency of 2 kHz (x)
Activate request, priority 8	AR8	1000	Activation command set D-channel priority to 8
Activate request, priority 10	AR10	1001	Activation command set D-channel priority to 10
Activate request	ARL	1010	Activation of test loop 3 (x)
Deactivate indication	DIU	1111	IOM interface can be switched into idle state
Indication (upstream)			
Power up	PU	0111	IOM clocking is provided
Deactivate request	DR	0000	Deactivation request by S
Slip detected	SD	0010	Wander is larger than 18 µs peak-to-peak
Disconnected	DIS	0100	Pin CON connected to GND
Error indication	EI	0110	(RST = 1 and CFS-bit = 0) or RS
Level detected	RSY	0100	Signal received, receiver
Activate request	ARD	1000	Info 2 received
Test indication	TI	1010	Test loop 3 activated or continuous zeros transmitted
Activate indication with priority class 8	AI 8	1100	Info 4 received, D-channel priority is 8 or 9
Activate indication with priority class 10	AI 10	1101	Info 4 received, D-channel priority is 10 or 11
Deactivate indication	DID	1111	Clocks will be in disabled quiescent state

Note: (x) = unconditional commands

1

Transfer of LAPD frames in the D-Channel

When Layer 1 of the S interface is activated, the ISAC-S is able to transmit and receive LAPD frames via this international standardized interface in a highly sophisticated manner.

The LAPD protocol support depends on the selected message transfer mode (Table 5 and Layer 2 Functions section). The powerful FIFO structure of the ISAC-S, which consists of a 2 × 32 byte receive and a 2 × 32 byte transmit FIFO, as well as an intelligent FIFO controller, builds a flexible connection between the LAPD controller of the ISAC-S and upper layer protocol functions in the microcontroller system via the microprocessor interface. Assuming a normally running communication link (Layer 1 activated, Layer 2 link established, TEI assigned, and so on), Figure 5 demonstrates the transfer of an I-frame via the D channel.

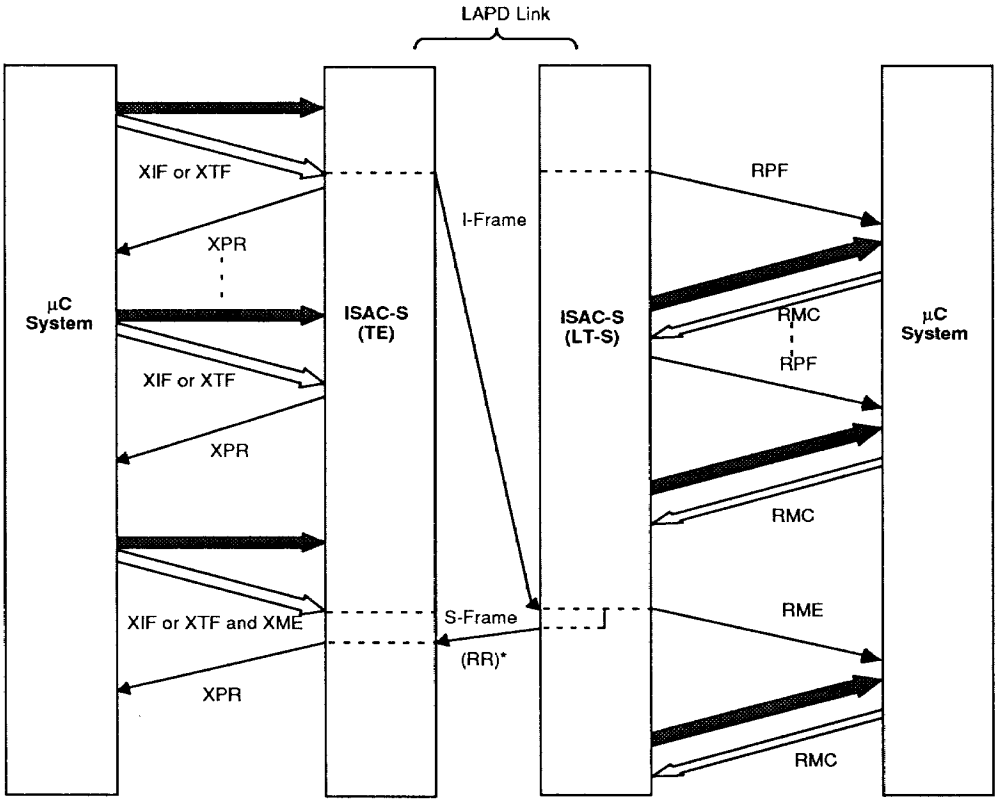


Figure 5. Transmission of an I-Frame in the D-channel (Subscriber to Exchange)

The following table summarizes the commands which can be programmed by setting appropriate bits in the CMDR register to Control Layer 2 (see also Detailed Register Description).

Table 7. CMDR Register Bits for Layer 2 Control

Com.	HEX	Bit 7–0	Meaning
RMC	80	1000 0000	Receive message complete
RHR	40	0100 0000	Reset HDLC receiver
RNR	20	0010 0000	Receiver not ready (auto mode)
STI	10	0001 0000	Start timer
XTF	08	0000 1000	Transmit transparent frame without closing the frame
XIF	04	0000 0100	Transmit "auto mode" I-frame without closing the frame
XTFC	0A	0000 1010	Transmit transparent frame and close frame
XIFC	06	0000 0110	Transmit "auto mode" I-frame and close frame
RHX	01	0000 0001	Reset HDLC Transmitter

Interrupt List

In the following table, all interrupts of the ISAC-S are listed together (see also Detailed Register Description).

Table 8. Meaning of ISAC-S Interrupts (Layer 1 and Layer 2)

	Interrupt			Meaning	Reaction (ISDN)
Layer 2 receive	RPF	ISTA	Receive Pool Full	Request for reading received octets of a LAPD frame from RFIFO.	Read the octets and acknowledge with RMC command.
	RME	ISTA	Receive Message End		
	RFO	EXIR	Receive Frame Overflow	A frame has been lost. The microcontroller has failed the minimum reaction time.	Error report for statistical purposes only.
	PCE	EXIR	Protocol Error	S- or I-frame with incorrect N(R) or S-frame with I-field received, (in auto mode only).	Error report Data link release indication to Layer 3.
	TIN	ISTA	Timer interrupt	External timer expired or, in auto mode, internal timer (T200) and repeat counter (N200) both expired.	Error report Data link release indication to Layer 3 (no acknowledgment from peer entity).
Layer 2 transmit	XPR	ISTA	Transmit Pool Ready	Acknowledgment that further octets of an LAPD frame can be written to the XFIFO.	Write further octets to the XFIFO and subsequently request (further) transmission with X_F or X_FC.
	RSC	ISTA	Receive Status Change	A status change from peer has been received, RR/RNR frame.	Read STAR register, check RRNR-bit and report it.
	XMR	EXIR	Transmit Message Repeat	Frame must be repeated due to a transmission error and/or a received negative acknowledgment.	Transmission of this frame must be repeated. No indication to Layer 3.
	XDU	EXIR	Transmit Data Underrun	Frame has been aborted because the XFIFO holds no further data (messages greater than 32 octets).	
Layer 1	CIC	ISTA	C/I Code Change	A change of indication from layer-1 has been detected.	Read CIRR register and report reason to management entity.
	MOR	EXIR	—	Not used in the ISAC-S.	
Synchronous transfer	SIN	ISTA	Synchronous Transfer Interrupt	Synchronization of microprocessor and data transfer via serial interfaces.	Access to B-channel registers BCX1/2, BCR1/2, or SFCR. Has to be confirmed by setting the appropriate STO/(1)-bit in STCR within a time limit.
	SOV	EXIR	Synchronous Transfer Overflow	The SIN interrupt was not confirmed on time by setting the appropriate STO/(1)-bit in STCR.	Abnormal error condition. Revise access software.
Terminal-specific functions	SAW	EXIR	Subscriber Awake	Indicates a falling edge on SAW line (terminal-specific functions are selected.	Switch into "Power Up" state and start data link establish procedure.
	WOV	EXIR	Watchdog Timer Overflow	Watchdog timer has been expired (terminal-specific functions are selected).	Worst error condition. Restart system software.
	EXI	ISTA	Extended Interrupt	An interrupt indicated in EXIR has occurred.	Read EXIR and determine interrupt source.

FUNCTIONAL DESCRIPTION

The Am2085 performs the Layer 1 functions of the ISDN basic access as well as B-channel switching and wide-spread functional support for Layer 2.

General Functions and Device Architecture

The detailed block diagram of the ISAC-S is shown in Figure 6.

The left side of the diagram contains the Layer 1 functions, according to CCITT I series recommendations:

- S-bus transmitter and receiver
- Timing recovery and synchronization by means of digital PLL circuitry
- Activation/Deactivation
- D-channel access

Furthermore the following diagnostic tests are implemented:

- Test loop 2 (NT/LT-S) and 3 (TE/LT-T) close to the S-bus
- Send single AMI pulses at 2 kHz and send continuous AMI pulses at 96 kHz

The right side consists of Layer 2 functions to support LAPD and provides B-channel switching capabilities.

In a special operating mode, the auto mode, the ISAC-S processes information transfer and procedure handshakes (I- and S-frames) of the LAPD protocol autonomously.

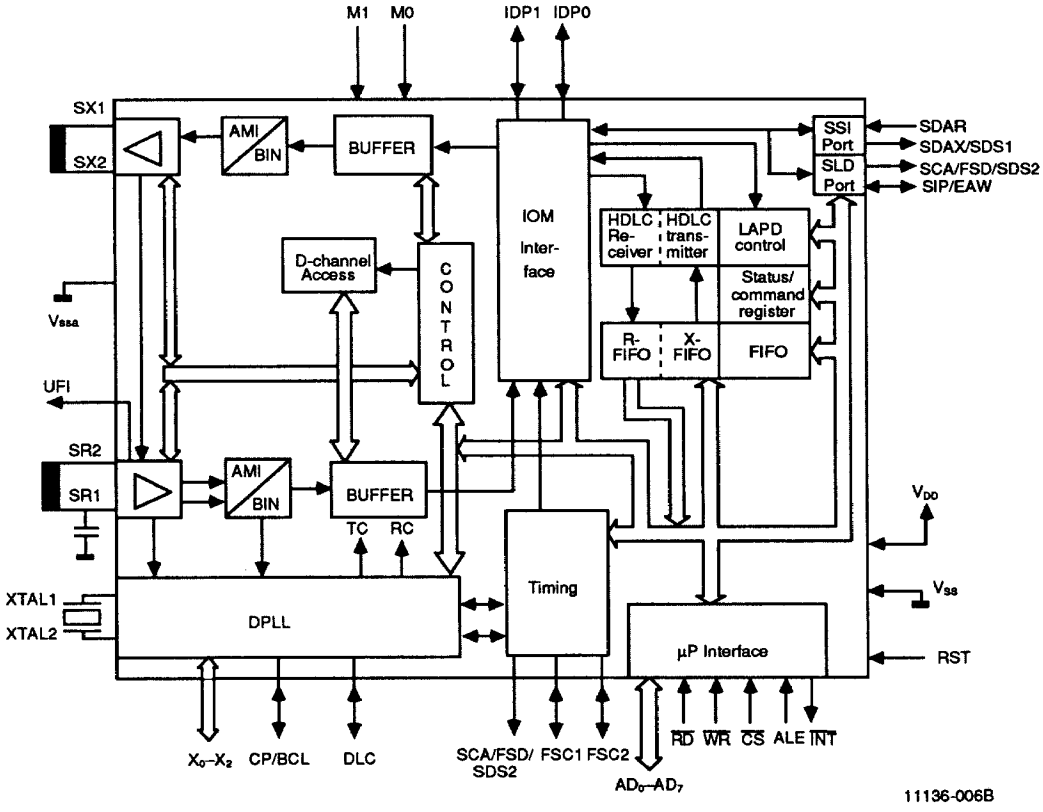


Figure 6. ISAC-S Device Architecture

Two serial interfaces to B-channel sources/destinations are realized:

- The standard SLD interface which is a bidirectional (ping-pong) 256-kb/s interface primarily optimized for telecommunication applications
- The full-duplex 128-kb/s interface, SSI, which can serve as a general interface in TEs to transfer the two B-channels

Control and monitor functions as well as data transfers (D-channel messages, transparent B-channel data) by the user's CPU is performed through a standard 8-bit microprocessor interface. A highly sophisticated 2 × 64 byte FIFO structure for both directions enables a flexible D-channel message information exchange between the LAPD (HDLC) controller and a microcontroller system.

The timing unit is responsible for the system clock and frame synchronization. Pin-strapping determines its operating mode.

Operating Modes

The Am2085 is configurable for the following applications:

- ISDN terminals (TE)
  —> TE (mode)
- ISDN subscriber line termination (LT-S)
  —> LT-S/(NT) mode
- ISDN trunk line termination (PABX connection to central office)
  —> LT-T mode

Configuration is performed by pin-strapping (pins M_2, M_0), yielding different meanings to the multifunctional pins (X_0, X_1, X_2) as well as the clock and framing signal pins (DCL, FSC1, FSC2, CP).

Table 9. Operating Modes and Functions of Mode-Specific Pins of Am2085 ISAC-S

Application	M2	M0	DCL	FSC1/2	CP	X2	X1	X0
TE	0	0	O: 512 kHz*	O: 8 kHz*	O: 1536 kHz*	O: ECHO	O: 3840 kHz	I: CON
LT-T	0	1	I: 512 kHz	I: 8 kHz	O: 512 kHz*	I: fixed at 0	I: fixed at 0	I: CON
LT-S1	1	0	I: 512 kHz	I: 8 kHz	I: fixed	I: fixed at 0	O: 7680 kHz at 0	I: fixed at 0
NT	1	1	I: 512 kHz	I: 8 kHz	I: SCZ	I: SSZ	I: fixed at 0	–

*synchronized to S I = Input O = Output

Notes:
ECHO Reproduces the E-bits received from the S interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1.
CON Connected to S-bus
SCZ Send continuous binary zeros (96 kHz)
SSZ Send single binary zeros (2 kHz)

The different operating modes in relation to the timing recovery are illustrated in Figure 7.

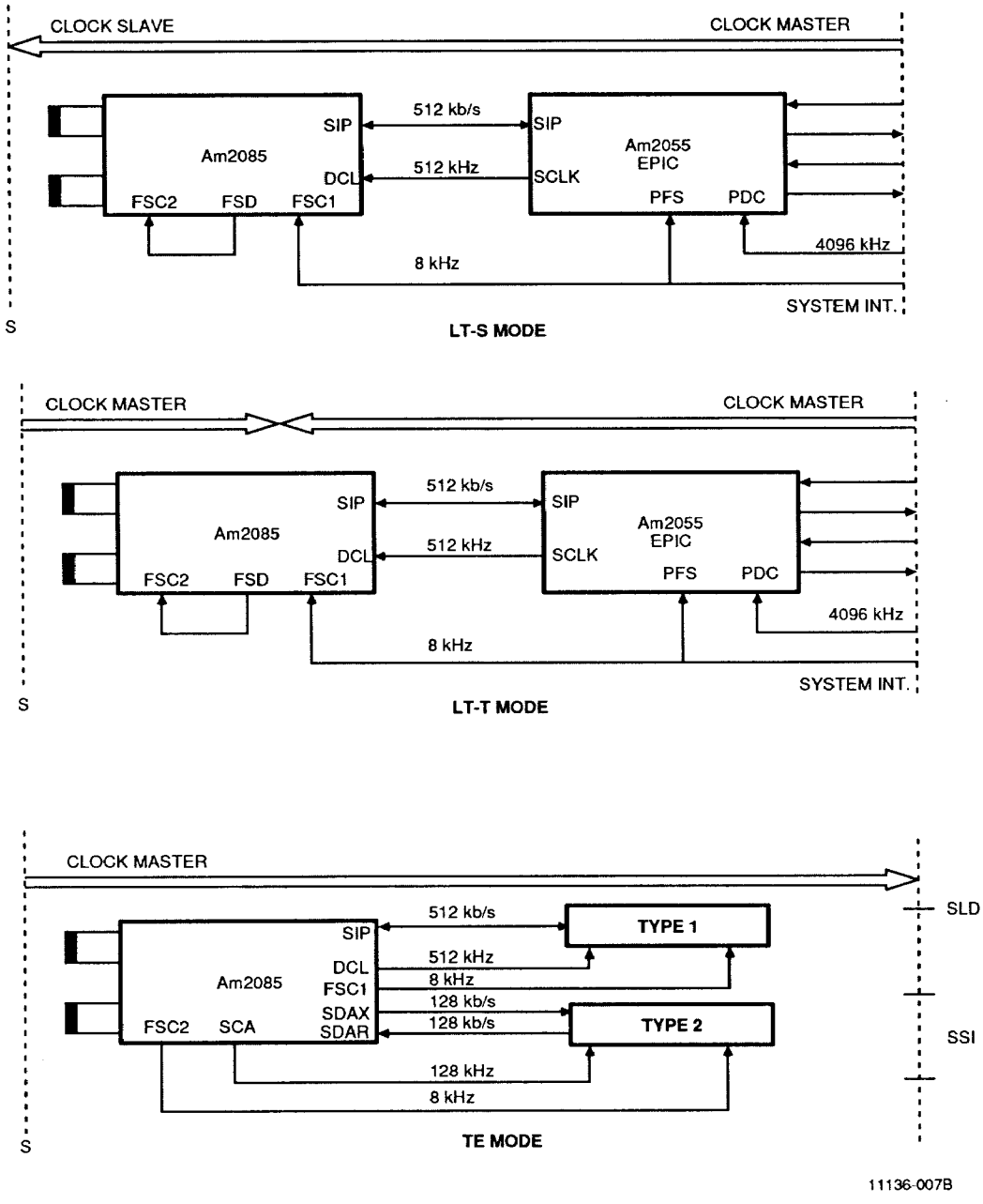


Figure 7. Operating Modes of ISAC-S

Interfaces

The ISAC-S serves three different user-oriented interface types:

- parallel processor interface to higher layer functions
- SSI and SLD as interfaces for B-channel sources/destinations
- IOM interface; to the Layer 1 functions of the ISDN basic access (TIC bus)

Microprocessor Interface

The microprocessor interface consists of bus transceiver, address register, and bus control logic. Via this interface, the ISAC-S can be connected to the multiplexed address/data bus of a microcontroller system. The following functions can be performed by writing and reading special registers in the ISAC-S (see Detailed Register Description section):

- Transfer of data packets in the D-channel
- Control of Layer 2 functions for the ISDN basic access
- Switching of B-channels
- Access to the B-channels
- Control of Layer 1 functions for the ISDN basic access
- Support of diagnostic functions

In the case of special events in the ISAC-S, the processor is notified by interrupt. The interrupt source can be determined and acknowledged by means of the ISAC-S registers ISTA, EXIR, and MASK (see Detailed Register Description).

Serial Synchronous Interface (SSI)

The serial port SSI serves as a full-duplex connection to B-channel sources/destinations in terminal equipment with a data rate of 128 kb/s. SSI consists of one data line for each direction (SDAX and SDAR), the 8-kHz frame synchronization signal (FSC1 and/or FSC2), and the 128-kHz clock signal (SCA/FSD). This serial interface allows the possible connection of serial synchronous transceiver devices (USART Am82520 HSCC) and various CODEC filters directly to the ISAC-S, as illustrated in Figure 8.

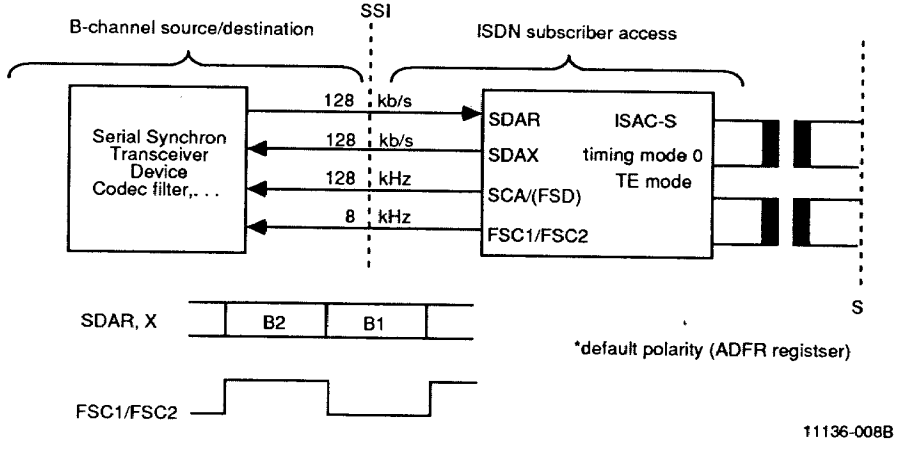


Figure 8. Connection of B-channel Sources/Destinations to the ISAC-S via SSI

Programming the FSC1/FSC2-bit in the ADFR register makes it possible to independently program the strobe signals FSC1/FSC2 so that either B1 or B2 is selected for further processing by the terminal device. The microcontroller system has access to B-channel data via the ISAC-S registers BCR1/BCR2 and BCX1/BCX2.

The microprocessor access must be synchronized to the serial transmission process by means of the Synchronous Transfer Interrupt (STCR; see Detailed Register Description).

SLD Interface

The standard SLD interface is a three-wire interface with a 512-kHz clock (DCL), an 8-kHz frame direction signal (exchange: FSC1 only, terminal: FSC1 and FSC2), and a serial ping-pong data lead (SIP) with an effective full-duplex data rate of 256 kb/s.

The SLD interface can be used in:

- Terminal configurations (timing mode "0") as a full-duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations.
- Digital exchange configurations (timing mode "1") as a full-duplex time-multiplexed connection of B-channel sources/destinations, in this case the ISAC-S itself, to a peripheral board controller. In a typical line-card application the PBC performs time slot assignment of the B-channels to PCM highways, building a system interface to a switching network and a central processor as shown in Figure 10.

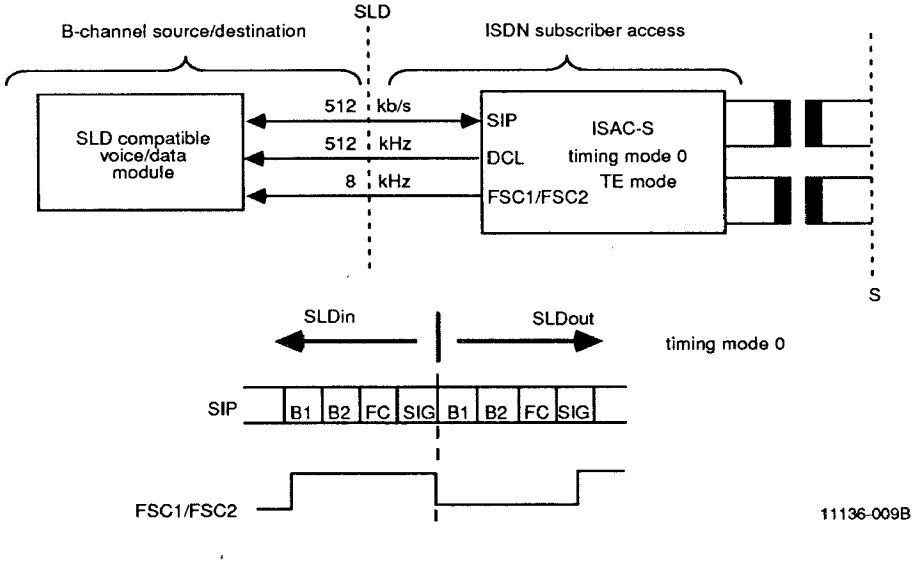


Figure 9. Connection of B-channel Sources/Destinations to the ISAC-S via SLD

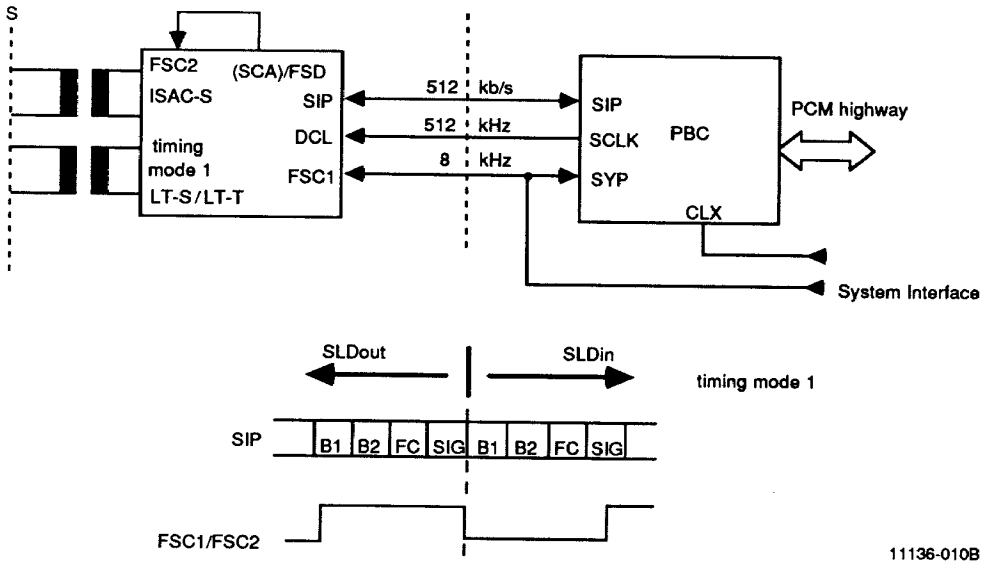


Figure 10. Connection of the ISAC-S as B-channel Source/Destination to a Peripheral Board Controller (PBC)

1

The microcontroller system has access to B-channel data, the Feature Control Byte (FC) and the Signaling Information (SIG) via the ISAC-S registers:

- BCR1/2 and BCX1/2 <—B1/B2
- SFCR <—FC
- SSGR and SSGX <—SIG

The microprocessor access to BCR1/2, BCX1/2 and SFCR must be synchronized to the serial transmission process by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

ISDN Oriented Modular (IOM) Interface

Although the ISAC-S combines the Layer 1 functions of an Am2080 S-bus transceiver (SBC) with the HDLC functions on one chip, the IOM interface is externally still available for Telecom IC (TIC) bus applications. The TIC bus allows the possible connection of up to seven additional IOM-compatible Communications Controllers via the Layer 1 functions of the ISAC-S to CCITT's S interface as shown in Figure 11.

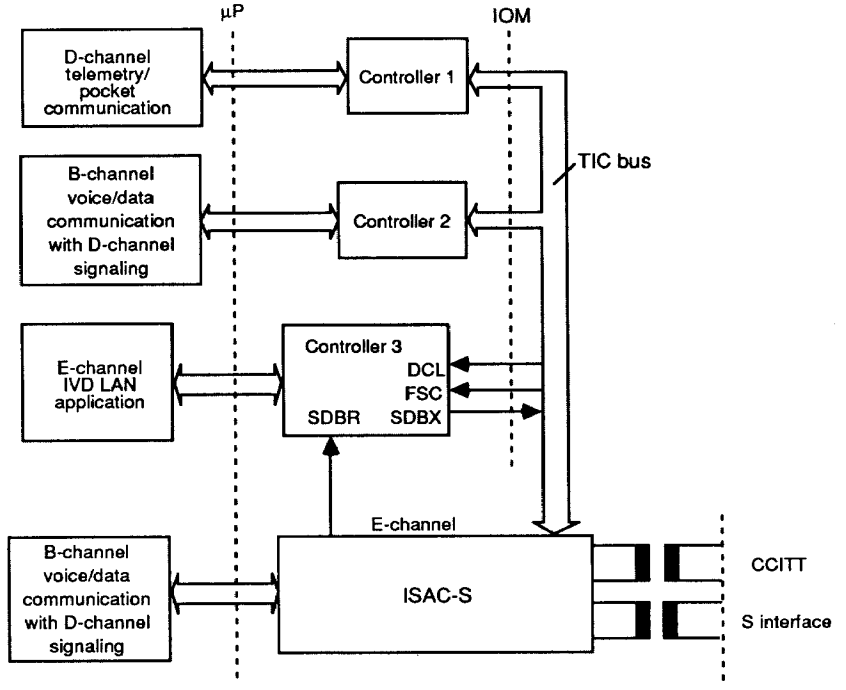


Figure 11. Typical TIC Bus Application

The IOM interface consists of one data line per direction (SDBR and SDBX). Three additional signals define the data clock (DCL) and the frame synchronization (FSC1/FSC2) at this interface. These signals are internally derived from the S interface and are delivered by the ISAC-S in timing mode 0 (terminal).

In timing mode 1 (exchange), the clock and a synchronization signal are provided by the system. In this case, the IOM interface is synchronization by a synchronization signal SCA/FSD, delayed in time with respect to the frame synchronization signal supplied by the system. This reduces the round-trip delay time (see Figure 12).

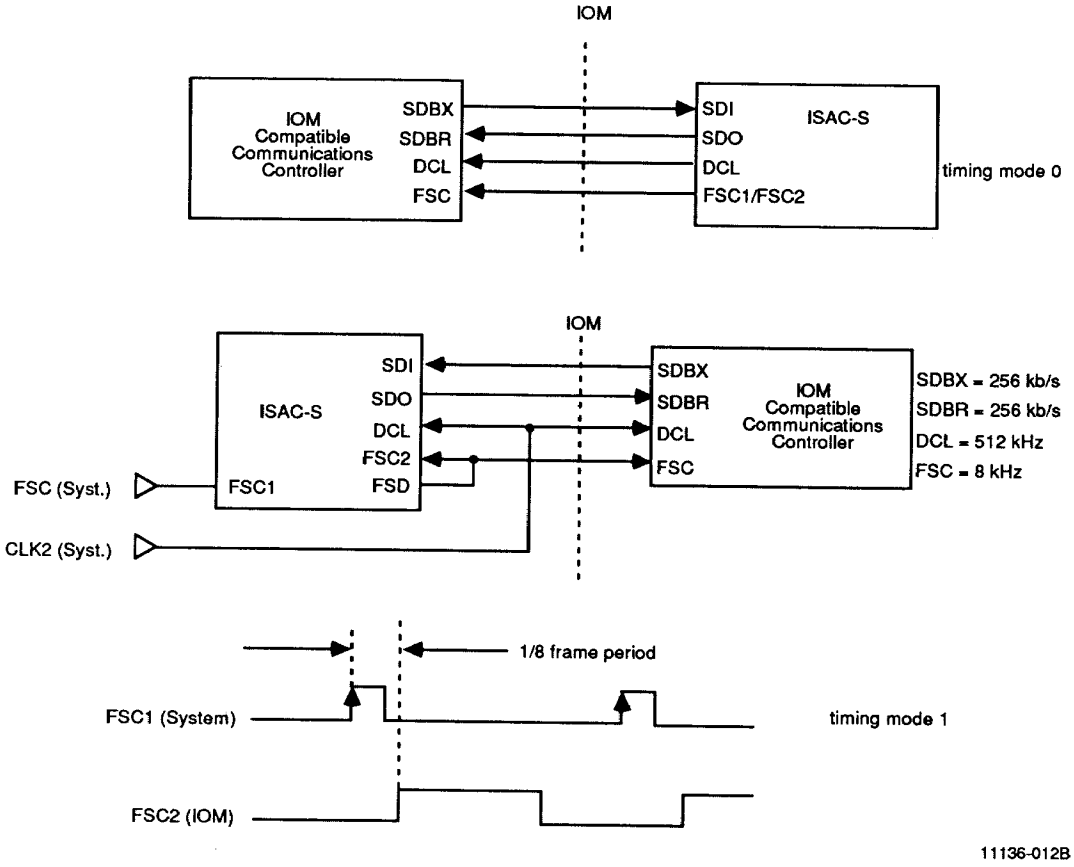


Figure 12. IOM Interface Signals

The IOM interface has two different clocking states:

- Idle state <— FSC1/FSC2 and DCL are disabled and both data lines are logical High (power down)
- Clocked state <— FSC1/FSC2 and DCL are enabled (stand by)

Unlike digital exchange configurations in which the IOM interface always remains in the synchronized state, in terminal equipment both clock states can be selected.

The transition from idle state to clocked state will be automatically initiated by an incoming call from network side. An activation of the IOM interface from the subscriber end has to be programmed in this case by setting and resetting the SPU-bit in the SPCR register, before the IOM interface can be used (that is, for the activation/deactivation procedure at the S interface, see Operational Description section).

The IOM Channel Structure

The channel frame structure of the IOM interface and the related channel capacity are defined in Figure 13 as follows:

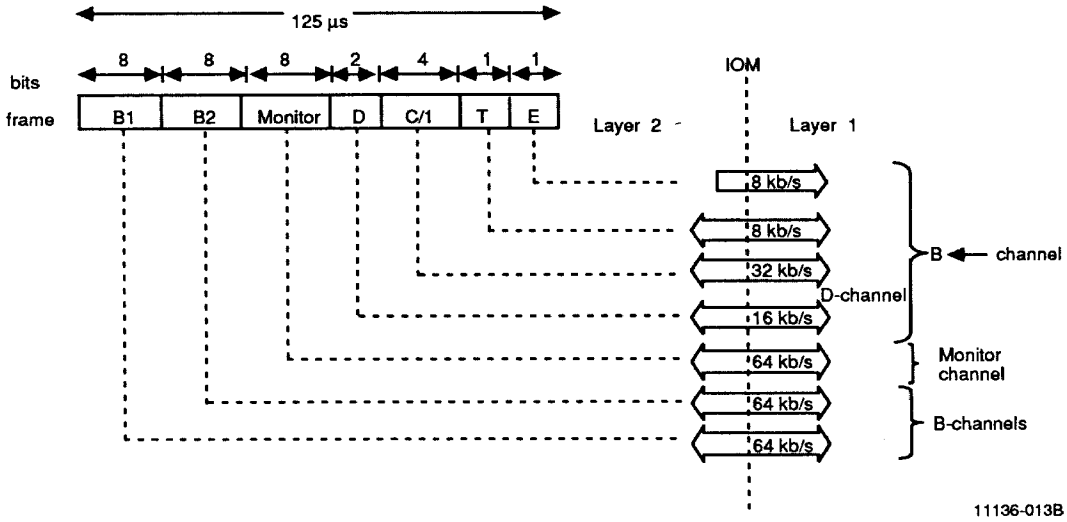


Figure 13. IOM Channel Capacity

In the ISAC-S, the monitor channel supports the TIC bus access mechanism as well as the indication of the S-bus status (D-channel access). The ISAC-S indicates by means of monitor bit 3 (BAC) whether or not it occupies the TIC bus (B-channel).

The control of the Layer 1 functions, especially the activation/deactivation procedure at the S interface, will be done by the exchange of special 4-bit C/I-codes in the C/I channel.

The T-channel, which is fully transparent, and the E-channel are reserved for future use.

TIC Bus

The TIC bus is operated in point-multipoint configuration. It uses a wired-OR connection of the data outputs to enable the TIC bus access mechanism. Therefore the ISAC-S contains an internal pull-up resistor at the SDI pin.

The TIC bus is controlled by a collision resolution mechanism in the monitor channel similar to the D-channel access on the S-bus.

Individual Functions

Distinctive functions for the ISDN basic access realized in the ISAC-S are:

- B-channel switching
- Layer 1 functions
- Layer 2 functions
- Terminal-specific functions
- Test functions

B-Channel Switching

The ISAC-S contains two serial synchronous interfaces which can serve as interfaces to B-channel sources/destinations.

- SSI —> 128 kb/s data rate, B1 and B2
  —> one data line per direction
- SLD —> 256 kb/s data rate, B1 and B2 (and also FC and SIG)
  —> one data line for both directions (ping-pong)

Both channels B1 and B2 can be switched independently of one another to the IOM interface and to the four-wire S interface. Furthermore, it is possible to program a loop for B-channel data received from the IOM or SLD interface. The microcontroller can select the B-channel routes in the SPCR register and has access to the B-channels by writing or reading the BCR/BCR2 and BCX1/BCX2 registers (Figure 14). Synchronization to the 8-kHz frame is done by means of a Synchronous Transfer programmed in the STCR register (SIN Interrupt indicated in the ISTA register and SOV interrupt in EXIR).

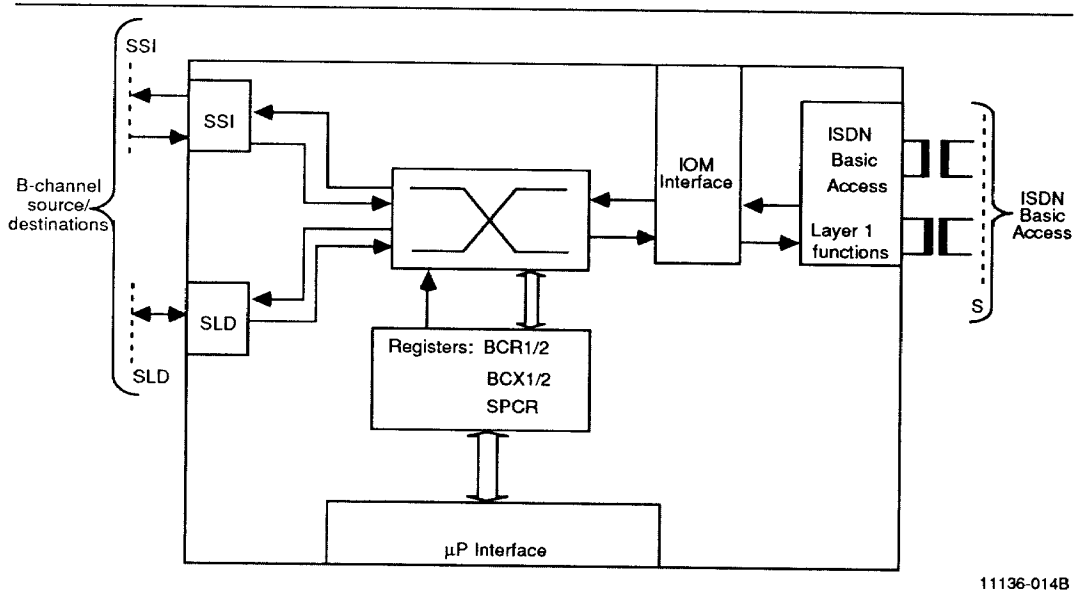
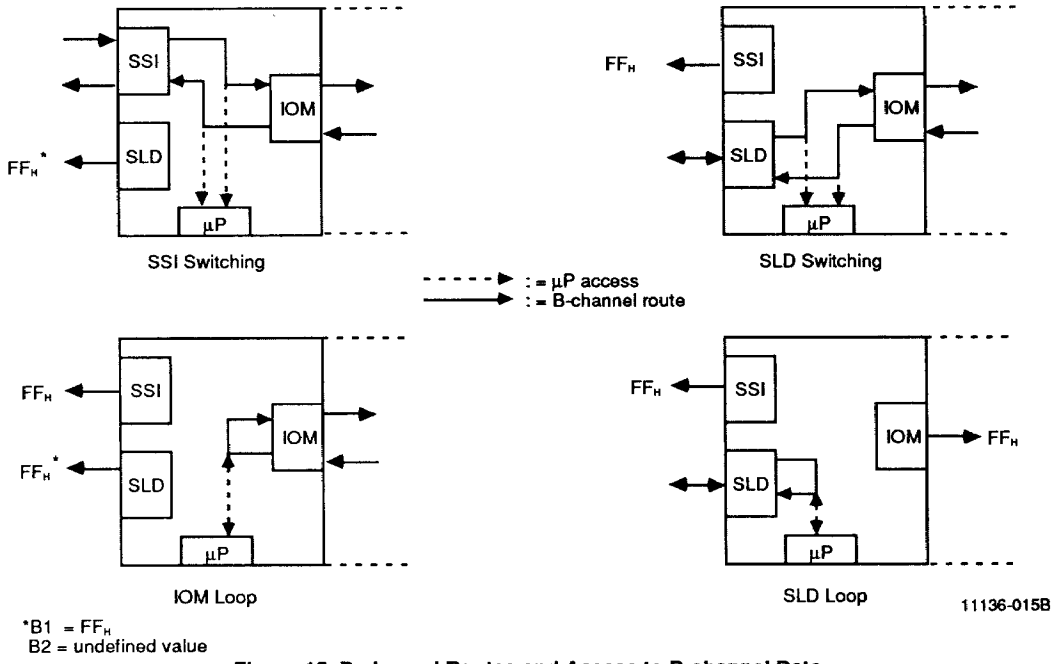


Figure 14. Principle of B-channel Switching

In Figure 15 all possible selections of the B-channel routes and access to B-channel data via the micoprocessor interface are illustrated.



*B1 = FF$_H$
B2 = undefined value

Figure 15. B-channel Routes and Access to B-channel Data

Layer 1 Functions for the ISDN Basic Access

The S-bus interface circuit in the ISAC-S performs the Layer 1 functions for the S/T interface of the ISDN basic access according to CCITT I.430. The distinctive functions are listed below:

- S-bus transceiver according to CCITT I.430
- Recovery of clock and frame in all applications
- Frame alignment for trunk line termination
- Implementation of activation/deactivation procedures
- Switching of test loops
- Level detection in power-down state

The wiring configurations in user premises, in which the ISAC-S can be used, are illustrated in Figure 16.

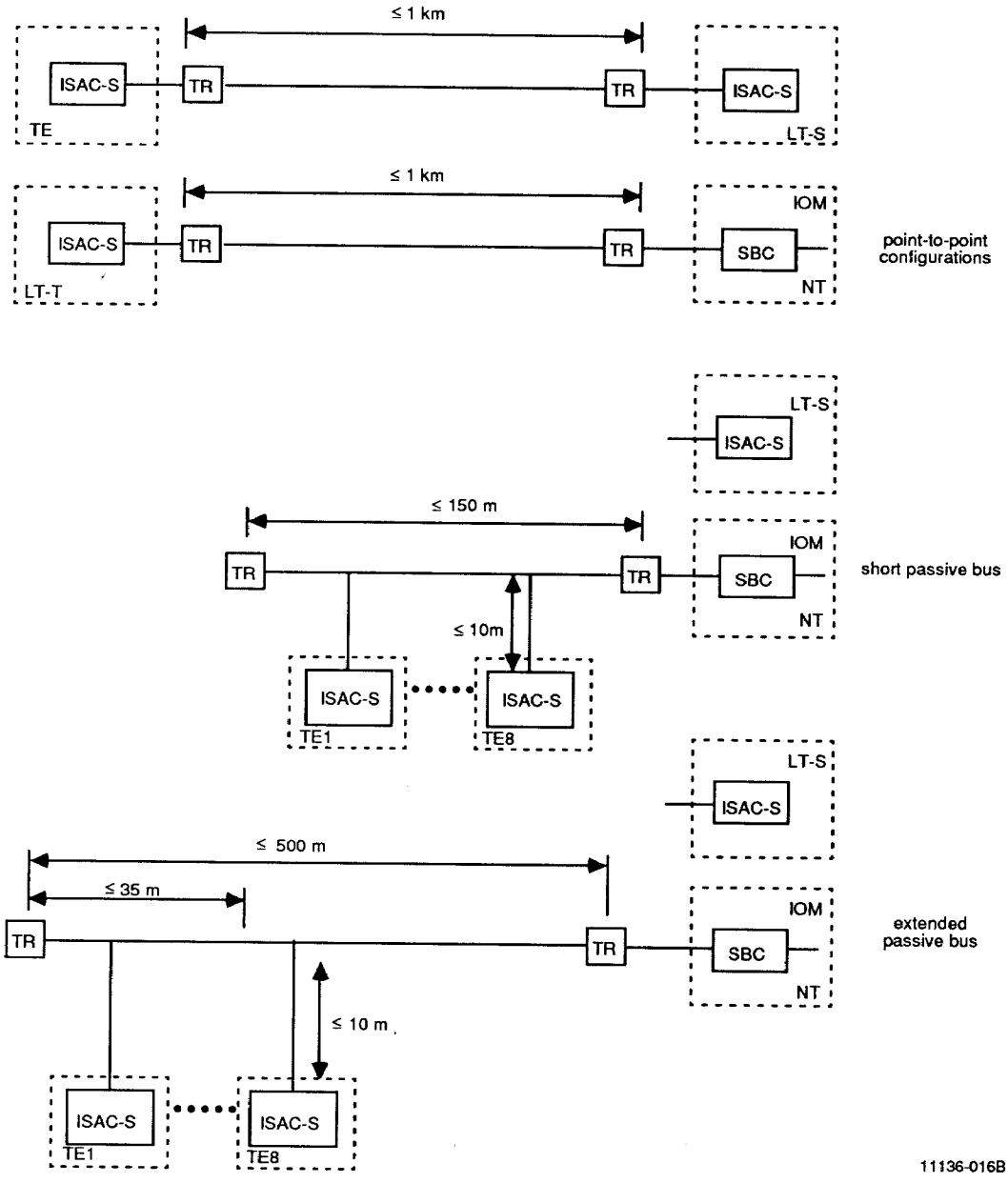


Figure 16. Wiring Configurations in User Premises

"S" Interface

According to CCITT recommendation I.430, a modified AMI code with 100% pulse width is used on the S interface. A logical 1 corresponds to a neutral level (no current), whereas logical 0s are coded as alternating positive and negative pulses. An example of a modified AMI code is shown in Figure 17.

One S-frame consists of 48 bits at a nominal bit rate of 192 kb/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1+B2+D structure defined for the ISDN basic access (total useful data rate: 144 kb/s). Frame beginning is marked using a code violation. The frame structures (from network to subscriber and subscriber to network) are shown in Figure 18.

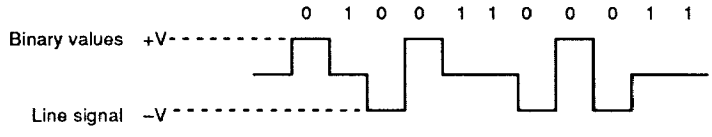


Figure 17. Modified AMI Code

System Integration

The basic architecture for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals, PABX system and the NT in the user area as depicted in Figure 18.

The NT equipment simply serves as a link between the U interface on the exchange and the S interface on the user side. The NT itself may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between Layer 1 of S and Layer 1 of U. NT2 also includes the complex functions like multiplex and exchange functions in higher layer OSI functions.

The ISAC-S is specifically designed for the user area of the ISDN basic access, especially Terminal and PABX exchange equipment. Figure 19 illustrates the general subscriber access architecture in the user area of the ISDN basic access including Terminal and PABX equipment.

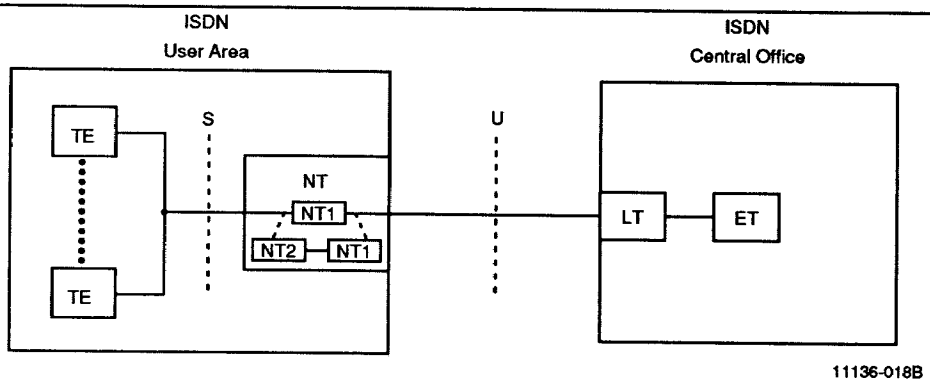


Figure 18. ISDN Architecture for the Basic Access

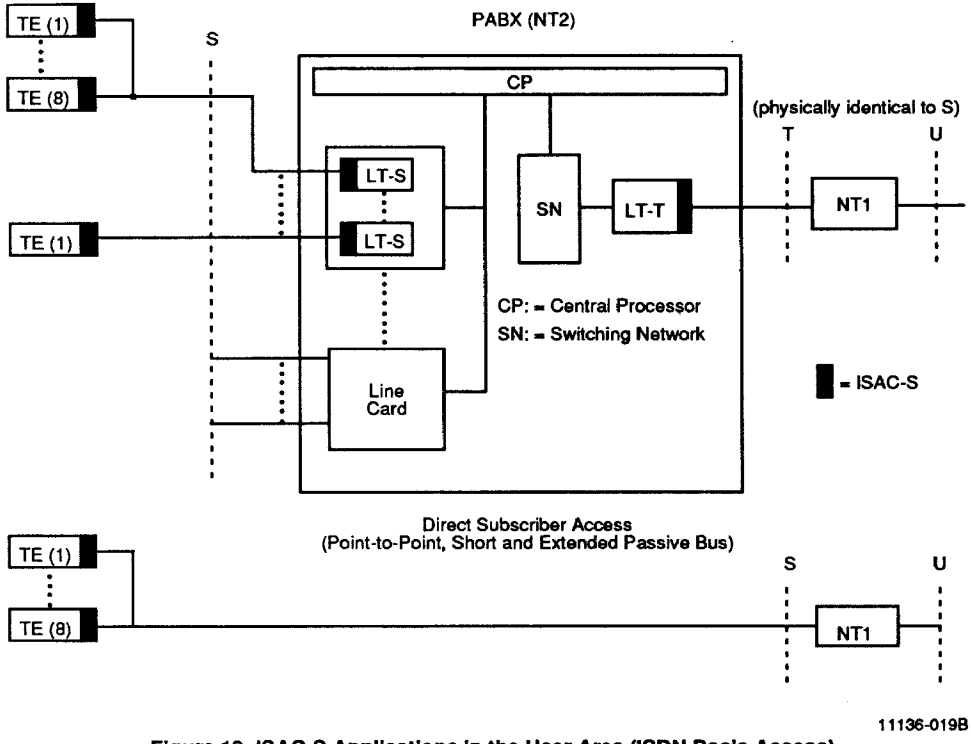


Figure 19. ISAC-S Applications in the User Area (ISDN Basic Access)

The concept of the ISDN basic access is based on two circuit-switched 64 kb/s B-channels and a message-oriented 16 kb/s D-channel for packetized data, signaling, and telemetry information.

The two serial interfaces of the ISAC-S, SLD, and SSI can be used as interfaces for B-channel sources/destinations, and the IOM interface in TIC-bus configuration provides the possibility of connecting further D-channel link entities to the S-bus.

Via the microprocessor interface, the microcomputer system can select the B-channel switching, can transmit/receive data packets in the D-channel, and has control over various functions (Layer 2, Layer 1, diagnostic, . . .).

To get a general idea, the following figures illustrate the ISAC-S integration into typical ISDN applications.

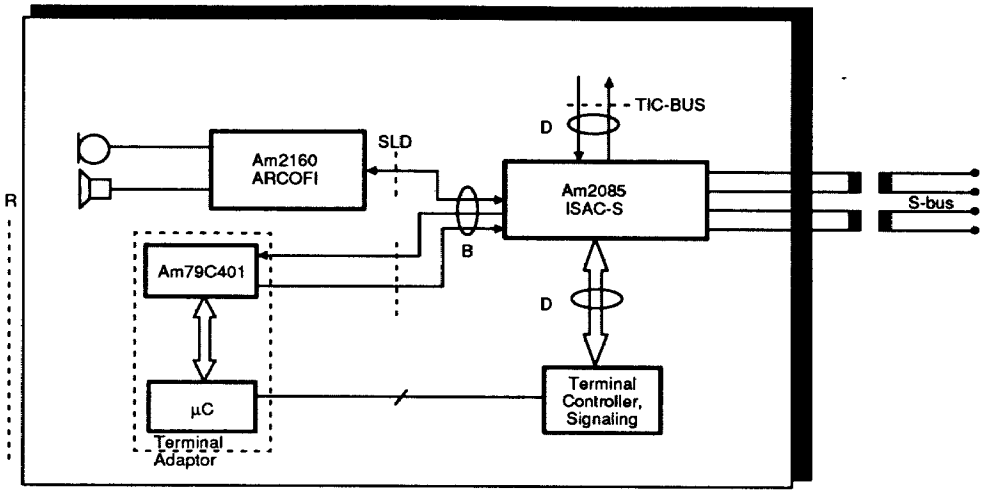
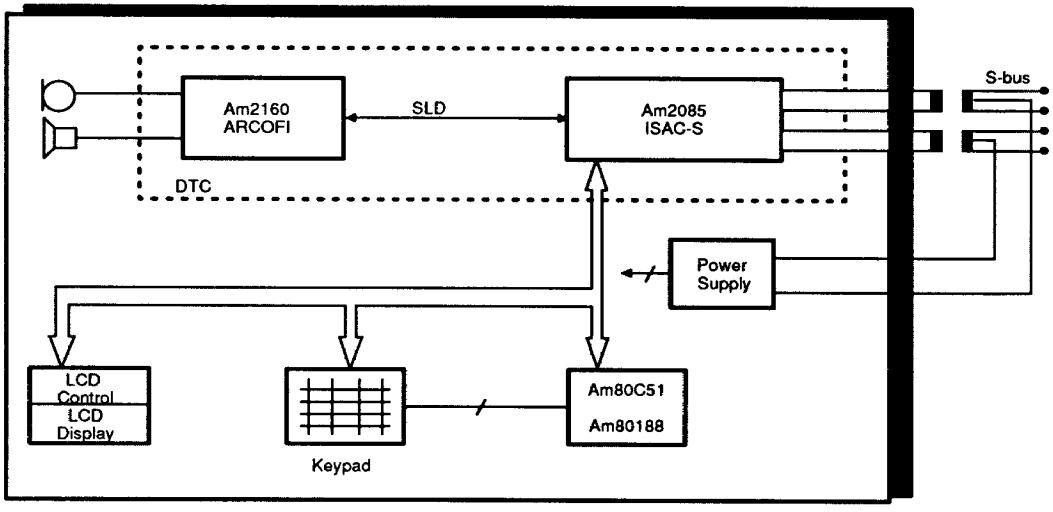


Figure 20. Extended ISDN Terminal (Voice/Data Workstation) 11136-020B



11136-021B

Figure 21. Basic ISDN Feature Telephone

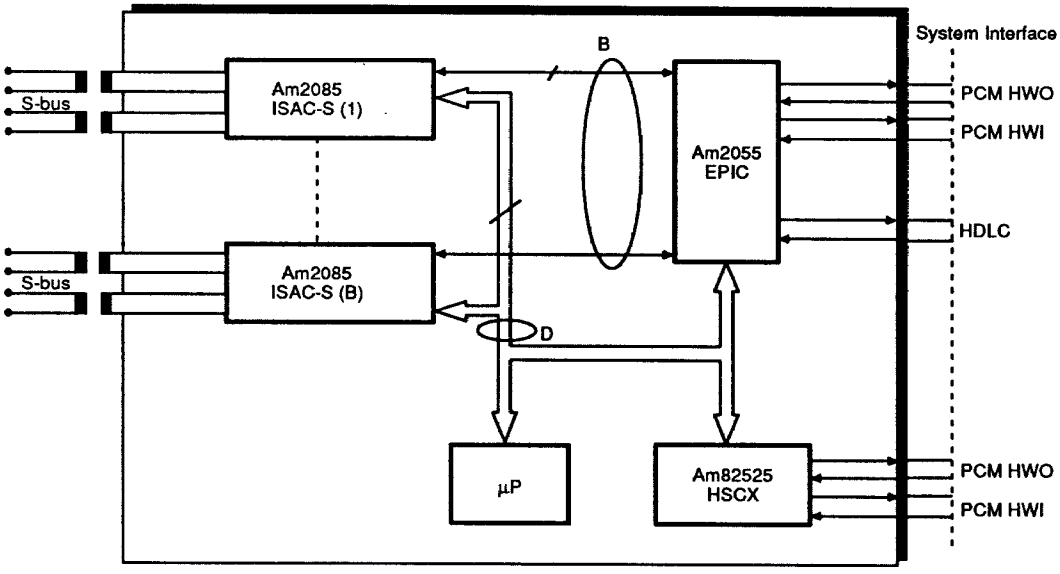


Figure 22. ISDN Line Card for PABX

11136-021B

Microprocessor Environment

The ISAC-S is especially suitable for cost-sensitive applications with single-chip microcontrollers (that is, Am8031, Am8051). Due to its bus structure (8-bit multiplexed address/data bus) and non-critical bus timing, it also fits perfectly into almost every 8-bit microprocessor system environment (that is, 8085, 8088, 80188).

With minimum hardware or software expense, it is also possible to use the ISAC-S with 16-bit microprocessors (that is, 8086, 80186). Figure 23 gives an example of the integration of ISAC-S in an 80C51 or 80188 system.

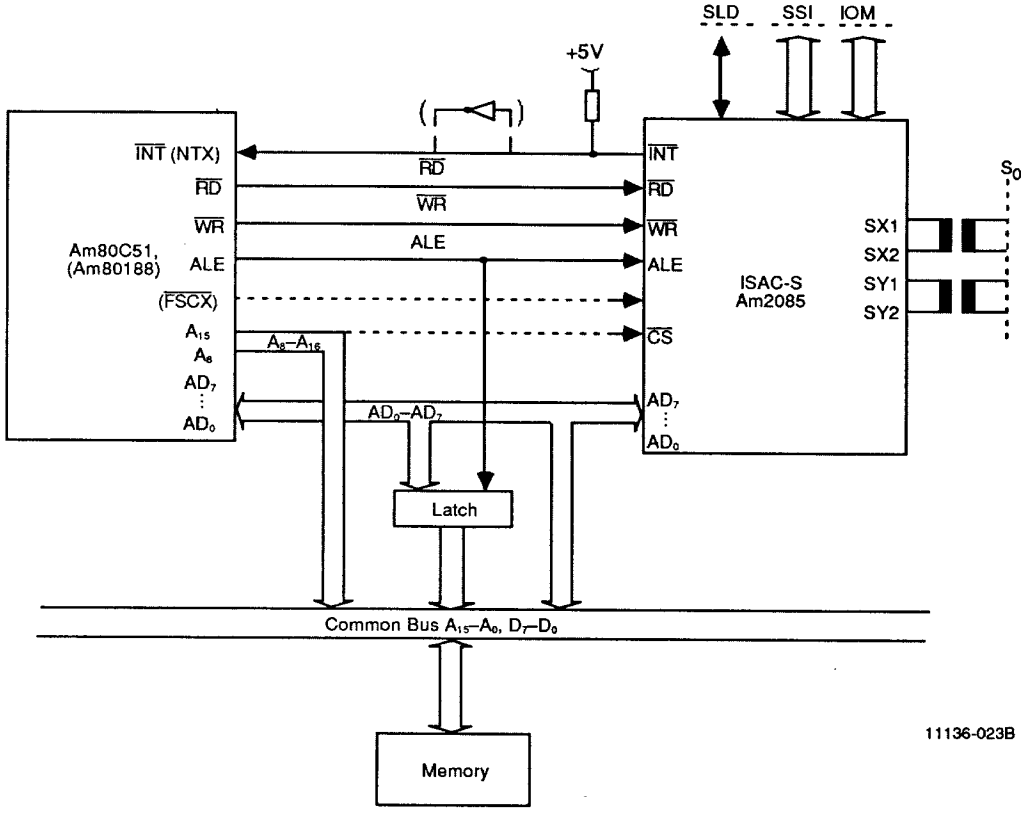
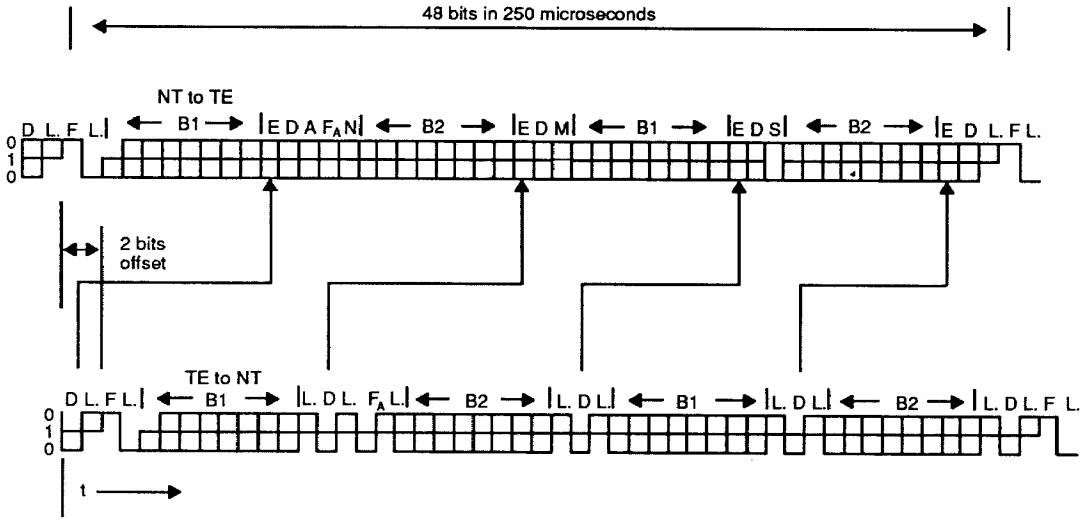


Figure 23. Example of Integration of ISAC-S in an Am80C51 or Am80188 System



A = bit used for activation
B1 = bit within B channel 1
B2 = bit within B channel 2
D = D-channel bit
E = D-echo-channel bit
F = framing bit
F_A = auxiliary framing bit or Q-bit
L = DC balancing bit
M = multiframing bit
N = bit set to a binary value N = F_A
S = reserved for future standardization

11136-024B

Note: Dots demarcate those parts of the frame that are independently DC-balanced.

Figure 24. Frame Structure at Reference Points S and T (CCITT I.430)

Analog Functions

The full-bauded AMI pulse shaping is achieved with the integrated transmitter which is realized as a voltage limited current source. A current of 7.5 mA is delivered over SX1-SX2, which yields a voltage of 1.5 V over 200 ohms.

The receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

An external transformer of ratio 2:1 is needed in both receive and transmit directions to provide for isolation and to transform voltage levels according to CCITT recommendations.

Level Detection Power Down (TE mode)

In power-down state, only an analog level detector is active. All clocks, including the IOM interface, are stopped. The data lines are High, whereas the clocks are Low.

An activation initiated from the exchange side (Info 2 on S-bus detected) will have the consequence that a clock signal is provided automatically. From the terminal side, an activation must be started by setting and resetting the SPU-bit in the SPCR register (see Detailed Register Description section).

Timing Recovery

A DPLL circuitry working with a frequency of 7.68 MHz ±100 ppm serves to generate the 192-kHz line clock from the reference clock delivered by the network and to extract the 192-kHz line clock from the receive data stream.

The 7.68-MHz clock may be generated with the help of an external crystal between pins XTAL1 and XTAL2. It may also be provided by an external oscillator.

The buffer memory serves to adapt the different bit rates of the S and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503.

Activation/Deactivation

An incorporated finite state machine controls ISDN Layer 1 activation/deactivation according to CCITT.

D-Channel Access

The D-channel access procedure according to CCITT I.430, including priority management, is fully implemented in the ISAC-S. When used in LT-S (NT) mode in a multipoint configuration, the device generates the echo bits necessary for D-channel collision detection.

Q-Channel Support

In terminal applications (TE), the Q-channel as specified by I.430 is supported. In case the ISAC-S in the terminal has received a binary one in F_A-bit position, it will reflect this binary one in the next S frame (also F_A-bit position) from TE to NT. This allows another terminal to use the extra transmission capacity.

Control of Layer 1

The control of the Layer 1 functions, especially the activation/deactivation procedure at the S interface, will be done by the exchange of special 4-bit Command/Indication codes in the C/I channel (see Operational Description section).

Layer 2 Functions for the ISDN Basic Access

LAPD, Layer 2 of the D-channel protocol (CCITT I.441) includes functions for :

- Provision of one or more data link connections on a D-channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI).
- HDLC-framing
- Application of a balanced class of procedure in point-multipoint configuration.

The simplified block diagram in Figure 25 shows the functional blocks of the ISAC-S which support the LAPD protocol.

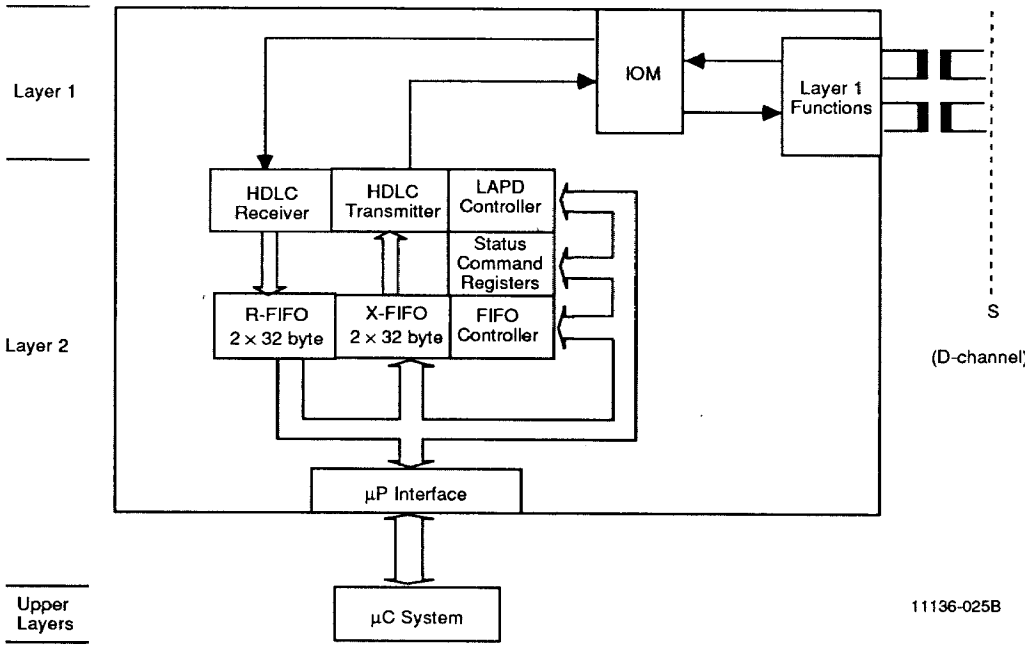


Figure 25. D-Channel Processing of the ISAC-S

For the support of LAPD, the ISAC-S contains an HDLC transceiver which is responsible for flag generation/recognition, bit stuffing, CRC-check and address recognition. In the auto mode, the LAPD controller handles the control field utilization and parts of LAPD procedures (information transfer in multiple frame operation with window size of 1).

A FIFO structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO controller permits flexible transfer of protocol data units to and from the microcontroller system. Programming of the several modes and control of message transfer is done via status, command, and mode registers (see Operational Description and Detailed Register Description sections).

For the address recognition, the ISAC-S contains the registers SAP1, SAP2 for an individual SAPI address (fixed value for Group SAPI) and TEI1, TEI2 for an individual TEI address. The C/R-bit interpretation can be programmed according to network or user side in the SAP1 register (CRI-bit). The control field format for the optional modulo 128 operation can be selected in the SAP2 register (MCS-bit).

Message Transfer Modes

The ISAC-S supports Layer 2 of the D-channel protocol (LAPD) with different capabilities depending on the selected message transfer mode.

- **Auto mode**

  The ISAC-S processes all S- and I-frames of a logical link fully autonomously, according to CCITT I.441.

  During the "communication procedure," dialogue between the ISAC-S and processor is not necessary. The ISAC-S reports the status of the procedure to the processor. The Layer 2 software remaining in the microcontroller system is used for initialization and error recovery. As a prerequisite for this mode, window size 1 must be used between transmitted and acknowledged frames.

- **Non-auto mode**

  In this mode the control field and the information field of an HDLC frame is forwarded directly to the processor. The Layer 2 address recognition is still performed.

- **Transparent modes**

  The address field is either partly checked by the ISAC-S (SAPI) or completely forwarded to the processor. The Layer 2 headers are either stored in special purpose registers (transparent mode) or, together with the information field, in the FIFO buffer (extended transparent mode).

The three major types of message transfer mode and the corresponding Layer 2 functions in the ISAC-S are illustrated in Figure 26 in relation to the ISO's OSI reference model.

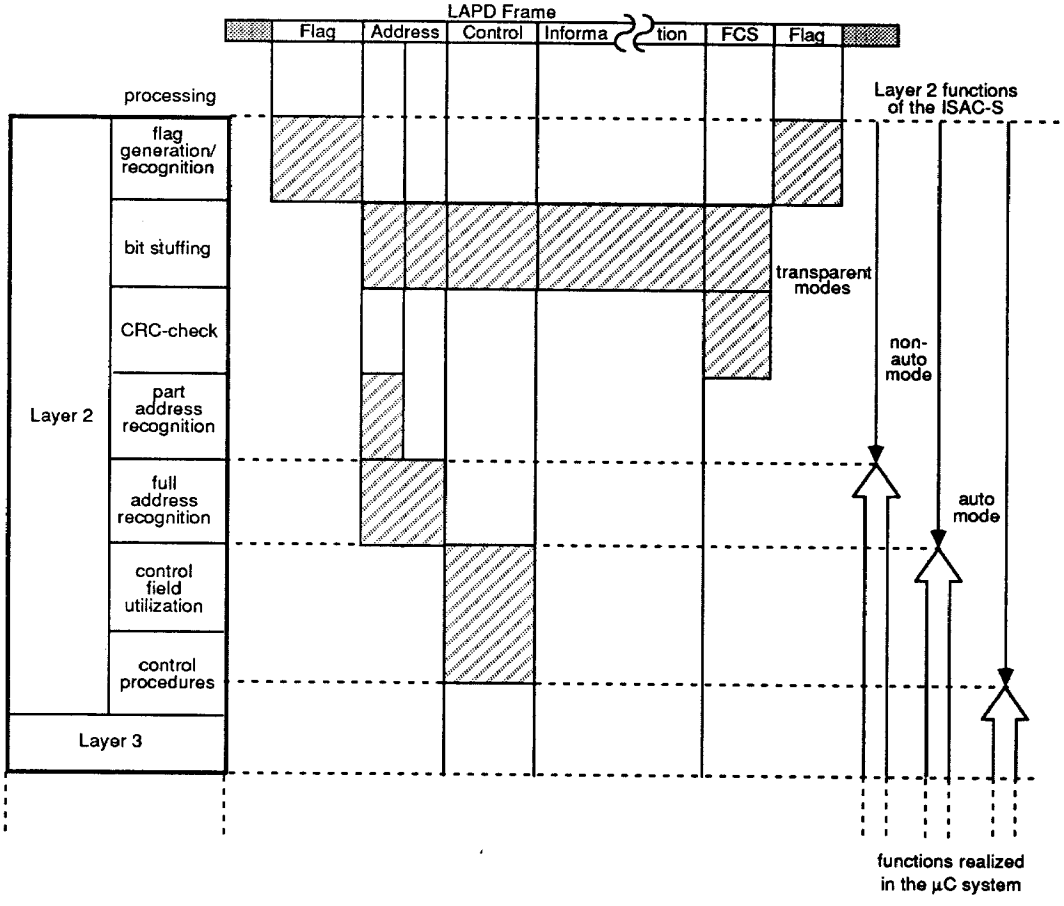


Figure 26. D-channel Protocol Support of the ISAC-S 11136-026B

Reception of Frames

Depending on the selected message transfer mode, the protocol data (address, control and information field) of a received frame will be stored in the RFIFO as well as in additional registers (RHCR, TEI1). The processor will be informed by an appropriate interrupt and must react within a corresponding reaction time.

The RFIFO and the FIFO-controller have been so designed that the maximum microprocessor reaction time is 16 ms for messages of more than 32 octets. The processor will be informed about the receiver operation (status) chiefly by means of the two interrupts:

- RPF (Receive Pool Full)
- RME (Receive Message End) —> ISTA (see Detailed Register Description)

When one of the two receive pools is filled up completely, the ISAC-S generates an RPF interrupt.

If the processor wants to save the frame, it should, as a consequence, react by reading the 32 bytes out of the RFIFO within the maximum reaction time.

During a handshake procedure between ISAC-S and microcontroller system, the processor has to acknowledge the reading by means of the RMC (Receive Message Complete) command.

When the end of a frame is detected, an RME interrupt will be generated, indicating that the remainder of the current frame is now available in one of the two receive pools. The reception of the last part of a frame must also be completed with an RMC command (see Operational Description).

With respect to the RME interrupt, the ISAC-S provides additional information about the received frame in its internal registers, according to Table 10.

Transmission of Frames

The processor initiates the transmission of a message with one of the two commands:

- XTF (Transmit Transparent Frame)
- XIF (Transmit I-frame, in auto mode only) —> CMDR

after it has written up to 32 bytes in one of the two 32-byte pools of the XFIFO.

When one pool is empty an XPR interrupt alerts the processor. The processor can then write further data to the XFIFO and enable the continuation of frame transmission according to a handshake procedure with the appropriate transmit command XIF of XTF (see also Interrupt List).

The microcontroller must indicate the message end with an XME command (together with the appropriate transmit command XIF or XTF) for the following cases:

- The message length is shorter than or equal to 32 bytes and all data is entered into the XFIFO or
- The last part of a longer message is written into the XFIFO

Table 10. Received Frame Information Saved in the Internal Registers

Information	Register	Bit	Mode
SAPI of LAPD address field	TEI1		Extended transparent mode 0
TEI of LAPD address field	TEI1		Extended transparent mode 1
			Transparent mode
	RHCR		Extended transparent mode 0
LAPD control field	RHCR		Auto mode
			Non-auto mode
			Transparent mode
			Extended transparent mode 1
Type of frame (Command/Response)	RSTA	C/R	—
Result of CRC-check (positive/negative)	RSTA	CRC	—
Data available in RFIFO (yes/no)	RSTA	RDA	—
Abort condition detected (yes/no)	RSTA	RAB	—
Data overflow during reception of a frame (yes/no)	RSTA	RD0	—
Recognition of Data Link Connection	RSTA	SA0	Auto mode
Identifier (DLCI = SAPI + TEI)		SA1	Non-auto mode
		TA	
Number of bytes received in RFIFO	RFBC	5–0	—
Message length (≤ 223)	RFBC	7–0	—

An XPR interrupt will also be generated subsequent to:

- The complete transmission of a transparent frame after the XTF and XME command or
- The reception of a positive acknowledge after the XIF and XME command or
- When no frame transmission is in progress and the microprocessor gives the XRES command

The message will be aborted automatically:

- When there is no more data in the XFIFO ready to be transmitted or
- When the processor gives an XRES command

The ISAC-S then transmits an abort sequence and generates an XDU interrupt.

Collisions that occur on the S-bus (D-channel) up to the 32nd data byte of a frame are treated without microprocessor interaction. The ISAC-S will retransmit the frame automatically. If the collision is detected later than the 32nd data byte of a frame, the ISAC-S aborts the frame and requests the processor to repeat the frame with an XMR (Transmit Message Repeat) interrupt.

In every mode, the start flag will be inserted automatically, as are likewise the end flag and the frame check sequence (CRC-16 according to LAPD) which are appended after an XME command.

When auto-mode I-frames are transmitted, the LAPD controller of the ISAC-S generates in addition to the delimiting flags and the FCS field, the address and control field autonomously. In this mode the XFIFO contains only the data for the information field.

The status of the XFIFO can also be read from the STAR register (XFW-bit: XFIFO write enable). This allows for a polling procedure instead of or in addition to the XPR interrupt and can be useful when there is no need to transmit a high quantity of messages (referred to the D-channel capacity).

Layer 2 Functions in the Auto Mode

In addition to address recognition, all S- and I-frames are processed independently by the ISAC-S in the auto mode with window size 1. The control field format may be either for basic (modulo 8) or extended (modulo 128) operation. The following functions are performed:

- Update of transmit and receive counter
- Evaluation of transmit and receive counter
- Processing of S commands
- Flow control with RR/RNR
- Response generation
- Recognition of protocol errors
- Transmitting of S commands, if an acknowledgment is not received
- Continuous status query of remote station after RNR has been received
- Programmable timer/repeater functions

Terminal-Specific Functions

In addition to the ISAC-S standard functions supporting the ISDN basic access, the ISAC-S contains optional functions, useful in various terminal configurations:

- Subscriber Awake (using SIP/SAW line)
- Watchdog Timer

The terminal-specific functions, STCR, SPCR, and CIXR registers (see Detailed Register Description), make it possible to generate a Reset signal as well as the appropriate interrupt in the following cases:

- Power Down
  - —Subscriber Awake—initiated by a falling edge on the SAW line (SAW interrupt)
  - —Exchange Awake—initiated by a message from Layer 1 (CIC interrupt)
- Power Up
  - —Watchdog Timer—after expiration of the internal watchdog timer (WOV interrupt)

The reset pulse generated by the ISAC-S has a pulse width of 5 ms and is an active High signal. During one time period of 128 ms, the WTC1- and WTC2-bit of the ADFR register must be set consecutively in the following manner:

Steps	WTC1	WTC2
1	1	0
2	0	1

As a result, the watchdog timer is reset and restarted.

Test Functions

The ISAC-S provides several test and diagnostic functions which can be grouped as follows:

- Closing loops in the transmission path; that is;
  - —loop internally inside the B-channel switching circuit (B-channel IOM loop) see B-Channel Switching)
  - —loop internally at the IOM interface, with reduced timer resolution (IOM interface loop), SPCR: TLP-bit, (see Detailed Register Description)
  - —loop at the analog end of the S interface (see Interrupt List)
- Using the IOM interface as an HDLC port without IOM frame structure (D-channel splitting) and no Layer 1, MODE and ADFR: TEM-bit, (see Detailed Register Description)
- Sending of special test signals on the S-bus, according to the modified AMI code; that is;
  - —single zeros (SSZ, 2 kHz repetition rate)
  - —continuous zeros (SCZ, 96 kHz repetition rate) (see Layer 1 Functions for the ISDN Basic Access; also see Processing)

DETAILED REGISTER DESCRIPTION

The parameterization of the ISAC-S as well as transfer of data and control information between the microprocessor and ISAC-S is performed with the R- and XFIFO and two register sets (Figure 27). The two FIFOs are accessed with the addresses 00—1FH which are of equal value and are referenced to the respective actual byte in the FIFO.

The special purpose registers of the address range 20-2FH pertain to the HDLC transceiver and LAPD controller as well as to higher-ranking functions in the ISAC-S.

The serial interfaces are controlled and monitored with the register record 30–3FH.

Register Address [1]	Read			Write	
	Name	Description	Name	Description	
00 ... 1F	RFIFO	Receive FIFO		Transmit FIFO	FIFO Buffer
20	ISTA	Interrupt Status Register	MASK	Mask Register	HDLC-Transceiver LADP-Controller, ...
21	STAR	Status Register	CMDR	Command Register	
22	MODE	MODE Register			
23	TIMR	Timer Register			
24	EXIR	Extended Interrupts	XAD1	Transmit Address 1	
25	RFBC	Receive Frame Byte Counter	XAD2	Transmit Address 2	
26	[2]		SAP1	SAPI Address 1	
27	RSTA Receive Status Register		SAP2	SAPI Address 2	
28	TEI1	TEI Address 1		[3]	
29	RHCR Receive HDLC Control		TEI2	TEI Address 1	
2A ... 2F	[4]				
30	SPCR	Serial Port Control			Serial Interface ...
31	CIRR	Command/Indicate Receive	CIXR	Command/Indicate Transmit	
32	MDNR	Monitor Register			
33	SSGR	SLD Signaling Receive	SSGX	SLD Signaling Transmit	
34	SFCR	SLD Feature Control			
35	BCX1	B1-Channel Transmit			
36	BCX2	B2-Channel Transmit			
37	BCR1	B1-Channel Receive	STCR	Synchr. Transfer Control	
38	BCR2	B2-Channel Receive	ADFR	Additional Features	
39 ... 3F					

Notes: 1) Hexadecimal representation of AD0_7
2) Inverted contents of SAP1 when reading
3) Inverted contents of TEI1 when reading auto
4) Invalid address range (data value "00" when reading)

11136-027B

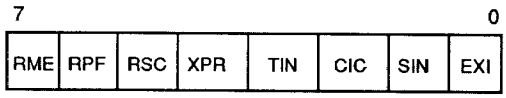
Figure 27. Register Address Arrangement

For quick reference, the page numbers for all registers are listed below:

ISTA—Interrupt Status Register—(Read)

Value after Reset: 00H
Address: 20H

Format:



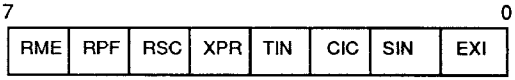
Bit Name	Description
RME	Receive Message End The receive message is now complete. Either one complete message, shorter than 32 bytes, or the remaining part of a longer message has been received. The contents are now available in the RFIFO. The actual message length and additional information may be obtained from the RFBC and the RSTA register.
RPF	Receive Pool Full A 32 byte block of a message, greater than 32 bytes has been received and is now available in the RFIFO. The message is not yet complete.
RSC	Receive Status Change (used in auto mode only) A status change in the receiver of the remote station (receiver ready/receiver not ready) has been detected, due to a received "RR"/"RNR" S-Frame (according to HDLC and LAPD). The current status can be read from the STAR register (RRNR-bit).
XPR	Transmit Pool Ready A data block of up to 32 bytes can be written to the XFIFO. An XPR interrupt will be generated in the following cases: after an XTF or XIF command, when one transmit pool is emptied and the frame is not yet complete after an XTF together with an XME command, when the whole transparent frame has been transmitted after an XIF together with an XME command, when the whole I-frame has been transmitted and a positive acknowledge from the remote station has been received.
TIN	Timer Interrupt The internal timer and repeat counter has expired (see also TIMR register).
CIC	C/I Code Change A change in C/I code has been recognized. The same C/I code, which differs from the prior subsequent received C/I code, has been received at least twice. The actual C/I code can be read from the CIRR register.
SIN	Synchronous Transfer Register The beginning or the center of an IOM-frame has been indicated, as programmed in the STCR register.
EXI	Extended Interrupt This interrupt signifies that one of eight non-critical interrupts, indicated in the extended interrupt register EXIR, has been generated. The exact cause must be read from EXIR.

Note: Reading of the EXIR register by the processor clears the EXI-bit, and reading of the ISTA register clears all other bits of ISTA.

MASK—Mask Register—(Write)

Value after Reset: 00H (all interrupts enabled)
Address: 20H

Format:



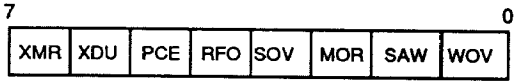
Bit Name	Description
RME	Each bit of the MASK register relates to the corresponding bits of the ISTA register. Each interrupt can be selectively masked by setting the respective bit in MASK.
EXI	Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective MASK is reset.

Note: In the event of an extended interrupt, no interrupt request (INT = Low) will be generated with a masked EXI-bit, although this bit is set in ISTA.

EXIR—Extended Interrupt Register—(Read)

Value after Reset: 00H
Address: 24H

Format:



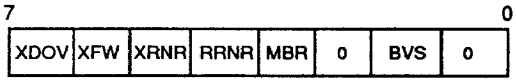
Bit Name	Description
XMR	Transmit Message Repeat The transmission of the last message has to be repeated because: the ISAC-S has received a negative acknowledgment in auto mode (according to HDLC/LAPD) a collision on the S-bus has been detected after the 32nd data byte
XDU	Transmit Data Underrun The actual transmission of a frame has been aborted with "IDLE" because the XFIFO holds no further data. This interrupt occurs whenever the processor has failed to respond to an XPR interrupt (ISTA register) quickly enough, after having initiated a frame transmission, and the message to be transmitted is not yet complete.
PCE	Protocol Error (significant during auto mode only) A protocol error has been detected during auto mode due to a received S- or I-frame with an incorrect sequence number N(R), or to an S-frame containing an I-field.
RFO	Receive Frame Overflow The received data of a message could not be stored entirely, because the internal message buffer is occupied (the whole message has been lost). This interrupt can be used for statistical purposes and indicates that the processor does not respond quickly enough to an incoming RPF or RME interrupt (ISTA).
SOV	Synchronous Transfer Overflow The synchronous transfer programmed in STCR (ST0/ST1) was not confirmed in time (setting SC0/SC1 by the processor).
MOR	Monitor Byte Received (not used in the ISAC-S) A valid monitor byte has been identified in an IOM frame and has been stored in the MONR register.
SAW	Subscriber Awake Indicates that a falling edge on the SAW line has been detected, in case the terminal-specific functions are adjusted (TFS-bit in STCR).
WOV	Watchdog Timer Overflow Signals the expiration of the watchdog timer, which means that the processor has failed to set the watchdog timer control bits WTC1 and WTC2 in the correct manner. A reset pulse has been generated by the ISAC-S.

Note: When an XMR or XDU interrupt is generated, it is not possible to send transparent frames or I-frames until the interrupt has been acknowledged by the processor.

STAR—Status Register—(Read)

Value after Reset: 48H
Address: 21H

Format:

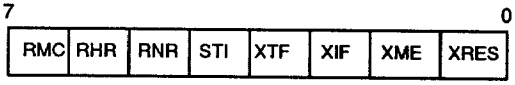


Bit Name	Description
XDOV	Transmit Data Overflow More than 32 bytes have been written to one pool of the XFIFO, and data have been overwritten in this pool.
XFW	Transmit FIFO Write Enable Data can be written to the XFIFO. The polling of the XFW-bit can be used instead of or in addition to an XPR interrupt handling when few messages have to be transmitted (refer to D-channel capacity).
XRNR	Transmit RNR (significant during auto mode only) During auto mode, this bit indicates whether the ISAC-S receiver status is ready or not ready (if not ready, the ISAC-S sends an "RNR" S-frame autonomously to the remote station.) 0 —> receiver ready 1 —> receiver not ready
RRNR	Received RNR (significant in auto mode only) During auto mode, this bit indicates the receiver status of the remote station 0 —> (remote) receiver ready 1 —> (remote) receiver not ready (If not ready, the ISAC-S has received an "RNR" S-frame from the remote station.)
MBR	Message Buffer Ready This bit signifies that temporary storage is available in the RFIFO to receive at least the first 16 bytes of a new message.
BVS	B-channel Valid at SLD port BVS indicates the beginning of an SLD frame, especially the validity of the two B-channels, and represents a 16-kHz signal, synchronous to the SLD frame.

CMDR—Command Register—(Write)

Value after Reset: 00H
Address: 21H

Format:



Bit Name	Description
RMC	Receive Message Complete Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the processor confirms to the ISAC-S, that it has fetched the current frame or data block, and the ISAC-S can release the space occupied in the RFIFO.
RHR	Reset HDLC Receiver All data in the RFIFO and the contents of the message buffer is deleted. In auto mode, the Transmit and Receive counters (V)[S], V[R] according to HDLC), also are reset.
RNR	Receiver Not Ready (used in auto mode only) The status of the ISAC-S receiver is set. Determines, whether a received frame is acknowledged via an "RR" or "RNR" supervisory frame (S-frame according to HDLC) in auto mode. 0 —> receiver ready ("RR") 1 —> receiver not ready ("RNR")
STI	Start Timer The internal timer is started in external timer mode (TMD-bit in MODE register). The timer is stopped by rewriting the TIMR register after start.
XTF	Transmit Transparent Frame After having written up to 32 bytes in the XFIFO, this command bit initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the ISAC-S.
XIF	Transmit I-Frame (used in auto mode only) Initiates the transmission of an I-frame in auto mode. In addition to the opening flag sequence, the address and control field of the frame is automatically added by the ISAC-S.
XME	Transmit Message End Indicates that the data block written last to the XFIFO completes the current frame. The ISAC-S terminates the transmission operation properly by appending the CRC and the closing flag sequence to the data.
XRES	Transmit Reset The contents of the XFIFO is deleted and an "IDLE" is transmitted. This command can be used by the processor to abort a frame currently in transmission.

Note: After an XPR interrupt, further data have to be written in the XFIFO and the appropriate Transmit Command (XTF or XIF) has to be written in the CMDR register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTA).

During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.

MODE—Mode Register—(Read/Write)

Value after Reset: 00H
Address: 22H

Format:

7							0
MDS1	MDS0	ADM	TMD	RAC	HMD2	HMD1	HMD0

Bit Name **Description**

MDS1, MDS0 Mode Select
The message transfer mode of the HDLC controller is selected.

MDS1	MDS0	Mode
0	0	auto
0	1	non-auto
1	0	transparent
1	1	extended transparent

ADM Address Mode
Defines the length of the address field in an HDLC frame.
0 —> 1-byte address field, LAPB
1 —> 2-byte address field, LAPD
If the extended transparent mode is selected by setting MDS1 = MDS0 = 1, this bit differentiates between the two modes:
0 —> extended transparent mode 0 (no address recognition)
1 —> extended transparent mode 1 (SAPI address recognition)

TMD Timer Mode
The operating mode of the internal timer is set.
0 —> external mode
The Timer is controlled by the processor and can be started at any time by setting the STI-bit in CMDR and can be stopped by rewriting the TIMR register (see also TIMR register).
1 —> internal mode
The timer is used internally by the ISAC-S for time-out and retry conditions in auto mode (refer to TIMR register description).

RAC Receiver Active
Switches the receiver to operational or inoperational state.
0 —> receiver inactive
1 —> receiver active

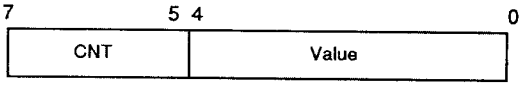
HMD2, HMD1, HMD0 HDLC Port Mode
The operating mode of the IOM/(HDLC) interface is set.

HMD2	HMD1	HMD0	Mode	Interface Monitor Channel
0	0	0	IOM	Monitor channel is not used. In point-to-point or for primary use (LT-S/NT mode) in point-multipoint configurations (S-bus).
0	0	1		Monitor channel is used. For secondary use (TE mode) in point-multipoint configurations (D-channel access control).
0	1	0	/	Reserved
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1	HDLC	For diagnostic or test configurations, it is possible to program a pure HDLC frame without the complex 2-D-bit splitting of the IOM frame. The data clock and the component clock are identical.

TIMR—Timer Register—(Read/Write)

Value after Reset: Undefined (Previous Value)
Address: 23H

Format:



Field Name	Description

CNT is a 3-bit field; value is a 5-bit field.

Value — Sets the time period T1 as follows:
T1 = (Value + 1) • 64 µs

CNT — Interpreted differently, depending on the selected timer mode (TMD-bit in the MODE register).
Internal timer mode (TMD = 1)

CNT indicates the maximum number of S-commands "N1" which are transmitted autonomously by the ISAC-S after expiration of time period T1 (retry, according to HDLC). The internal timer procedure will be started in auto mode:

after start of I-frame transmission; or,
after an "RNR" S-frame has been received

After the last retry, a timer interrupt (TIN-bit in ISTA) is generated.
The maximum time between the start of I-frame transmission or reception of an "RNR" S-frame and the generation of a TIN interrupt would be: (CNT + 1 • T1.

The timer procedure will be stopped when:

a TIN interrupt is generated; or,
the TIMR is written to; or,
a positive or negative acknowledgment has been received.

Note: The maximum value of CNT can be 6. If CNT is set to 7, the number of retries is unlimited.
External timer mode (TMD = 0)
CNT together with Value determine the time period T2 after which a TIN interrupt will be generated:
T2 = CNT • 2.048 sec + T1
The timer can be started by setting the STI-bit in CMDR and will be stopped when :

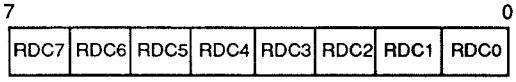
a TIN interrupt is generated; or,
the TIMR register is written to

If CNT is set to 7, a TIN interrupt is periodically generated after every expiration of T1.

RFBC—Receive Frame Byte Counter—(Read)

Value after Reset: 00H
Address: 25H

Format:



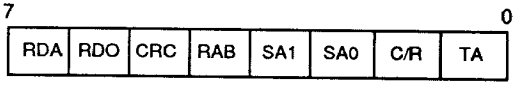
Bit Name	Description
RDC7–0	Receive Data Count Represents the total number of actual received data bytes of a message (limited to 223).
RCRDC4–0	Indicates always the length of the data block currently available in the 32-byte RFIFO. For message lengths greater than 223 data bytes, the bits RDC7–5 remain to the value "111." In this case only the bits RDC4–0 are significant.

Note: Normally this register should be read by the processor after an RME interrupt in order to determine the number of bytes to be read from the RFIFO, and the total message length.

RSTA—Receive Status Register—(Read)

Value after Reset: Undefined
Address: 27H

Format:



Bit Name	Description
RDA	Data Received Data is available in the RFIFO. (RDA = "1"). After an RME interrupt, an RDA = "0" means that data is available in the internal registers RHCR or TEI1 only (that is, S-frame).
RDO	Receive Data Overflow A data overflow has occurred with the current frame. At least one byte of the frame has been lost (that is, the last message has to be deleted).
CRC	CRC compare/check 0 —> CRC check failed (received frame contains errors) 1 —> CRC check passed (received frame contains no errors) Receive Message Aborted The received message was aborted from the remote station. According to HDLC, this frame must be discarded by the processor.
SA1, SA0	SAPI Address Identification Indicates which of the three possible SAPI addresses were recognized. SA1 SA0 — 0 0 SAPI2 (programmable); 0 1 Group SAPI (fixed value, ISDN/LAPD management functions); 1 0 SAPI1 (programmable)
C/R	Command/Response The C/R bit identifies a frame as either a command or a response, according to LAPD. Command — 0 — user to network side; Response — 1 Command — 1 — network to user side; Response — 0
TA	TEI Address Identification The comparison of the TEI address in the received frame with the two programmable addresses TEI1 and TEI2 resulted in: 1 —> TEI1 was recognized 0 —> TEI2 was recognized

Note: In transparent and extended transparent mode with ADM-bit set to 1 in the MODE register:
SAPI address recognition—the TA-bit is irrelevant.
In extended transparent mode with ADM-bit set to 0
No address recognition—bits 0–3 are irrelevant.

If the programmable address registers SAP1 and SAP2 contain the same address value, the bit combination "00" will be omitted.

LAPD/(HDLC) Address Variables

XAD1—Transmit Address 1—(Write)

Address: 24H

Format:

Bit Name	Description
Bit 0–7	Used in auto mode only XAD1 contains an individual programmable address byte which is appended automatically to the frame by the ISAC-S in auto mode. Depending on the selected address mode (ADM-bit in MODE,) XAD1 is interpreted as follows: 2-byte address field (AMD = 0) XAD1 builds up the high byte (SAPI in the ISDN) of the 2-byte address field. According to the ISDN LAPD protocol, bit 1 is interpreted as the command/response bit "C/R" and will be automatically inserted by the ISAC-S depending on the CRI bit in the SAP1 register. Bit 1 must be set to 0. In the ISDN LAPD, the address field extension bit "EA," that is, bit 0 of XAD1 must be set to 0.

C/R Bit			
Command	Response	Transmission Side	CRI Bit
0	1	Network	0
1	0	User	1

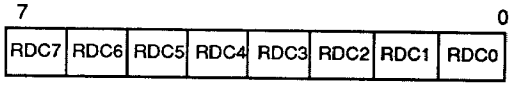
1-byte address field (ADM = 1)
According to the X.25 LAPB protocol, XAD1 indicates a command.

Note: In standard ISDN/LAPD applications, only 2-byte address fields are used.

XAD2—Transmit Address 2—(Write)

Address: 25H

Format:



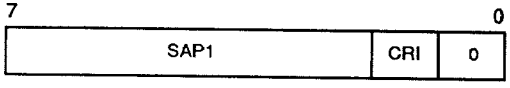
Bit Name	Description
Bit 0–7	Used in auto mode only XAD2 represents the second individual programmable address byte, whose function depends on the selected address mode (ADM-bit in MODE) 2-byte address (ADM = 0) XAD2 builds up the low byte (TEI in the ISDN) of the 2-byte address field. 1-byte address (ADM = 1) According to the X.25 LAPB protocol, XAD2 indicates a response.

Note: See note to XAD1 register description.

SAP1—SAPI Register 1—(Write)

Address: 26H

Format:



Bit Name	Description
SAPI1 Bit 7–2	SAPI 1 value Value of the first individual programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.
CRI	Command/Response Interpretation CRI defines the side of the ISDN user-network interface for identification of command/response frames. Depending on CR,I the C/R-bit will be interpreted autonomously by the ISAC-S, when receiving frames in auto mode, as follows:

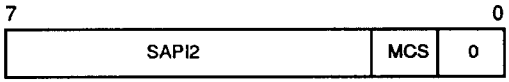
CRI Bit	Receiver End	C/R Bit	
		Command	Response
0	Network	1	0
1	User	0	1

For transmitting frames in auto mode, the C/R-bit manipulation will also be done automatically, depending on the setting of the CRI-bit (refer to XAD1 register description). In message transfer modes with SAPI address recognition (all except extended transparent mode 0) the high byte of the received address is compared with the individual programmable values in SAP1, SAP2, and the fixed group SAPI. (In 1-byte address mode, the CRI-bit would have to be set to 0.)

SAP2—SAPI Register 2—(Write)

Address: 27H

Format:



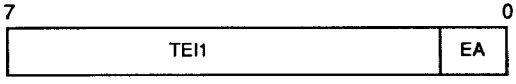
Bit Name	Description
SAPI2 Bit 7–2	SAPI 2 value Value of the second individual programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.
MCS	Module Count Select (valid in auto mode only) The MCS bit adjusts the control field format according to the ISDN LAPD protocol. 0 —> basic operation (modulo 8) 1 —> extended operation (modulo 128)

Note: When modulo 128 is selected in auto mode, the RHCR register contains compressed information of the extended control field (see RHCR register description).

TEI1—TEI Register 1—(Read/Write)

Address: 28H

Format:



Bit Name	Description
TEI(1) Bit 7–1	TEI value 1
EA	Address field Extension bit Has to be set to "1" according to ISDN LAPD. Write: Value of the first individual programmable Terminal Endpoint Identifier (TEI) according to the ISDN LAPD protocol (2-byte address field). In auto and non-auto mode this value is used by the ISAC-S for the address recognition. Read: Depending on the message transfer mode, the reading of the TEI1 register contains the following information:

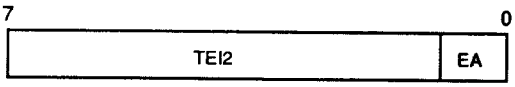
Message Transfer Mode	Meaning/Contents
Auto	Inverted value of the programmed TEI1
Non-auto	Inverted value of the programmed TEI1
Transparent	Received TEI value
Extended Transparent 0	First byte of the frame after the opening flag
Extended Transparent 1	Received TEI value

Note: In auto and non-auto mode with 1-byte address field, the whole contents of TEI1 would be recognized as a command according to X.25 LAPB.

TEI2—TEI Register 2—(Write)

Address: 29H

Format:



Bit Name	Description
TEI(2) Bit 7–2	TEI value 2 Value of the second individual programmable Terminal Endpoint Identifier (TEI) according to the ISDN LAPD protocol (2-byte address field). In auto and non-auto mode, this value is used by the ISAC-S for the address recognition.
EA	Address field Extension bit Has to be set to "1" according to ISDN LAPD.

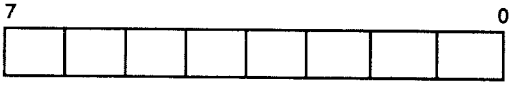
Note: In auto and non-auto mode with 1-byte address field, the whole contents of TEI2 would be interpreted as a response according to X.25 LAPB.

LAPD/(HDLC) Control Data

RHCR—Receive HDLC Control Register—(Read)

Address: 29H

Format:



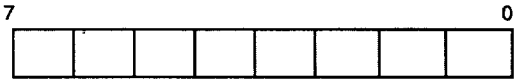
Bit Name	Description
Bit 0–7	Value of the received HDLC control field In extended transparent mode 0 (no address recognition), RHCR contains the second byte of a received frame after the opening flag. When modulo 128 is selected in auto mode, the RHCR register contains compressed information of the extended control field. In this case the bit 0 of the RHCR register has the following meaning: 0 —> an I-frame has been received 1 —> a U-frame has been received (S-frames will be handled autonomously by the ISAC-S.) When message transfer modes other than the auto mode are used and "modulo 128" is agreed upon, then the first octet of the extended control field is available in the RHCR register. The second octet is always available in the RFIFO corresponding to the message transfer mode.

LAPD/(HDLC) Information Data

RFIFO—Receive FIFO—(Read)

Address: 00–1FH

Format:

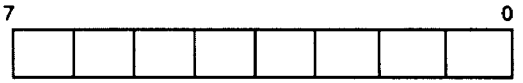


Bit Name	Description
Bit 0–7	Up to 32 bytes of received data can be read from the RFIFO. After an RPF interrupt (ISTA), exactly 32 bytes are available. After an RME interrupt (ISTA), the number of data bytes to be read may be obtained reading the RFBC register.

XFIFO—Transmit FIFO—(Write)

Address: 00–1FH

Format:



Bit Name	Description
Bit 0–7	Up to 32 bytes of transmit data can be written into the XFIFO following an XPR interrupt (ISTA).

Note: Addresses within the address space of the FIFOs (00–1FH) are interpreted equally, that is, the current data byte can be accessed with any address within the valid space.

SPCR—Serial Port Control Register—(Read/Write)

Address: 30H

Format:

7							0
SPU	SAC	SPM	TLP	B1C1	B1C0	B2C1	B2C0

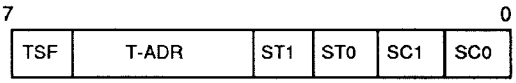
Bit Name	Description
SPU	Software Power Up (in TE mode only) For activating the ISDN S interface in TE mode, the SPU-bit has to be set to '1' and then cleared again. After a subsequent CIC interrupt (C/I code change; ISTA) and reception (the C/I code "PU" Power Up indication in TE mode), the reaction of the processor would be: to write an Activate Request command as C/I code in the CIXR register to reset the SPU-bit and wait for the following CIC interrupt.
SAC	SIP Activated With SAC, the state of the SLD port can be programmed as follows: 0 —> inactive in transmit direction (SIP: always high impedance) 1 —> active in transmit direction
SPM	Serial Port Timing Mode SPM selects the timing mode: 0—> timing mode 0 — terminal: Timing signals are derived from the S-bus. DCL, FSC1 and FSC2 are outputs. FSD/SCA is a 128-kHz clock signal for SSI. 1 —> timing mode 1 — exchange: Timing signals are provided by the digital exchange system. DCL, FSC1 and FSC2 are inputs. FSD/SCA is the delayed frame signal of FSC1.
TPL	Test Loop Instructs the ISAC-S to connect internally the IOM interface lines SDI and SDO. Also, the times T1 and T2 programmed in the TIMR register—are reduced by a factor of 64.
B1C1, B1C0	Switching of B1 channel — Both B-channels can be switched independently of each other.
B2C1, B2C0	Switching of B2 channel

BC1	BC0	B-Channel Switching	µP Access
0	0	SLD loop	monitoring, loop
0	1	SLD-IOM (S-bus) connection	monitoring
1	0	SSI-IOM (S-bus) connection	monitoring
1	1	IOM loop	monitoring, loop

STCR—Synchron Transfer Control Register—(Write)

Address: 37H

Format:



Bit Name	Description
TSF	Terminal Specific Functions 0 —> The serial interface port for the SLD interface is selected (SIP). 1 —> The terminal-specific, such as Subscriber/Exchange Awake (SIP/SAW)functions, are activated, Watchdog Timer In this case, the SIP/SAW line is always an input signal which can serve as a request signal from the subscriber to initiate the awake function in a terminal. A falling edge on the SAW line generates an SAW interrupt (EXIR). When the RSS-bit in the CIXR register is zero, a falling edge on the SAW line (Subscriber Awake) or a C/I code change (Exchange Awake) initiates a reset pulse. When the RSS-bit is set to one on the other hand, a reset pulse is triggered only by the expiration of the watchdog timer (see also CIXR register).
T-ADR	TIC bus Address T-ADR defines an individual address for the point-to-multipoint bus configuration of the IO -interface (TIC bus: Telecom IC bus). The bus configuration makes it possible to connect further ICCs (up to seven) to the Layer 1 component of the ISAC-S.
ST1	Synchronous Transfer 1 When set, causes the ISAC-S to generate an SIN interrupt (ISTA register) at the beginning of the 8-kHz frame signal. timing mode 0 FSC1 and FSC2 (IOM, SLD, SSI) timing mode 1 FSC1 (System)
ST0	Synchronous Transfer 0 When set, causes the ISAC-S to generate an SIN interrupt at the center of the 8-kHz frame signal. timing mode 0 FSC1 and FSC2 (IOM, SLD, SSI) timing mode 1 FSC1 (System)
SC1	Synchronous Transfer 1 Completed After an SIN interrupt, the processor has to access and subsequently acknowledge the interrupt by setting the SC1-bit before the center of the frame signal is reached, if the interrupt originated from a Synchronous Transfer 1 (ST1). Otherwise, an SOV interrupt (EXIR register) will be generated.
SC0	Synchronous Transfer 0 Completed After an SIN interrupt, the processor has to access and subsequently acknowledge the interrupt by setting the SC0-bit before the end of the frame signal is reached, if the interrupt originated from a Synchronous Transfer 0 (ST0). Otherwise, an SOV interrupt (EXIR register) will be generated.

Notes: ST0/1 and SC0/1 are useful for synchronizing microprocessor accesses and receive/transmit operations in the ISAC-S.

In a TIC bus configuration, that is, if additional Layer-2 controllers (ICCs) are connected to the IOM interface, it has to be ensured that one Layer-2 component has been assigned the TIC bus address "7." For applications without additional Layer-2 components it is generally recommended to set ADR to "7" (after reset T-ADR = "0").

The TSF-bit will be cleared only by Hardware reset.

CIXR—Control/Indicate Transmit Register—(Write)

Value after Reset: BFH
Address: 31H

Format:

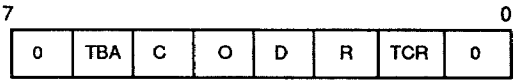
7							0
RSS	TBC	C	O	D	X	TCX	ECX

Bit Name	Description
RSS	Reset Source Select 0 —> Subscriber or Exchange Awake (Power Down) As reset source serves: a falling edge on the SAW line (Subscriber Awake) a C/I code change (Exchange Awake) A logical zero on the SAW line also activates the IOM interface clock and frame signal, just as the SPU-bit (SPCR) does. 1 —> Watchdog Timer (Power Up) The expiration of the watchdog timer generates a reset pulse. The watchdog timer will be reset and restarted when two special bit combinations are written in the ADFR register within the time period of 128 ms (see also ADFR register description). After a reset pulse generated by the ISAC-S and the appropriate interrupt (WOV, SAW or CIC), the actual reset source can be read from the ISTA and EXIR.
TBC	TIC bus Control For transmitting the C/I code written in the CIXR register, an access to the TIC bus can be forced by setting the TBC-bit. When no further Layer 2 controllers are connected to the TIC bus (IOM interface) and the TIC bus address is programmed to "7" (T-ADR in the STCR register,) the TIC bus is always accessed and it is not necessary to set the TBC-bit.
CODX	C/I-Code Transmit These four bits are transmitted continuously (beginning with the left-most one) as a Command/Indicate code in the C/I channel of the IOM frame, if the TIC bus is accessed.
TCX	T-Channel Transmit The TCX-bit will be transmitted continuously in the T-channel of the IOM frame if the TIC bus is accessed.
ECX	E-Channel Transmit The ECX-bit will be transmitted continuously in the E-channel of the IOM frame if the TIC bus is accessed.

CIRR—Control/Indicate Receive Register—(Read)

Value after Reset: 7EH
Address: 31H

Format:



Bit Name	Description
TBA	TIC Bus Access Indicates the state of the TIC bus (transmit direction: Layer 2 to Layer 1; SDI) when a C/I code change has been recognized. TBA = 0 means the TIC bus is occupied by the ISAC-S.
CODR	C/I Code Receive The receipt of a new C/I code in two successive IOM frames, which differs from the previously received value, will release a CIC interrupt (ISTA register). After detection of such a C/I code change the new code can be read from CIRR.
TCR	T-Channel Receive TCR represents the current value received in the T-channel.

Note: The TBA- and CODR-bits of the CIRR will be updated every time CIRR has been read previously by the processor and a C/I code change is recognized. If several C/I code changes were recognized before reading the CIRR register, only the very first and very last changes in the C/I code (also TBA) will be available for the processor to read.

MONR— Monitor Register—(Read/Write)

Address: 32H

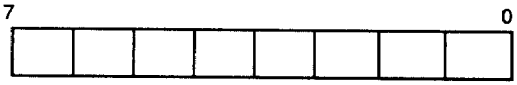
Format:

Bit Name	Description
Bit 0–7	The MONR register normally contains control information transferred in the monitor channel of an IOM frame between Layer 2 and Layer 1. In the ISAC-S however, MONR is not required since the monitor channel is used only for the TIC bus access mechanism, which will be automatically realized by the ISAC-S.

BCX1—B1-channel Transmit Register—(Read/Write)

Address: 35H

Format:



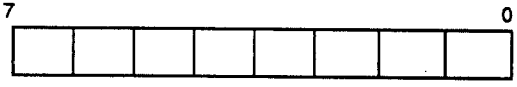
Bit Name	Description
Bit 0–7	BCX1 can be used in microprocessor-controlled interactions with the serial transmission process, for instance in loop or monitor applications. Depending on the selected B-channel switching (SPCR register) and synchronized to the transmission process via SIN interrupt (ISTA register) and BVS-bit (STAR register), the serial data can be read/written from/to BCX1 as follows:

B-channel Switching	Receive Data from (Read)	Transmit Data to (Write)
SLD loop	SLD	SLD
SLD-IOM connection	SLD	/
SSI-IOM connection	SSI	/
IOM loop	IOM	IOM

BCX2—B2-channel Transmit Register —(Read/Write)

Address: 36H

Format:



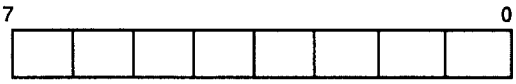
Bit Name	Description
Bit 0–7	BCX2 can be used in microcprocessor-controlled interactions with the serial transmission process, for instance in loop or monitor applications. Depending on the selected B-channel switching (SPCR register) and synchronized to the transmission process via SIN interrupt (ISTA register) and BVS-bit (STAR register), the serial data can be read/written from/to BCX2 as follows:

B-channel Switching	Receive Data from (Read)	Transmit Data to (Write)
SLD loop	SLD	SLD
SLD-IOM connection	SLD	/
SSI-IOM connection	SSI	/
IOM loop	IOM	IOM

BCR1—B1-channel Receive Register—(Read)

Address: 37H

Format:

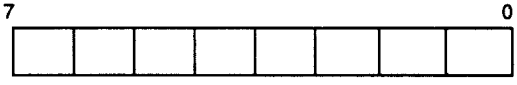


Bit Name	Description
Bit 0–7	BCR1 can be used in microprocessor-controlled monitoring of the serial transmission process by reading data from BCR1 as listed below: B-channel Switching — Receive Data from (Read) SLD-IOM connection — IOM SSI-IOM connection — IOM

BCR2—B2-channel Receive Register—(Read)

Address: 38H

Format:

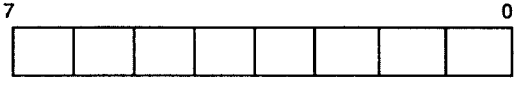


Bit Name	Description
Bit 0–7	BCR2 can be used in microprocessor-controlled monitoring of the serial transmission process by reading data from BCR2 as listed below: B-channel Switching — Receive Data from (Read) SLD-IOM connection — IOM SSI-IOM connection — IOM

SSGX—SLD Signaling Register Transmit—(Write)

Address: 33H

Format:

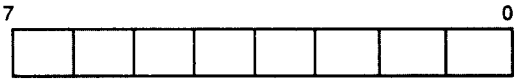


Bit Name	Description
Bit 0–7	The contents of SSGX represent directly the signaling byte (SIG) which will be transmitted continuously in an SLD frame.

SSGR—SLD Signaling Register Receive—(Read)

Address: 33H

Format:

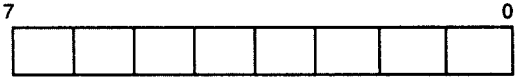


Bit Name	Description
Bit 0–7	The signaling byte of a received SLD-frame can be read from SSGR.

SFCR—SLD Feature Control Register—(Read/Write)

Address: 34H

Format:



Bit Name	Description
Bit 0–7	The Feature Control (FC) byte of an SLD frame (receive) can be read from SFCR. Also, an FC byte to be transmitted in an SLD frame (transmit) has to be written into SFCR. The microprocessor accesses are synchronized to SIN interrupts (ISTA, refer to STCR).

ADFR—Additional Feature Register—(Write)

Value after reset: 00H
Address: 38H

Format:

7							0
WTC1	WTC2	TEM	PFS	CFS	FC2	FC1	ITF

Bit Name	Description

WTC1, WTC2 — Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected, the watchdog timer is started. During every time period of 128 ms the processor has to program the WTC1- and WTC2-bit in the following consecutive sequence:

	WTC1	WTC2
1.	1	0
2.	0	1

to reset and restart the watchdog timer. If not, the timer expires and a WOV interrupt together with a reset pulse, are initiated.

TEM — Test Mode

Setting this bit makes it possible to test the Layer 2 functions of the ISAC-S using the IOM interface. The Layer 1 functions are disabled, and the ISAC-S is fully compatible to the "ICC" at the IOM interface with the following references to the "ICC" pin designation:

ICC (IOM) =	ISAC-S	Meaning
FSC	FSC1	frame synchronization
DC	DCL	interface clock
SDBR	SDO	receive data
SDBX	SDI	transmit data

PFS — Prefilter Select

This bit has to be set, if an external prefilter is connected to S-bus port receive, respectively pins SR1, SR2, and UFI. PFS initiates an internal delay time compensation.

CFS — Configuration Select

Depending on the operating mode, CFS determines clock relations and recovery on S and IOM interfaces.
TE mode:

0 —> The IOM interface clock and frame signal is always active (standby). With the C/I command Timing (TIM), the processor can initialize the "Power Up" state. With C/I command Deactivation Indication (DIU) the "Stand By" state will be reached again. It should be mentioned, however, that it is also possible to activate the S interface directly with the C/I command Activate Request (AR 8/10/L) without the TIM command.

1 —> The IOM interface clock and frame signal is normally inactive ("Power Down"). For activating the S inter face, the "Power Up" state can be initialized via software (SPU-bit in SPCR register). After that, the S interface can be activated with a C/I command Activate Request (AR8/10/L). The "Power Down" state will be reached again with the C/I command Deactivation Indication (DIU).

Note: After reset the IOM interface is always active. To achieve "Power Down" state properly the CFS- bit has to be set previously.

LT-S mode:

0 —> Bit stream on S-interface with the internal PLL. This is to tolerate a variable bit shift from 2 to 8 bit-times (greater distances possible: max. ≤ 1.0 – 1.5 km).

1 —> In bus configurations only a fixed bit shift of 2 bit-times will be accepted according to CCITT (max. round trip delay time; max. ≤ 150 m).

LT-T mode:

0 —> CFS always has to be set to "0."

ADFR (continued)

Bit Name	Description
FC2, FC1	Frame Synchronization Control 2,1 (significant in TE mode only) Adjusts the polarity of the symmetrical 8-kHz-frame output signal (IOM, SLD, SSI). 0 —> normal: High during the first half of the 125-µs frame, Low during the second half. 1 —> inverted: Low during the first half, High during the second half of the 125-µs frame. Note: If the FSC1, FSC2 outputs (in TE mode) supply the data strobe signal for B-channel sources/destinations connected to the Serial Synchron Interface (SSI), it is possible to select individual switching to the B1- or B2-channel.
ITF	Interframe Time Fill ITF selects the interframe time-fill signal which will be sent between HDLC frames when the HDLC port mode is selected in MODE. 0 —> idle (sequence of "1"s) 1 —> flags (sequence of patterns: "0111 1110") When the IOM interface mode is selected, the interframe time fill signal is always idle, according to LAPD.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... –65 to +125°C
Ambient temperature under bias ..... 0 to +70°C
Voltage on any pin with respect to ground ..... –0.4 to V_{DD} + 0.4 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

T_A = 0 to 70°C, V_{DD} = 5 V ±5%, V_{SSD} = 0 V, V_{SSA} = 0 V

Parameter Symbol	Parameter Descriptions	Test Conditions	Limit Values Min.	Max.	Unit
All pins except SX1, SX2, SR1, SR2, RREF					
V_{IL}	Input Low voltage	—	–0.4	0.8	V
V_{IH}	Input High voltage	—	2.0	V_{CC} + 0.4	V
V_{OL}	Output Low voltage	I_{OL} = 2 mA	—	0.45	V
V_{OH}	Output High voltage	I_{OH} = –400 µA	2.4	—	V
V_{OH}	Output High voltage	I_{OH} = –100 µA	—	V_{CC} –.5	V
I_{CC}	Power supply current operational	V_{DD} = 5V, Inputs at 0 V/V_{DD}	—	13	mA
	Power supply current power down	No output loads	—	1.3	mA
I_{LI}	Input leakage current	0 V < V_{IN} < V_{DD} to 0 V	—	+10	µA
I_{LO}	Output leakage current	0 V < V_{OUT} < V_{DD} to 0 V	—	+10	µA
SX1, SX2					
VX	Absolute value of output	R_L = 25 ohms**	—	0.3	V
	Pulse amplitude	R_L = 200 ohms	1.35	1.65	V
	(VSX2–VSX1)*	R_L = 1600 ohms	1.35	2.4	V
IX	Transmitter output current	R_L = 200 ohms	—	8.25	mA
RX	Transmitter output	Inactive or during binary one	10	—	kohm
	Impedance	During binary zero	80	—	ohm
		R_L = 200 ohms			
SR1, SR2					
VSR1	Receiver output voltage	I_o < 100 µA	2.4	2.6	V
VTR	Receiver threshold voltage VSR2–VSR1	Dependent on peak level	+225	+375	mV
RREF					
VO	Voltage at RREF	R_{REF} = 2.2 kohm ±1%	1.0	1.2	V
IO	Output Current	R_{REF} = 2.2 kohm ±1%	450	550	µA

Notes: *Due to the transformer, the pulse amplitude zero to peak on S interface line will be halved.
**Load resistance on S interface line will be divided by four.

CAPACITANCES

T_A = 25°C, V_{DD} = 5 V ±5%, V_{SSD} = 0 V, V_{SSA} = 0 V

Parameter Symbol	Parameter Descriptions	Test Conditions	Limit Values Min.	Max.	Unit
All pins except SR1,SR2, XTAL1, XTAL2					
C_{IN}	Input capacitance	—	—	7	pF
C_{IO}	I/O	—	—	7	pF
SX1, SX2					
C_{OUT}	Output capacitance against V_{SSA}	—	—	10	pF
SR1, SR2					
C_{IN}	Input capacitance	—	—	7	pF
XTAL1, XTAL2					
C_{LD}	Load capacitance	—	—	50	pF

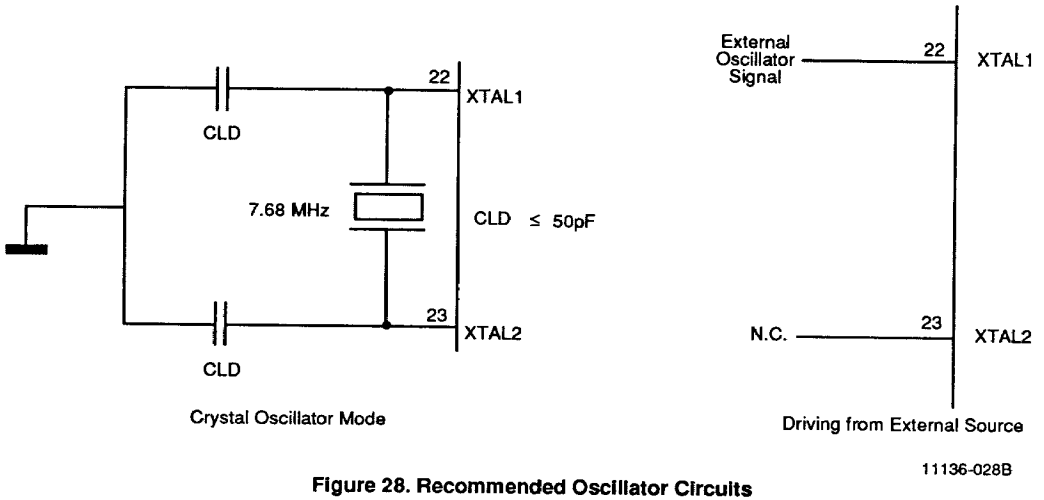


Figure 28. Recommended Oscillator Circuits

SWITCHING CHARACTERISTICS

T_A = 0 to 70°C, V_{DD} = 5 V ±5%, V_{SSD} = 0 V, V_{SSA} = 0 V

Inputs are driven at 2.4 V for a logic "1" and at 0.4 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0." The AC testing input/output waveforms are shown below.

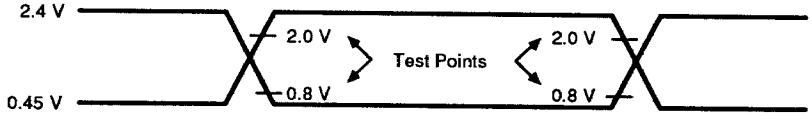
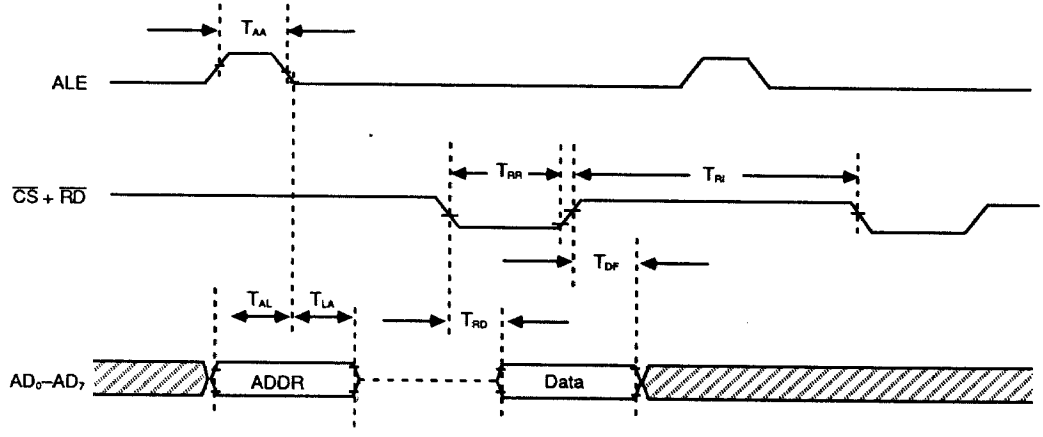


Figure 29. Input/Output Waveform AC Tests

Table 11. Microprocessor Interface Timing

Parameter Symbol	Parameter Description	Test Conditions	Limit Values Min.	Max.	Unit
T_{AA}	ALE pulse width	—	50	—	ns
T_{AL}	Address setup time at ALE	—	20	—	ns
T_{LA}	Address hold time from ALE	—	10	—	ns
T_{RR}	$\overline{RD}$ pulse width	—	110	—	ns
T_{RD}	Data output delay from $\overline{RD}$	—	—	25	ns
T_{DF}	Data float delay from $\overline{RD}$	—	—	110	ns
T_{RI}	$\overline{RD}$ control interval	—	70	—	ns
T_{WW}	$\overline{WR}$ pulse width	—	60	—	ns
T_{DW}	Data setup time to $\overline{WR} + \overline{CS}$	—	35	—	ns
T_{WD}	Data hold time from $\overline{WR} + \overline{CS}$	—	10	—	ns
T_{WI}	$\overline{WR}$ control interval	—	70	—	ns



11136-030B

Figure 30. Microprocessor Read Cycle

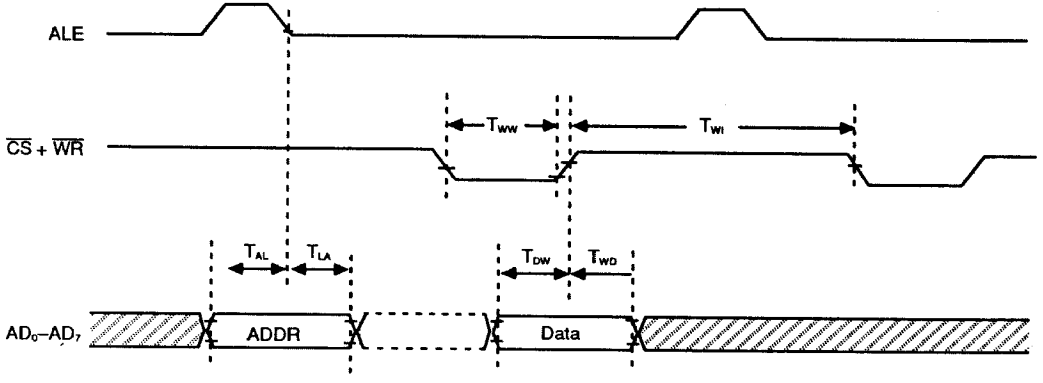


Figure 31. Microprocessor Write Cycle

11136-031B

Table 12. SLD Interface Timing

Parameter Symbol	Parameter Description	Test Conditions	Limit Values Min.	Max.	Unit
T_{SLD}	SLD data delay	—	20	100	ns
T_{SLS}	SLD data setup	—	30	—	ns
T_{SLH}	SLD data hold	—	30	—	ns
T_{FSH}	Frame sync. hold	—	30	—	ns
T_{FSS}	Frame sync. setup	—	50	—	ns
T_{FSW}	Frame sync. width	—	40	—	ns
T_{FSD}	Frame sync. delay	—	–20	20	ns

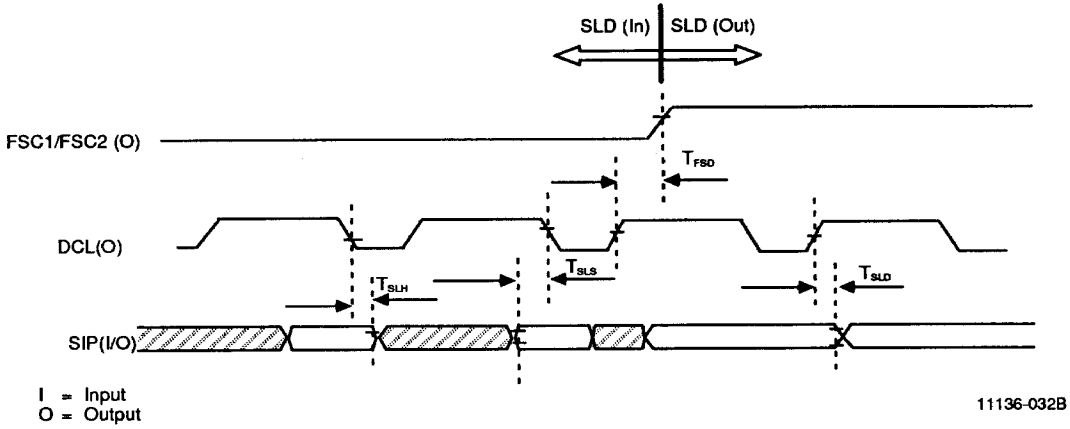


Figure 32. SLD (TE Mode)

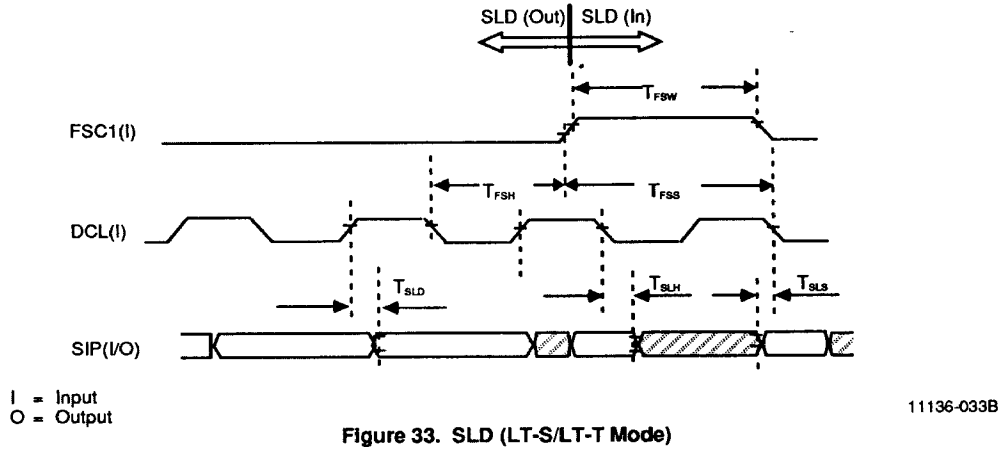
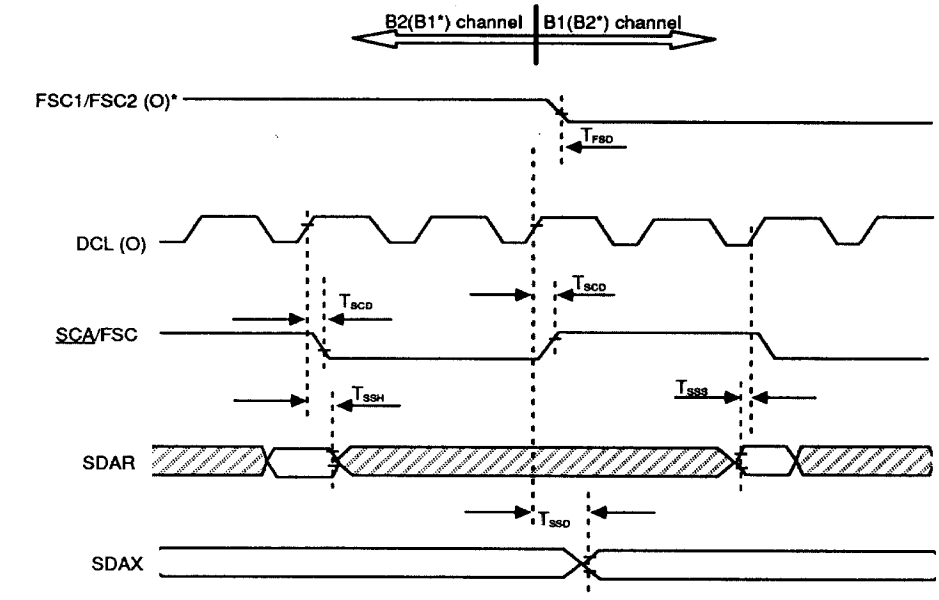


Figure 33. SLD (LT-S/LT-T Mode)

Table 13. SSI Timing

Parameter Symbol	Parameter Description	Test Conditions	Limit Value Min.	Max.	Unit
T_{SCD}	SCA clock delay	—	20	100	ns
T_{SSD}	SSI data delay	—	20	100	ns
T_{SSS}	SSI data setup	—	30	—	ns
T_{SSH}	SSI data hold	—	30	—	ns



*Default polarity
Individual B-channel switching to the B1 and B2 channel can be selected by programming the output polarity of PSC1 and FSC2 in the ADFR register.

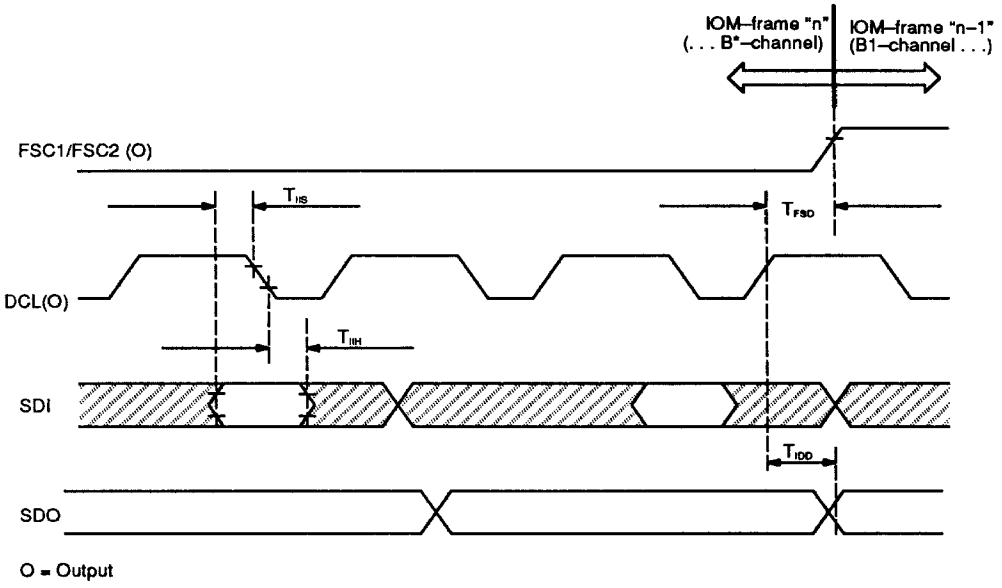
11136-034B

O = Output

Figure 34. SSI (TE Mode)

Table 14. IOM Interface/(HDLC Port) Timing

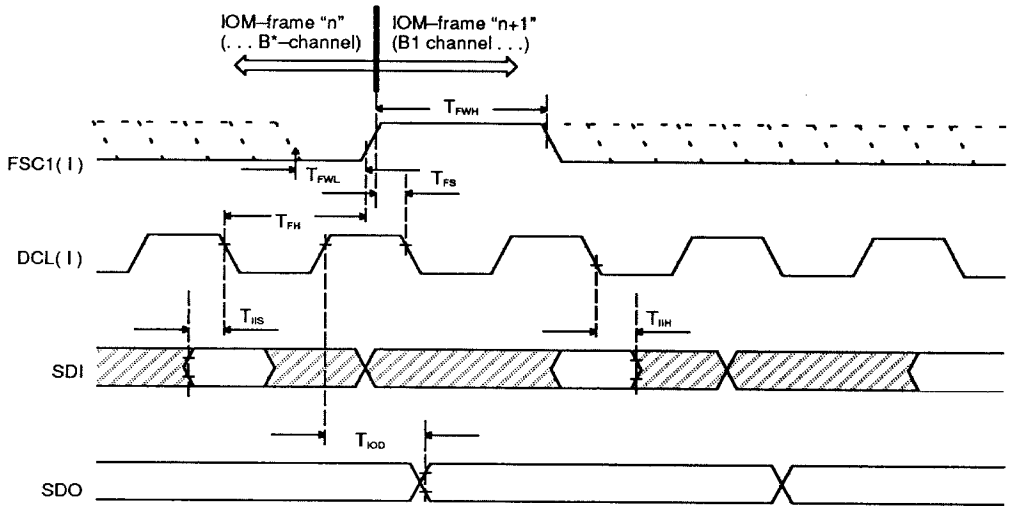
Parameter Symbol	Parameter Description	Test Conditions	Limit Values Min.	Max.	Unit
T_{DH}	Frame sync. hold	—	30		ns
T_{FS}	Frame sync. setup	—	50		ns
T_{FWH}	Frame sync. high	—	40		ns
T_{FWL}	Frame sync. low	—	2150		ns
T_{FSD}	Frame sync. delay	—	–20	20	ns
T_{IOD}	IOM output data delay	—	—	200	ns
T_{IIS}	IOM input data setup	—	20		ns
T_{IIH}	IOM input data	—	50		ns



O = Output

Figure 35. IOM (TE Mode)

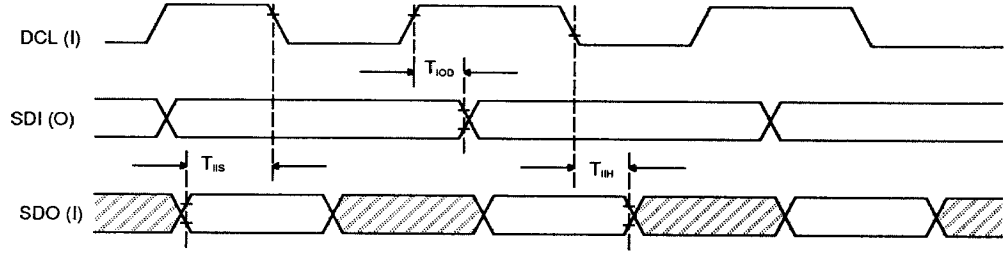
11136-035B



Note: At the SDI pin an internal Pull-Up Resistor is integrated for the TIC bus configuration with wired-OR connections (open drain outputs).

11136-036B

Figure 36. IOM (NT, LT-S, LT-T Mode)



HDLC port mode: – FSC1 = "High"
– HMD0,1,2 bits in MODE are set
– TEM—bit in ADFR is set

11136-37B

Figure 37. HDLC Port Mode

Clock Timing

The clocks in the different operating modes are summarized in Table 15, with the respective duty ratios.

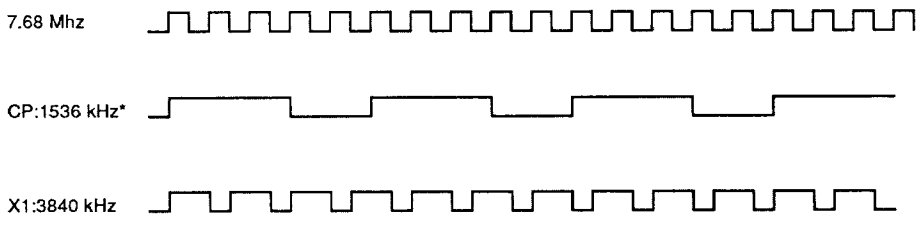
Table 15. ISAC-S Clock Signals

Application	M1	M0	DCL	FSC1/FSC2	CP	X1	X0
TE	0	0	O:512 kHz* 2:1	O:8 kHz* 1:1	O:1536 kHz* 3:2	O:3840 kHz 1:1	
LT-T	0	1	I:512 kHz	I:8 kHz	O:512 kHz* 2:1	—	—
LT-S	1	0	I:512 kHz	I:8 kHz	— —	O:7680 kHz 1:1	I:fixed at 0
NT	1	1	I:512 kHz	I:8 kHz	—	—	—

*Synchronous to receive "S" line P.

Clock CP is phase-locked to the receive S signal and is derived using the internal DPLL and the 7.68-MHz ±100 ppm crystal (TE and LT-T). A phase tracking of CP with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68-MHz period (CP duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since DCL and FSC1/FSC2 are derived from CP (TE mode), the high or low states of FSC1/FSC2 and DCL may likewise be reduced or extended by the same amount once every 250 µs.

Note: The phase adjustment may take place either in the sixth, seventh, or eighth CP cycle counting from the beginning of an IOM frame in TE.



*Synchronous to receive "S," Duty ratio 3:2 normally

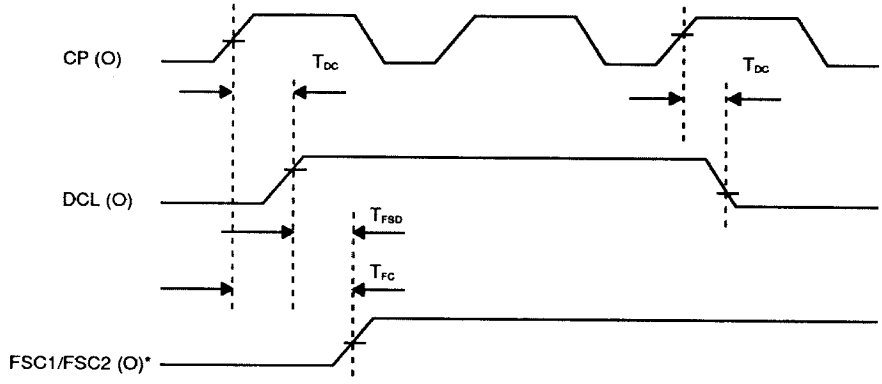
11136-038B

Figure 38. Phase Relationships of Auxiliary Clocks

The timing relationships between CP, DCL and FSC1/FSC2 are specified in Table 16 and Figure 39.

Table 16. CP, DCL, and FSC1/FSC2 Timing Specifications

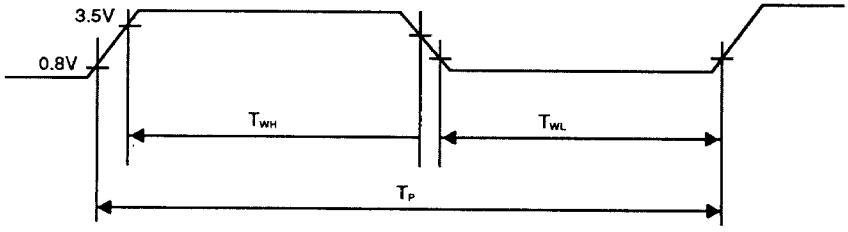
Symbol	Description	Test Conditions	Min.	Max.	Unit
T_{DC}	Clock delay CP-DCL	—	0	50	ns
T_{FC}	Clock delay CP-SC	—	0	50	ns
T_{FSD}	Frame sync delay	—	–20	20	ns



*Default polarity (can be programmed in ADFR).

11136-039B

Figure 39. CP, DCL, FSC1/FSC2 Timing Relationships



11136-040B

Figure 40. Definition of Clock Period and Width

Tables 17 through 19 give the timing characteristics of the clocks.

Table 17. Clocks Timing

Symbol	DCL Description	Test Conditions	Min.	Typ.	Max.	Unit
T_P Output	(TE) 512 kHz	Osc ±100 ppm	1822	1953	2084	ns
T_{WH} Output	(TE) 512 kHz 2:1	Osc ±100 ppm	1121	1302	1483	ns
T_{WL} Output	(TE) 512 kHz 2:1	Osc ±100 ppm	470	651	832	ns
T_{WH} Output	(NT, LT-S, LT-T)	—	200	—	—	ns
T_{WL} Output	(NT, LT-S, LT-T)	—	200	—	—	ns

Table 18. Clocks Timing

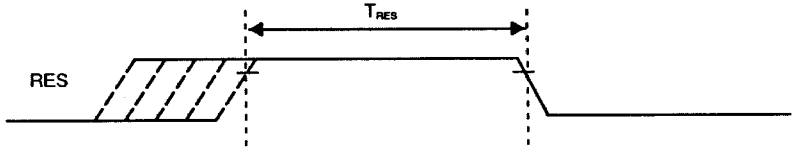
Symbol	CP Description	Test Conditions	Min.	Typ.	Max.	Unit
T_P Output	(TE) 1536 kHz	Osc ±100 ppm	520	651	782	ns
T_{WH} Output	(TE) 1536 kHz	Osc ±100 ppm	240	391	541	ns
T_{WL} Output	(TE) 1536 kHz	Osc ±100 ppm	24	260	281	ns
T_R, T_F	(TE, LT-T)	CL = 100 pF	—	—	20	ns
		CL = 50 pF	—	—	10	ns
T_P Output	(LT-T) 512 kHz	Osc ±100 ppm	1822	1953	2084	ns
T_{WH} Output	(LT-T) 512 kHz	Osc ±100 ppm	1121	1302	1483	ns
T_{WL} Output	(LT-T) 512 kHz	Osc ±100 ppm	470	651	832	ns

Table 19. Clocks Timing

Symbol	X1 Description	Test Conditions	Min.	Typ.	Max.	Unit
T_P Output	(TE) 3840 kHz	Osc ±100 ppm	−100 ppm	260	+100 ppm	ns
T_{WH} Output	(TE) 3840 kHz	Osc ±100 ppm	120	130	140	ns
T_{WL} Output	(TE) 3840 kHz	Osc ±100 ppm	120	130	140	ns

Table 20. Reset

Symbol	Parameter	Test Conditions	Min.	Unit
T_{RES}	Length of active high-state cycles	Power on/power down to Power Up (standby)	4	ms
		During Power Up (standby)	2 • DCL clock	



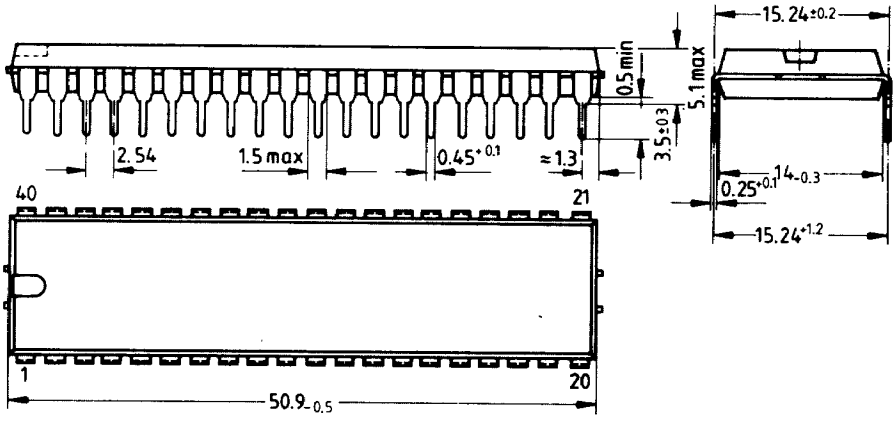
11136-041B

Figure 41. Reset Width

PHYSICAL DIMENSIONS

Note: All dimensions in metric.

PD040



PL044