µPSD3200 FAMILY

Flash Programmable System Device with 8032 Microcontroller Core

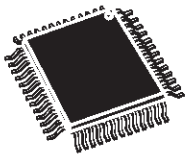
DATA BRIEFING

FEATURES SUMMARY

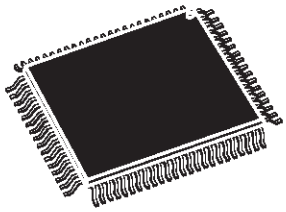
- The µPSD3200 Family combines a Flash PSD architecture with an 8032 microcontroller core

  The µPSD3200 Family of Flash PSDs features dual banks of Flash memory, SRAM, general purpose I/O and programmable logic, supervisory functions and access via USB, I^2C, ADC, DDC and PWM channels, and an on-board 8032 microcontroller core, with two UARTs, three 16-bit Timer/Counters and one External Interrupt. As with other Flash PSD families, the µPSD3200 Family is also in-system programmable (ISP) via a JTAG ISP interface.
- Large 8 KByte SRAM with battery back-up option
- Dual bank Flash memories
  - 128 KByte or 256 KByte main Flash memory
  - 32 KByte secondary Flash memory
- Content Security
  - Block access to Flash memory
- Programmable Decode PLD for flexible address mapping of all memories.
- High-speed clock standard 8032 core (12-cycle)
- USB Interface (µPSD3234A-40U6 only)
- I^2C interface for peripheral connections
- Five Pulse Width Modulator (PWM) channels
- Standalone Display Data Channel (DDC)
- Six I/O ports with up to 50 I/O pins
- 3000 gate PLD with 16 macrocells
- Supervisor functions
- In-System Programming (ISP) via JTAG
- Zero-Power Technology
- Single Supply Voltage
  - 4.5 to 5.5 V
  - 3.0 to 3.6 V

Figure 1. Packages



TQFP52 (T)



TQFP80 (U)

SUMMARY DESCRIPTION

- Dual bank Flash memories
  - Concurrent operation, read from memory one while erasing and writing the other. In-Application Programming (IAP) for remote updates
  - Large 128 KByte or 256 KByte main Flash memory for application code, operating systems, or bit maps for graphic user interfaces
  - Large 32 KByte secondary Flash memory divided in small sectors. Eliminate external EEPROM with software EEPROM emulation
  - Secondary Flash memory is large enough for sophisticated communication protocol (USB) during IAP while continuing critical system tasks
- Large SRAM with battery back-up option
  - 8 KByte SRAM for RTOS, high-level languages, communication buffers, and stacks
- Programmable Decode PLD for flexible address mapping of all memories
  - Place individual Flash and SRAM sectors on any address boundary
  - Built-in page register breaks restrictive 8032 limit of 64 KByte address space
  - Special register swaps Flash memory segments between 8032 “program” space and “data” space for efficient In-Application Programming
- High-speed clock standard 8032 core (12-cycle)
  - 40 MHz operation at 5 V, 24 MHz at 3.3 V
  - Two UARTs with independent baud rate, three 16-bit Timer/Counters and two External Interrupts
- USB Interface (µPSD3234A-40U6 only)
  - Supports USB 1.1 Slow Mode (1.5 Mbit/s)
  - Control endpoint 0 and interrupt endpoints 1 and 2
- I^2C interface for peripheral connections
  - Capable of master or slave operation
- Five Pulse Width Modulator (PWM) channels
  - Four 8-bit PWM units
  - One 16-bit PWM unit
- Standalone Display Data Channel (DDC)
  - For use in monitor, projector, and TV applications
  - Compliant with VESA standards DDC1 and DDC2B
  - Eliminate external DDC PROM
- Six I/O ports with up to 50 I/O pins
  - Multifunction I/O: GPIO, DDC, I^2C, PWM, PLD I/O, supervisor, and JTAG
  - Eliminates need for external latches and logic
- 3000 gate PLD with 16 macrocells
  - Create glue logic, state machines, delays, etc.
  - Eliminate external PALs, PLDs, and 74HCxx
  - Simple PSDsoft Express software ...Free
- Supervisor functions
  - Generates reset upon low voltage or watchdog time-out. Eliminate external supervisor device
  - Reset In pin
- In-System Programming (ISP) via JTAG
  - Program entire chip in 10 - 25 seconds with no involvement of 8032
  - Allows efficient manufacturing, easy product testing, and Just-In-Time inventory
  - Eliminate sockets and pre-programmed parts
  - Program with FlashLINK™ cable and any PC
- Content Security
  - Programmable Security Bit blocks access of device programmers and readers
- Zero-Power Technology
  - Memories and PLD automatically reach standby current between input changes
- Packages
  - 52-pin TQFP
  - 80-pin TQFP: allows access to 8032 address/data/control signals for connecting to external peripherals

Figure 2. µPSD3200 Family Functional Modules

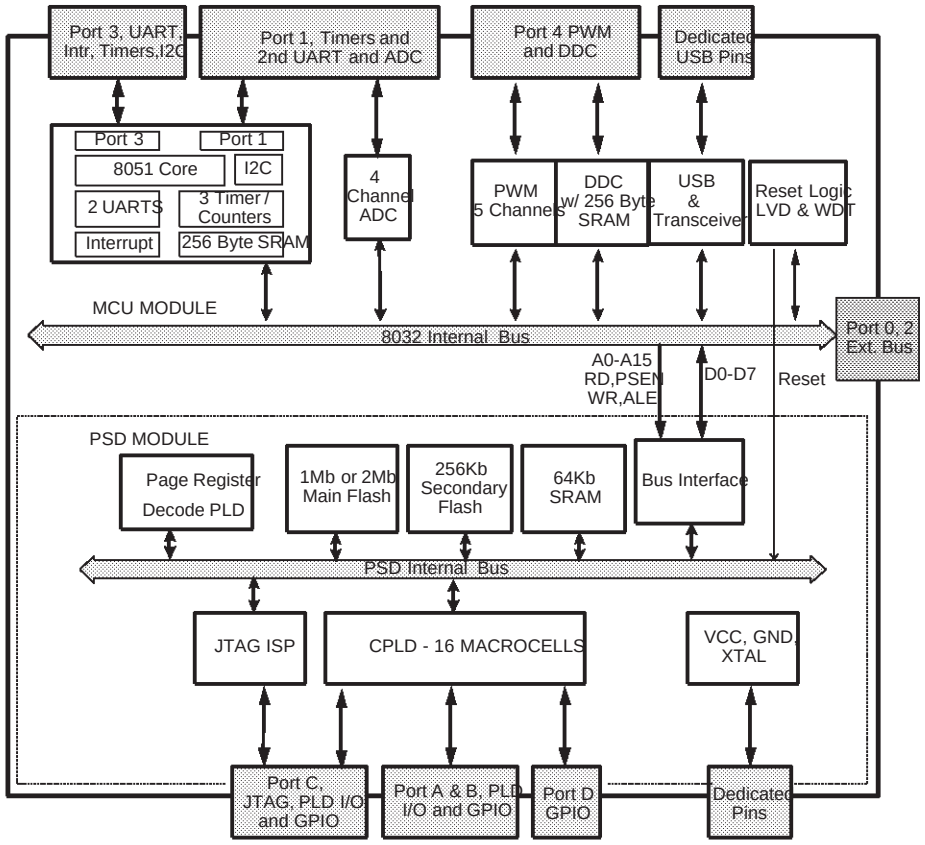
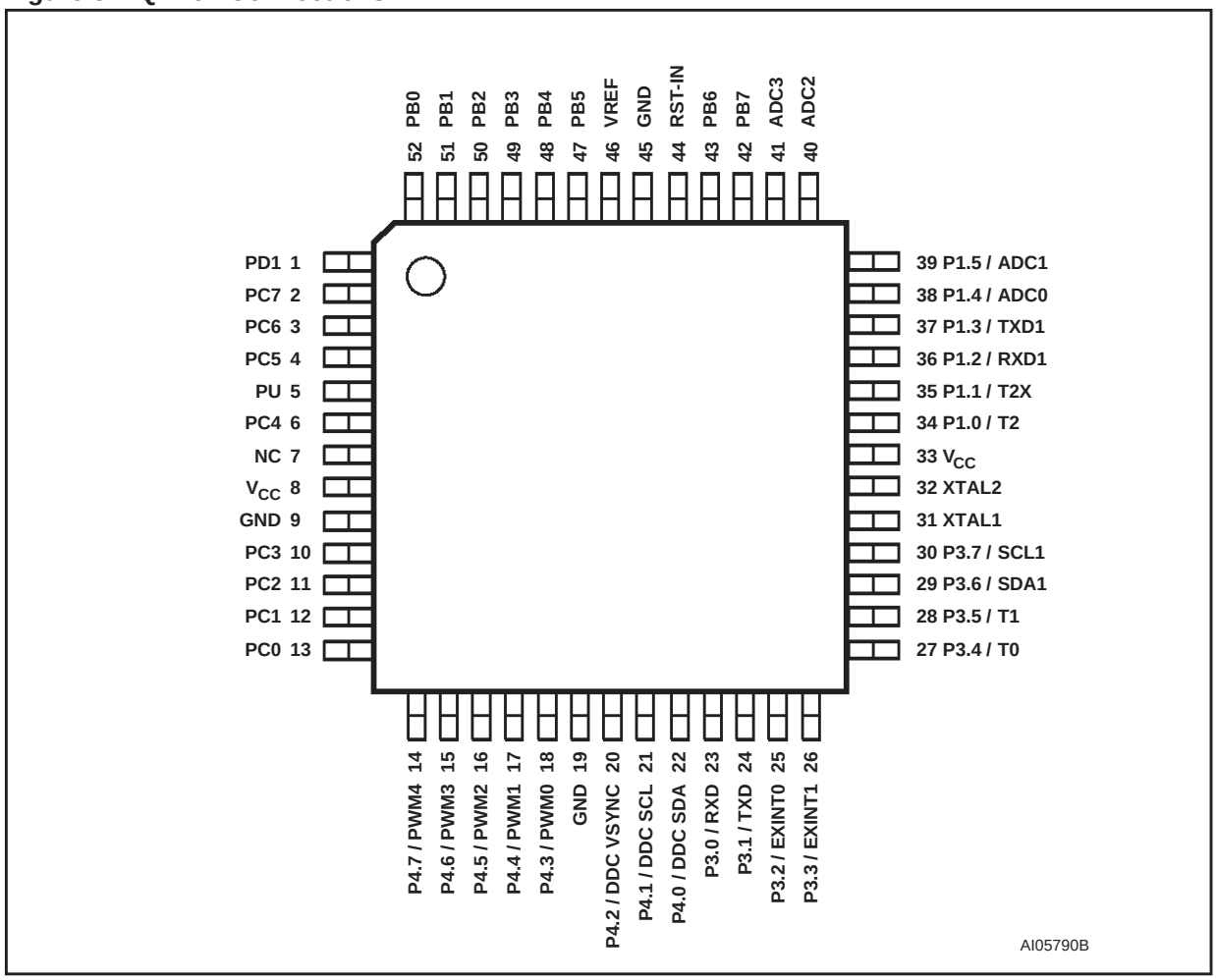


Table 1. 80-Pin Package Pin Description

Signal Name	In/Out	Function	
		Basic	Alternate
AD7-AD0	I/O	Multiplexed Address/Data bus	
A11-A8	I/O	External Address Bus	
RxD2-RxD1	I/O	General I/O port pins	UART Receive
TxD2-TxD1	I/O		UART Transmit
INT1-INT0	I/O		Interrupt inputs / timer gate controls
T2-T0	I/O		Counter inputs
SDA1-SDA2	I/O		I^2C Bus serial data I/O / DDC interface
SCL1-SCL2	I/O		I^2C Bus clock I/O
VSYNC	I/O		VSYNC input for DDC interface
T2EX	I/O		Timer 2 Trigger input
ADC3-ADC0	I/O		ADC Channels input
PWM4-PWM0	I/O		8-bit Pulse Width Modulation outputs
USB-, USB+	I/O	USB I/O	
AVREF	O	Reference Voltage input for ADC	
RD_	O	Read signal, external bus	
WR_	O	Write signal, external bus	
PSEN_	O	PSEN signal, external bus	
ALE	O	Address Latch signal, external bus	
RESET_	I	Active low reset input	
XTAL1	I	Oscillator input pin for system clock	
XTAL2	O	Oscillator output pin for system clock	
PA7-PA0	I/O	General I/O port pins	1. PLD Macro-cell outputs 2. PLD inputs 3. Latched Address Out (A0-A7) 4. Peripheral I/O mode
PB7-PB0	I/O	General I/O port pins	1. PLD Macro-cell outputs 2. PLD inputs 3. Latched Address Out (A0-A7)
PC7-PC0	I/O	General I/O port pins	1. PLD Macro-cell outputs 2. PLD inputs 3. SRAM stand by voltage input (VSTBY) 4. JTAG Interface (TDI, TDO, TMS, TCK, TSTAT, TERR) 5. SRAM battery-on indicator (PC4)
PD2-PD1	I/O	General I/O port pin	1. PLD I/O 2. Clock input to PLD and APD 3. Chip select to PSD Module

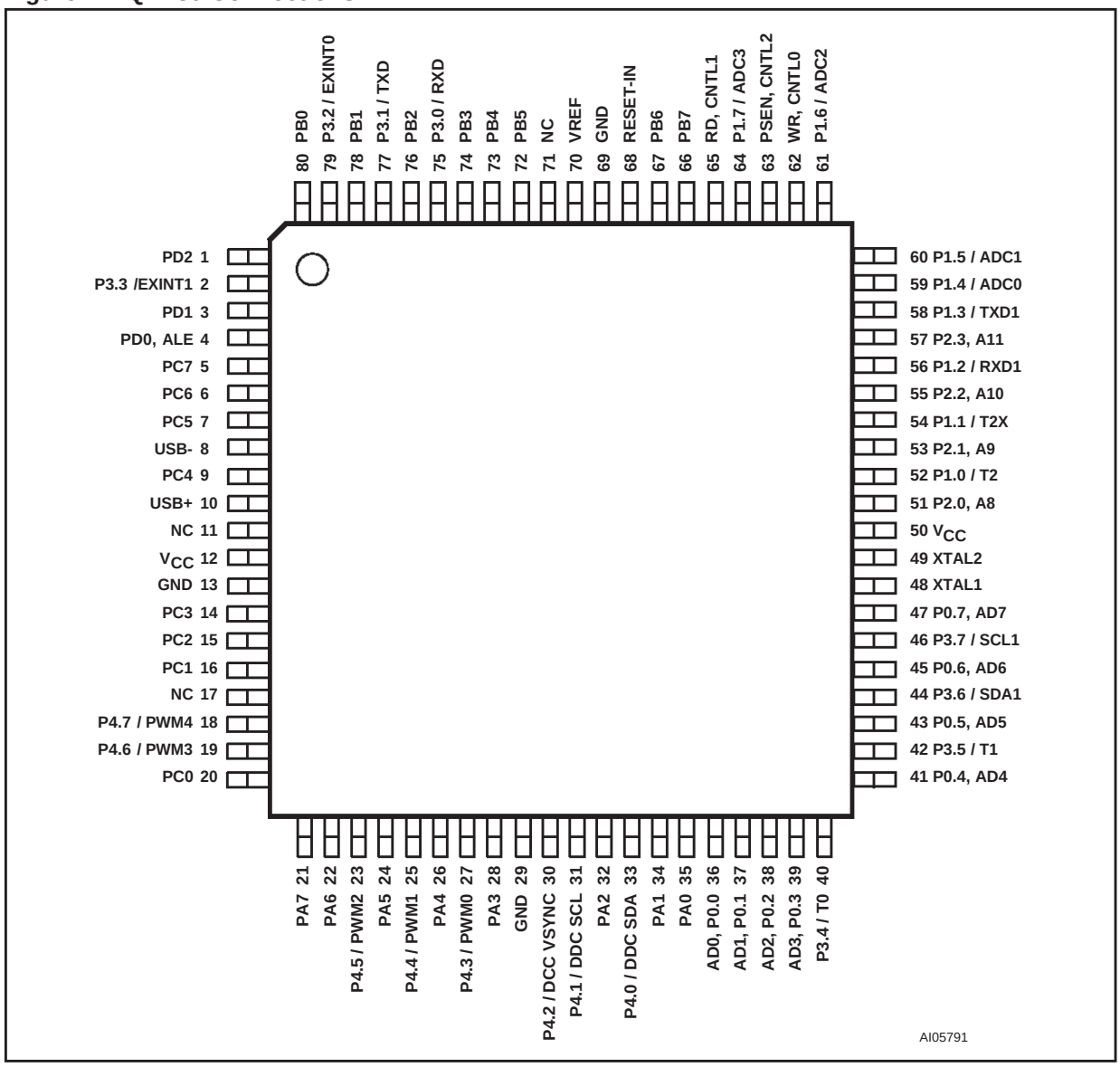
Note: PSD Port A and MCU Address/Data bus are added for 80-pin device

Figure 3. TQFP52 Connections



Note: NC = Not Connected
PU = Pull-up resistor required (2kΩ for 3V devices, 7.5kΩ for 5V devices)

Figure 4. TQFP80 Connections



Note: 1. NC = Not Connected
2. USB- needs a pull-up resistor (see the description of the USB function)

PART NUMBERING

Table 2. Ordering Information Scheme

Example: uPSD 3 2 3 4 B V – 24 U 6 T

Device Type
uPSD = Microcontroller PSD

Family
3 = 8032 core

PLD Size
2 = 16 Macrocells
3 = 32 Macrocells

SRAM Size
1 = 16 Kbit
3 = 64 Kbit
5 = 256 Kbit

Main Flash Memory Size
3 = 1 Mbit
4 = 2 Mbit
5 = 4 Mbit

IP Mix
A = USB, I^2C, PWM, DDC, ADC, (2) UARTs Supervisor (Reset Out, Reset In, LVD, WD)
B = I^2C, PWM, DDC, ADC, (2) UARTs Supervisor (Reset Out, Reset In, LVD, WD)

Operating Voltage
blank = V_{CC} = 4.5 to 5.5V
V = V_{CC} = 3.0 to 3.6V

Speed
24 = 24 MHz
40 = 40 MHz

Package
T = 52-pin TQFP
U = 80-pin TQFP

Temperature Range
1 = 0 to 70 °C (commercial)
6 = –40 to 85 °C (industrial)

Option
T = Tape & Reel Packing

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.