

NUP4103FC

Four Channel ESD Array

This integrated transient voltage suppressor device (TVS) is designed for applications requiring transient overvoltage protection. It is intended for use in sensitive portable equipment and other applications. Its integrated design provides very effective and reliable protection for four (4) separate lines using only one package. These devices are ideal for situations where board space is a premium.

Features

- Unidirectional, Quad ESD Protection
- Ultra-small Flip Chip Packaging (0.95 mm x 1.33 mm)
- Compliance with IEC61000-4-2 (Level 4) Requirements
- Maximum Leakage Current of 100 nA at 3.3 V

Benefits

- Protects Four Data Lines from ESD while Reducing Component Count
- Small Package Saves On PCB Real Estate
- Provides Protection for ESD Industry Standards, IEC 61000, HBM and MM
- Low Leakage Capability Minimizes Power Loss in the System

Applications

- ESD Protection for Portable Equipment
- Cell Phones
- MP3 Players
- PDAs

MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

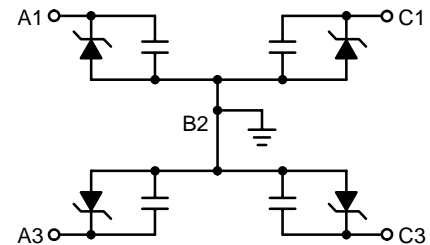
Rating	Symbol	Value	Unit
ESD Discharge IEC61000-4-2, - Air Discharge - Contact Discharge Human Body Model Machine Model	V _{PP}	30 30 16 1.6	kV
Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{STG}	-55 to +150	°C



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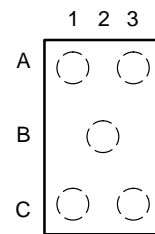
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CIRCUIT DESCRIPTION

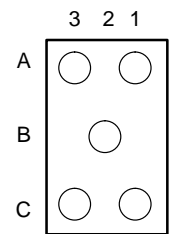


5 PIN FLIP CHIP CSP
CASE 766AB
PLASTIC

TOP VIEW
(Bumps Down)



BOTTOM VIEW
(Bumps Up)



DEVICE MARKING



E = Specific Device Code
D = Month Code

ORDERING INFORMATION

Device	Package	Shipping
NUP4103FCT1	Flip Chip	3000/Tape & Reel

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V _{RWM}	I _{RWM} = 10 μA (Note 1)			5.5	V
Breakdown Voltage	V _{BR}	I _T = 1.0 mA (Note 2)	6.0	7.0	8.0	V
Leakage Current	I _R	V _{RM} = 3.3 V per line			100	nA
Junction Capacitance	C _J	V _R = 2.5 V, f = 1 MHz		30		pF

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}) which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise specified)

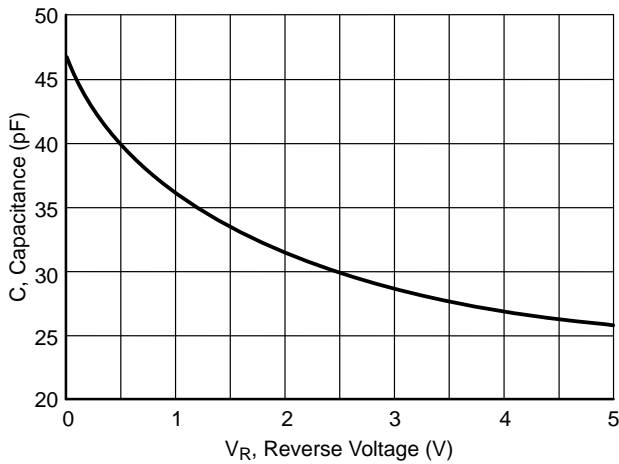


Figure 1. Reverse Voltage vs Junction Capacitance

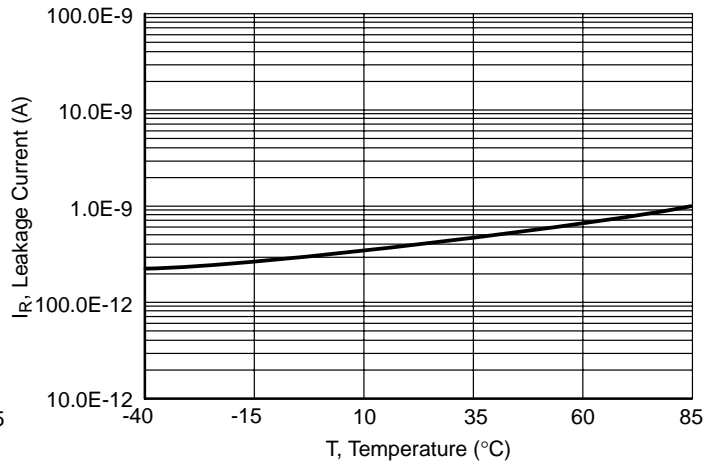


Figure 2. Reverse Leakage Current vs Junction Temperature

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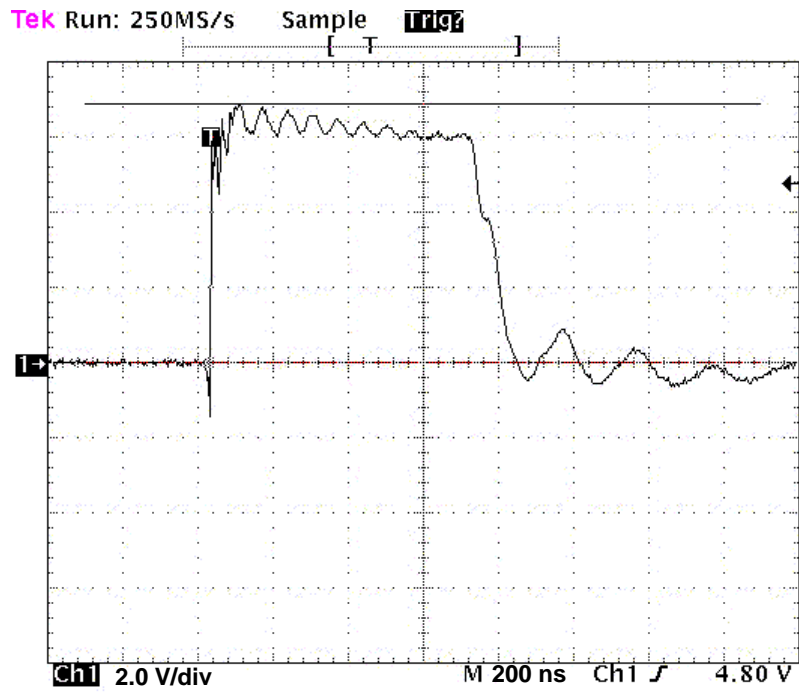


Figure 3. ESD Response for Human Body Model (+8 kV)

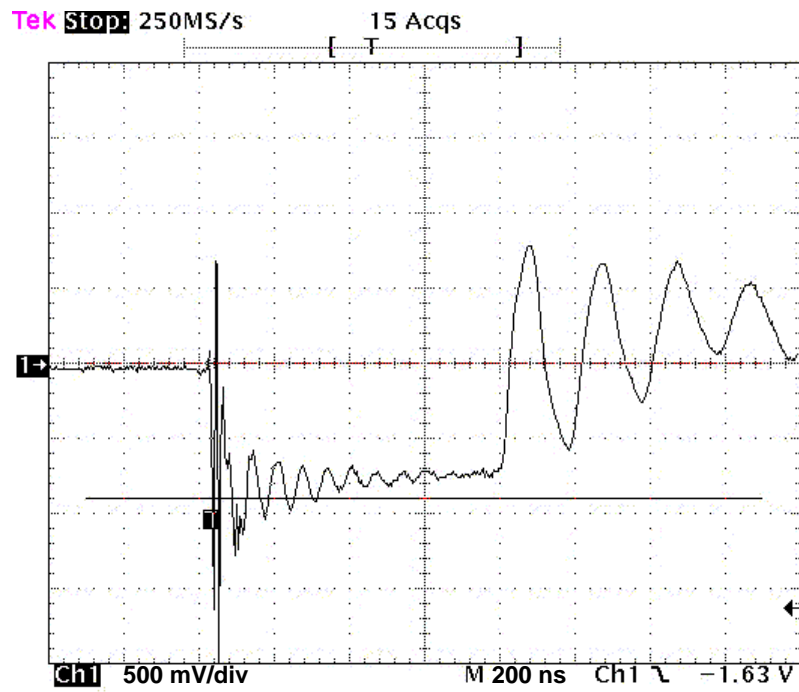


Figure 4. ESD Response for Human Body Model (-8 kV)

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Printed Circuit Board Recommendations

Parameter	500 μm Pitch 300 μm Solder Ball
PCB Pad Size	250 μm +25 / -0
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm \pm 25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

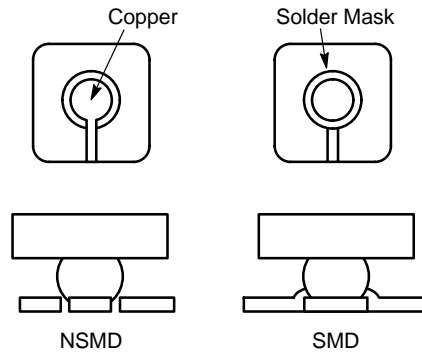


Figure 5. Solder Mask versus Non-Solder Mask Definition

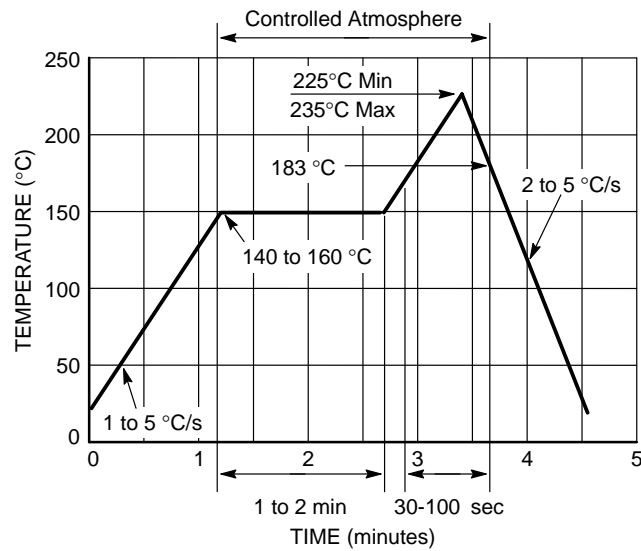
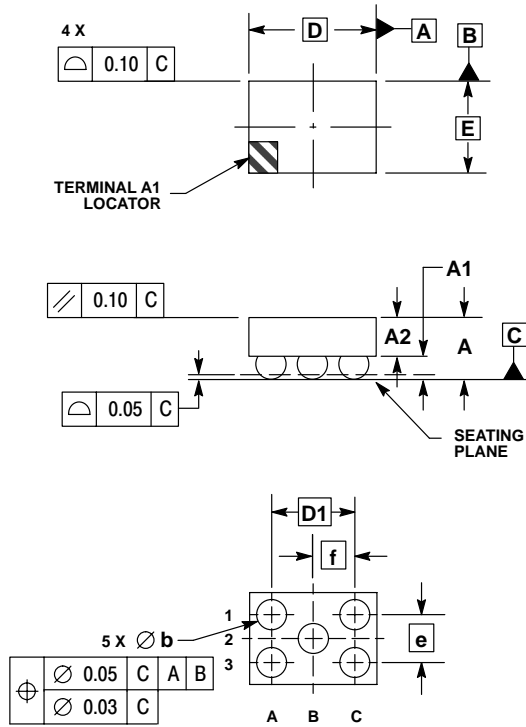


Figure 6. Solder Reflow Profile

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PACKAGE DIMENSIONS


5 PIN FLIP CHIP CSP CASE 766AB-01 ISSUE 0



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.680
A1	0.210	0.270
A2	0.380	0.430
D	1.330 BSC	
E	0.960 BSC	
b	0.290	0.340
e	0.500 BSC	
f	0.433 BSC	
D1	0.866 BSC	

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