QUINT 2-INPUT AND/NAND GATE

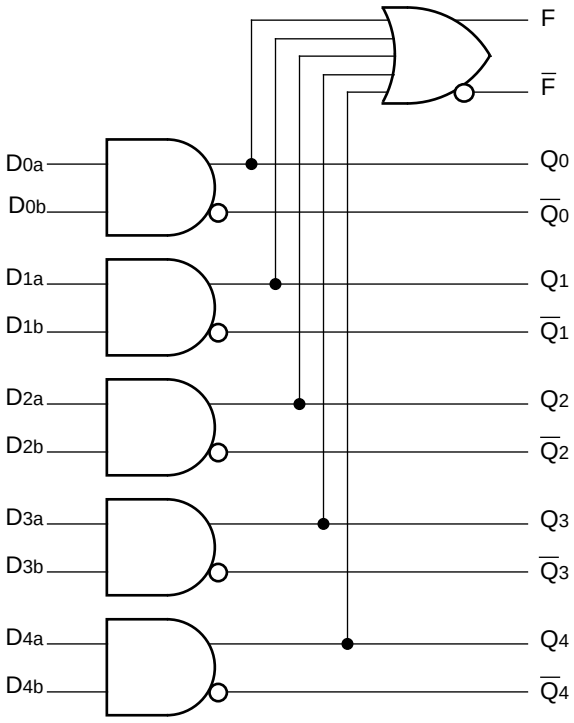
FEATURES

- **600ps max. propagation delay**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **True and complementary outputs**
- **OR/NOR function outputs**
- **Fully compatible with Industry standard 10KH, 100K I/O levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E104**
- **Available in 28-pin PLCC package**

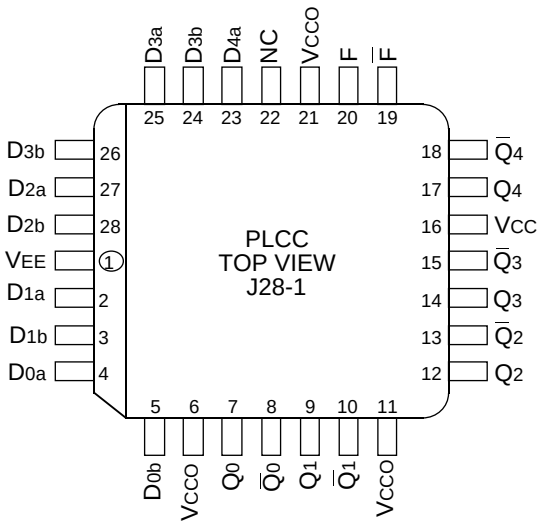
DESCRIPTION

The SY10/100E104 are quint 2-input AND/NAND gates designed for use in new, high-performance ECL systems. The E104 also features a function output, F, which is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. Both true and complementary outputs are provided.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{na}, D_{nb}	Data Inputs
Q_0-Q_4	AND Outputs
$\overline{Q}_0$-$\overline{Q}_4$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output
V_{CCO}	V_{CC} to Output

Rev.: E Amendment: /0
Issue Date: November, 1998

LOGIC EQUATION

$F = (D_{0a} \bullet D_{0b}) + (D_{1a} \bullet D_{1b}) + (D_{2a} \bullet D_{2b}) + (D_{3a} \bullet D_{3b}) + (D4a \bullet D_{4b})$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = -40°C$			$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	—	—	200	µA
I_{EE}	Power Supply Current													mA
	10E	—	38	46	—	38	46	—	38	46	—	38	46	
	100E	—	38	46	—	38	46	—	38	46	—	44	53	

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = -40°C$			$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	225	385	600	225	385	600	225	385	600	225	385	600	ps
	D to F	500	725	1000	500	725	1000	500	725	1000	500	725	1000	
t_{skew}	Within-Device Skew, D to Q[1]	—	75	—	—	75	—	—	75	—	—	75	—	ps
t_r t_f	Rise/Fall Time 20% to 80% Q	275	425	700	275	425	700	275	425	700	275	425	700	ps
	F	300	475	700	300	475	700	300	475	700	300	475	700	

NOTE:

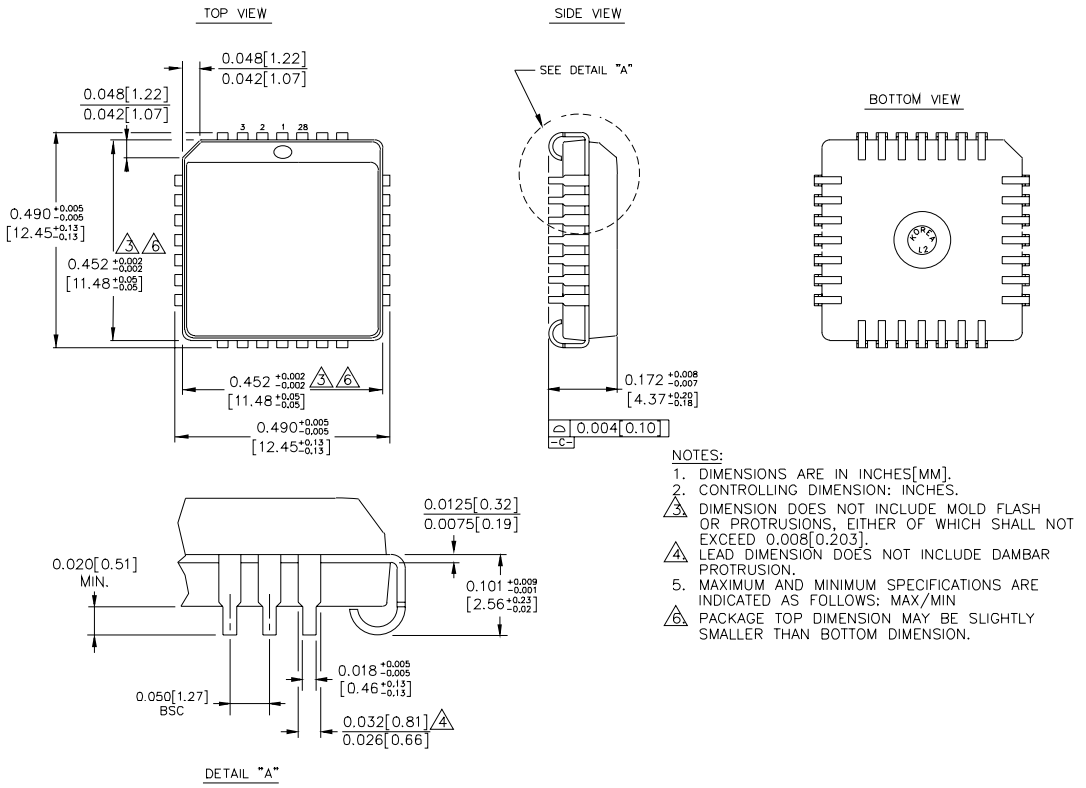
1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E104JC	J28-1	Commercial
SY10E104JCTR	J28-1	Commercial
SY100E104JC	J28-1	Commercial
SY100E104JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY10E104JI	J28-1	Industrial
SY10E104JITR	J28-1	Industrial
SY100E104JI	J28-1	Industrial
SY100E104JITR	J28-1	Industrial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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