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(IBM Order Number)

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REV 1

PowerPC™

Advance Information

PowerPC 604™ RISC Microprocessor Hardware Specifications

The PowerPC 604 microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the 604. For information about the functionality of the 604, refer to the *PowerPC 604 RISC Microprocessor Users Manual.*

This document contains the following topics:

In this document, the term “604” is used as an abbreviation for the phrase “PowerPC 604 microprocessor.” The PowerPC 604 microprocessors are available from IBM as PPC604 and from Motorola as MPC604.

IBM

MOTOROLA

1.1 General Parameters

Technology	0.5 μm CMOS, four-layer metal
Chip size	196 mm^2, 12.4 mm x 15.8 mm
Packages	Surface-mount 304-pin C4-CQFP
	Surface-mount 255-lead ceramic ball grid array (BGA)
Voltage	3.3 V ± 5%
Maximum power dissipation	24 W @ 133 MHz
	19 W @ 100 MHz

1.2 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 604. The following specifications are preliminary and subject to change without notice. For the most recent specifications, contact your local Motorola or IBM sales office.

1.2.1 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum rating and thermal characteristics for the 604.

Table 1. PowerPC 604 Microprocessor Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	Vdd	–0.3 to 3.6	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional operating conditions are given in DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Input voltage must not be greater than the supply voltage by more than 2.5 V during power-on reset.

Table 2. PowerPC 604 Microprocessor Thermal Characteristics

Characteristic	Symbol	Value	Rating
C4-CQFP package thermal resistance, junction-to-case	θ_{JC}	0.03	°C/W
BGA package thermal resistance, junction-to-case	θ_{JC}	0.03	°C/W

Notes:

1. For the BGA package, the θ_{JC} measurement is made from die junction to the back of the bare silicon die.
2. The junction temperature of the chip is a function of several parameters including θ_{JC}. Please refer to Section 1.8, “Thermal Management Information,” for additional details.

Table 3 provides the DC electrical characteristics for the 604.

Table 3. PowerPC 604 Microprocessor DC Electrical Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C, Input capacitance = 10 pF maximum

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	0	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	0	0.4	V
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 9 mA	V_{OL}	—	0.4	V

Table 4 provides the power dissipation numbers for the 604.

Table 4. PowerPC 604 Microprocessor Power Dissipation

	Processor Core Frequency			Unit	Notes
	100 MHz	120 MHz	133 MHz		
Full-On Mode					1
Typical	14.5	17.0	18.5	W	2
Maximum	19.0	22.5	24.0	W	3

Notes:
1. Power measured does not include power dissipated in output drivers.
2. Typical power is an average value measured at 3.3 V in a system executing typical applications and benchmark sequences. Typical power numbers should be used in planning for proper thermal management.
3. Maximum power is measured at 3.3 V using a worst case instruction mix. These values should be used for power supply design.

1.3 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 604. These specifications are for parts that operate at processor core frequencies of 100, 120, and 133 MHz. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0–PLL_CFG3 pins. All timings are specified respective to the SYSCLK.

1.3.1 Clock AC Specifications

Table 5 provides the clock AC timing specifications as defined in Figure 1.

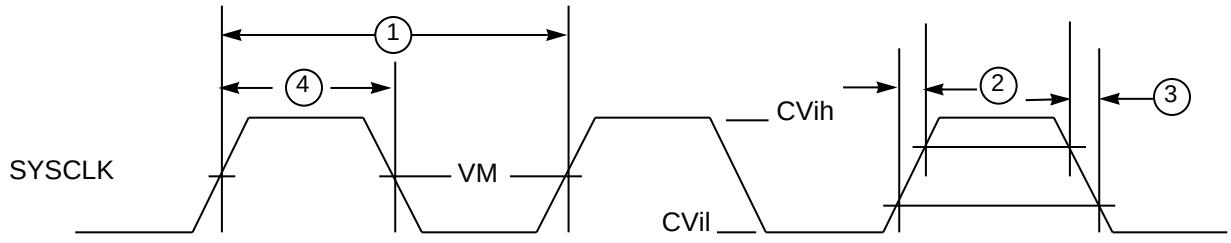
Table 5. PowerPC 604 Microprocessor Clock AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Frequency of operation	50	100.0	60.0	120.0	66.67	133.3	MHz	1
	Frequency of VCO	180	360	180	360	180	360	MHz	2
	SYSCLK frequency	16.67	66.67	20.0	66.67	22.2	66.67	MHz	3
1	SYSCLK cycle time	15.0	60.0	15.0	50.0	15.0	45.0	ns	
2,3	SYSCLK rise and fall time	1.0	2.0	1.0	2.0	1.0	2.0	ns	4
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	40	60	%	
5	SYSCLK jitter	—	±150	—	±150	—	±150	ps	5
6	Internal PLL relock time	—	100	—	100	—	100	µs	6, 7

Notes:
1. Times shown in specifications are only valid for the range of processor core frequencies specified.
2. **Caution**: The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
3. AC timing specifications are tested up to the maximum SYSCLK (bus) frequency shown in Table 5. However, it is theoretically possible to attain higher SYSCLK frequencies if allowed for by system design.
4. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
5. This number refers to cycle-to-cycle jitter.
6. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
7. Relock timing is guaranteed by design and is not tested.

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.3.2 Input AC Specifications

Table 6 provides the input AC timing specifications for the 604 as defined in Figure 2.

Table 6. PowerPC 604 Microprocessor Input AC Timing Specifications

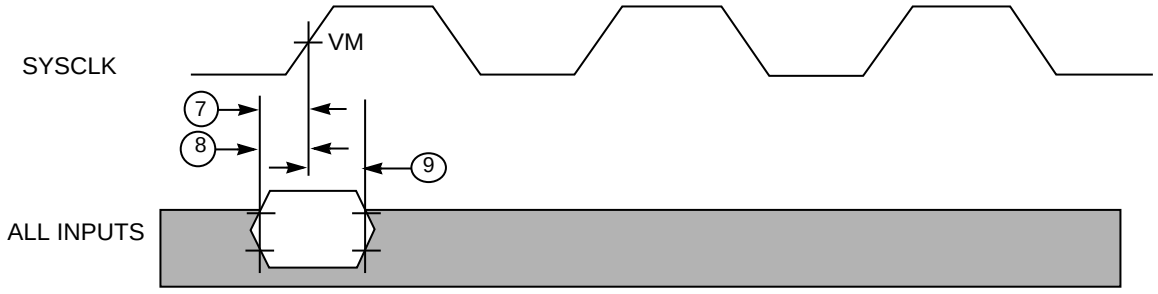
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
7	$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$,$\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, and $\overline{\text{DBWO}}$ valid to SYSCLK (setup)	5.5	—	5.0	—	5.0		ns	
8	All other inputs valid to SYSCLK (setup)	5.5	—	4.0	—	4.0	—	ns	1
9	SYSCLK to all inputs invalid (hold)	0	—	0	—	0	—	ns	1
10	Mode select input valid to $\overline{\text{HRESET}}$ (input setup for $\overline{\text{DRTRY}}$)	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	ns	2,3,4,5
11	$\overline{\text{HRESET}}$ to mode select input invalid (input hold for $\overline{\text{DRTRY}}$)	0	—	0	—	0	—	ns	2,3,4,5

Notes:

1. All other input signals include the following signals—all inputs except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{DBWO}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TEA}}$, and JTAG inputs.
2. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
3. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
4. These values are guaranteed by design, and are not tested.
5. Note this is for configuration of the fast-L2 mode. The $\overline{\text{DRTRY}}$ signal must be held negated during fast-L2 mode.

Figure 2 provides the input timing diagram for the 604.



VM = Midpoint Voltage (1.4V)

Figure 2. PowerPC 604 Microprocessor Input Timing Diagram

Figure 3 provides the timing diagram for the fast-L2 mode select input.

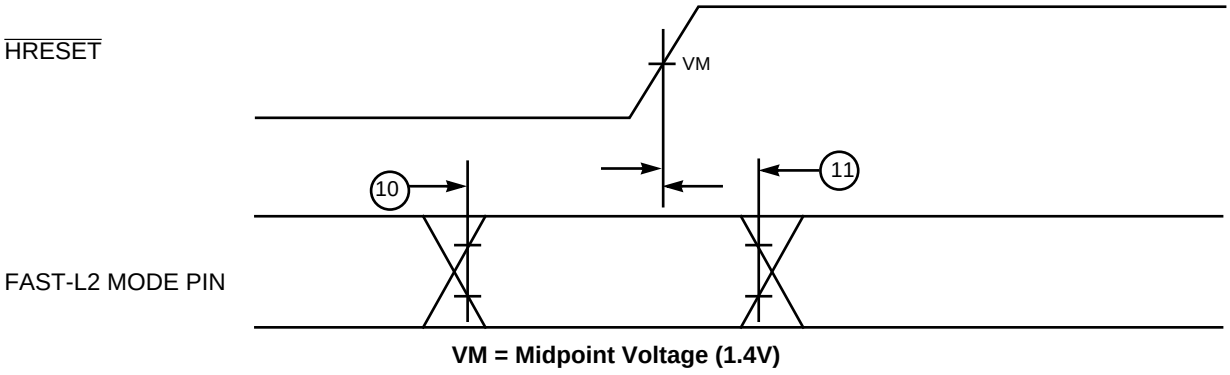


Figure 3. Fast-L2 Mode Select Input Timing Diagram

1.3.3 Output AC Specifications

Table 7 provides the output AC timing specifications for the 604 (shown in Figure 4).

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	0.75	—	0.75	—	0.75	—	ns	1
13a	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, and $\overline{DBB}$ output valid (for 5.5 V to 0.8 V)	—	8.5	—	7.5	—	7.0	ns	2
13b	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, and $\overline{DBB}$ output valid (for 3.6 V to 0.8 V)	—	7.5	—	6.5	—	6.0	ns	
14a	SYSCLK to all other signals output valid (for 5.5 V to 0.8 V)	—	8.5	—	7.5	—	7.0	ns	2
14b	SYSCLK to all other signals output valid (for 3.6 V to 0.8 V)	—	7.5	—	6.5	—	6.0	ns	
15	SYSCLK to output invalid (output hold)	1.0	—	1.0	—	1.0	—	ns	
16	SYSCLK to output high impedance (all signals except $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$, and $\overline{XATS}$)	—	7.0	—	6.5	—	6.0	ns	
17	SYSCLK to output high impedance $\overline{TS}$, $\overline{XATS}$	—	7.0	—	6.5	—	6.0	ns	
18	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge	—	1.0* t_{sysclk}	—	1.0* t_{sysclk}	—	1.0* t_{sysclk}	ns	3
19	SYSCLK to $\overline{ARTRY}$ and $\overline{SHD}$ high impedance before precharge	—	7.0	—	6.5	—	6.0	ns	

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications (Continued)

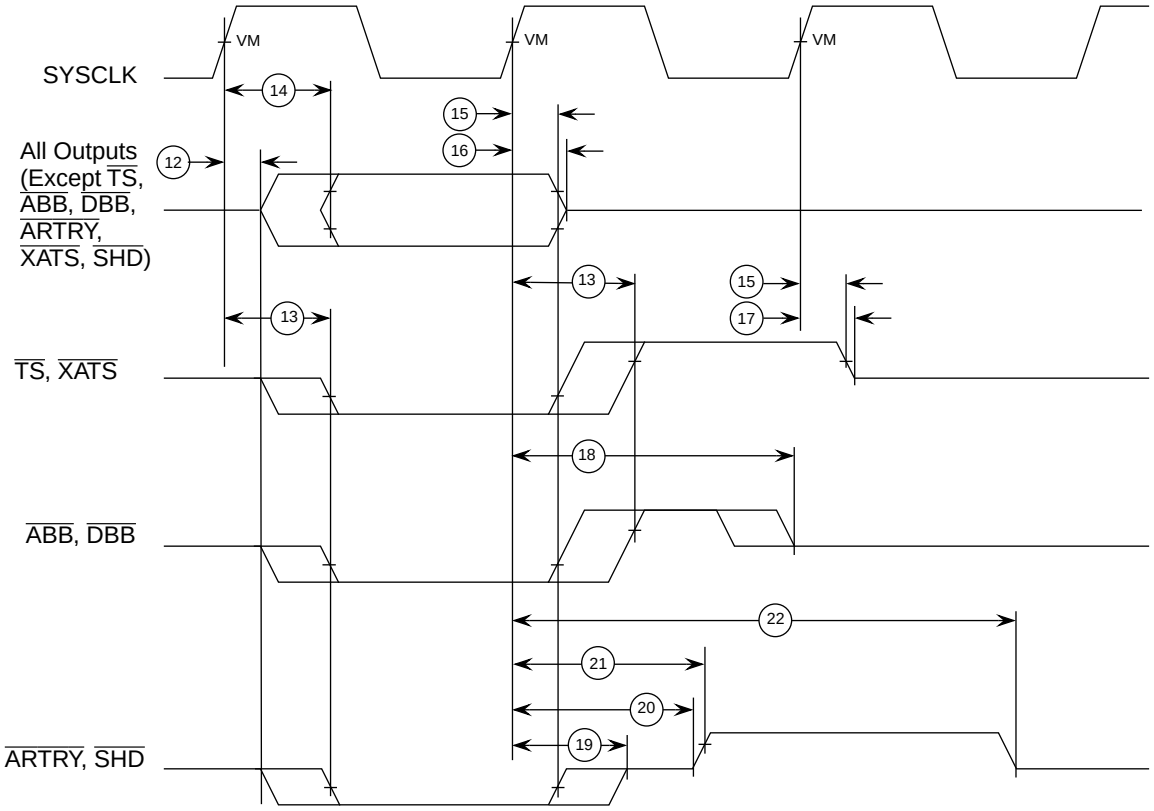
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
20	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ precharge enable	—	0.5* t_{sysclk} + 0.75	—	0.5* t_{sysclk} + 0.75	—	0.5* t_{sysclk} + 0.75	ns	3
21	Maximum delay to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ precharge	—	1.5* t_{sysclk}	—	1.5* t_{sysclk}	—	1.5* t_{sysclk}	ns	3
22	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge	—	2.0* t_{sysclk}	—	2.0* t_{sysclk}	—	2.0* t_{sysclk}	ns	3
	Rise time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Rise time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Fall time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Fall time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4

Notes:

1. These values are guaranteed by design, and are not tested.
2. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from 3.6 V to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
3. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
4. These specifications are nominal values.

Figure 4 provides the output timing diagram for the 604.



Notes: VM = Midpoint voltage (1.4 V)
All output specifications are measured from 0.8 V or 2.0 V of the signal in question to the 1.4 V of the rising edge of the input SYSCLK.

Figure 4. PowerPC 604 Microprocessor Output Timing Diagram

The output specifications of the 604 for both driving high and driving low depend on the capacitive loading on each output and the drive capability enabled for that output. Additionally, the timing specifications for outputs driving low also depend on the voltage swing required to drive to 0.8 V (either 5.5 V to 0.8 V or 3.6 V to 0.8 V). Table 7 provides the output AC timing specifications for a 50 pF load. In order to derive the actual timing specifications for a given set of conditions, it is recommended that IBIS simulation models be used. Contact the local Motorola or IBM sales office for information on the availability of these models.

1.3.4 JTAG AC Timing Specifications

Table 8 provides the JTAG AC timing specifications.

Table 8. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.5 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	2
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	0	—	ns	
7	Boundary-scan input data hold time	27	—	ns	
8	TCK to output data valid	4	35	ns	
9	TCK to output high impedance	3	24	ns	
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	1
13	TCK to TDO high impedance	3	15	ns	1

Notes:
1. Load capacitance = 50 pF.
2. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes.

Figure 5 provides the JTAG clock input timing diagram.

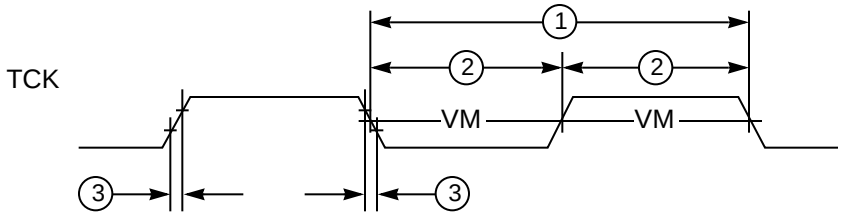


Figure 5. Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

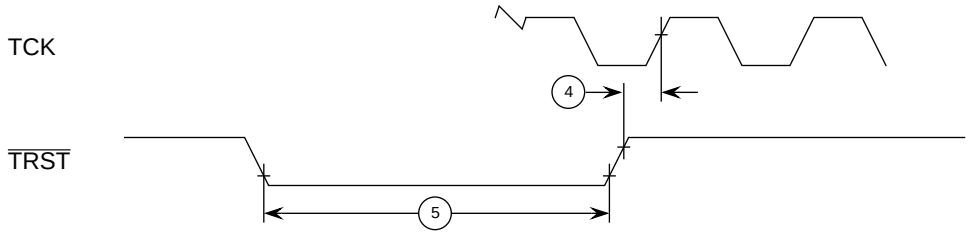


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

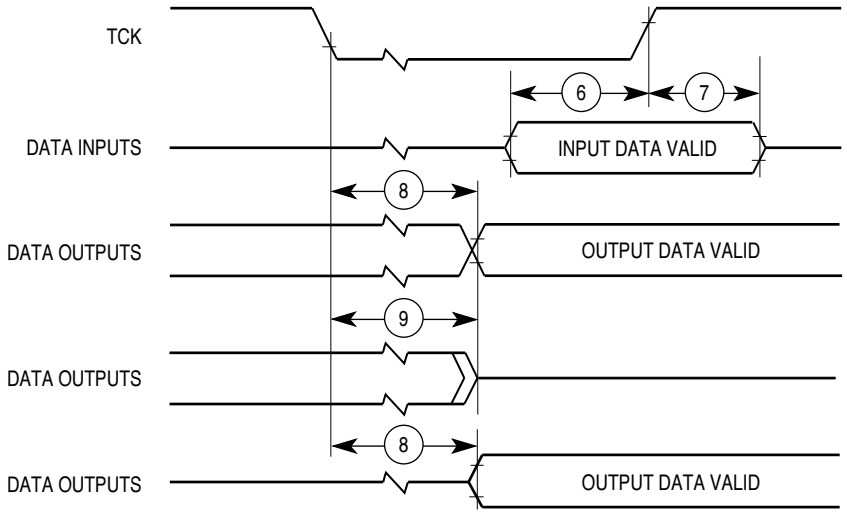


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

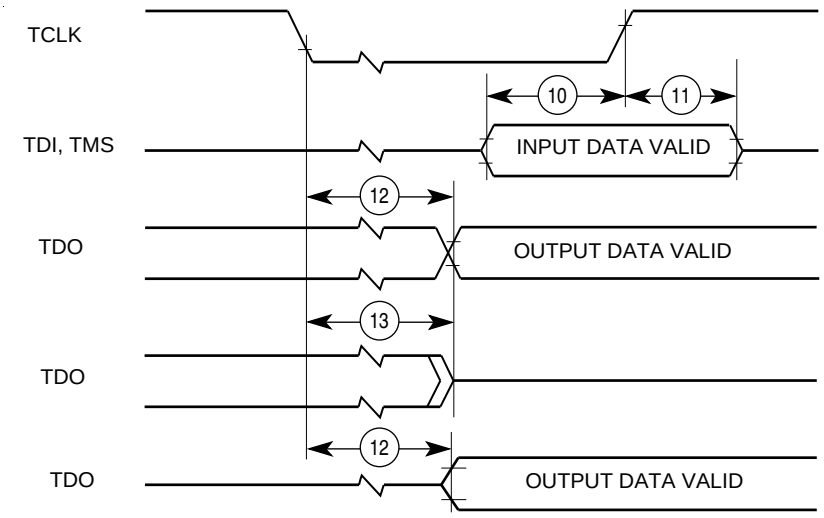


Figure 8. Test Access Port Timing Diagram

1.4 PowerPC 604 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the 604. Note that the 604 is currently offered in two packages. Motorola and IBM both offer a C4 Ceramic Quad Flat Pack (C4-CQFP), and a Ball Grid Array (BGA) package. Both IBM and Motorola C4-CQFP and BGA packages have identical pinouts.

1.4.1 Pinout Diagram for the C4-CQFP Package

Figure 9 contains the pinout diagram of the C4-CQFP package for the 604.

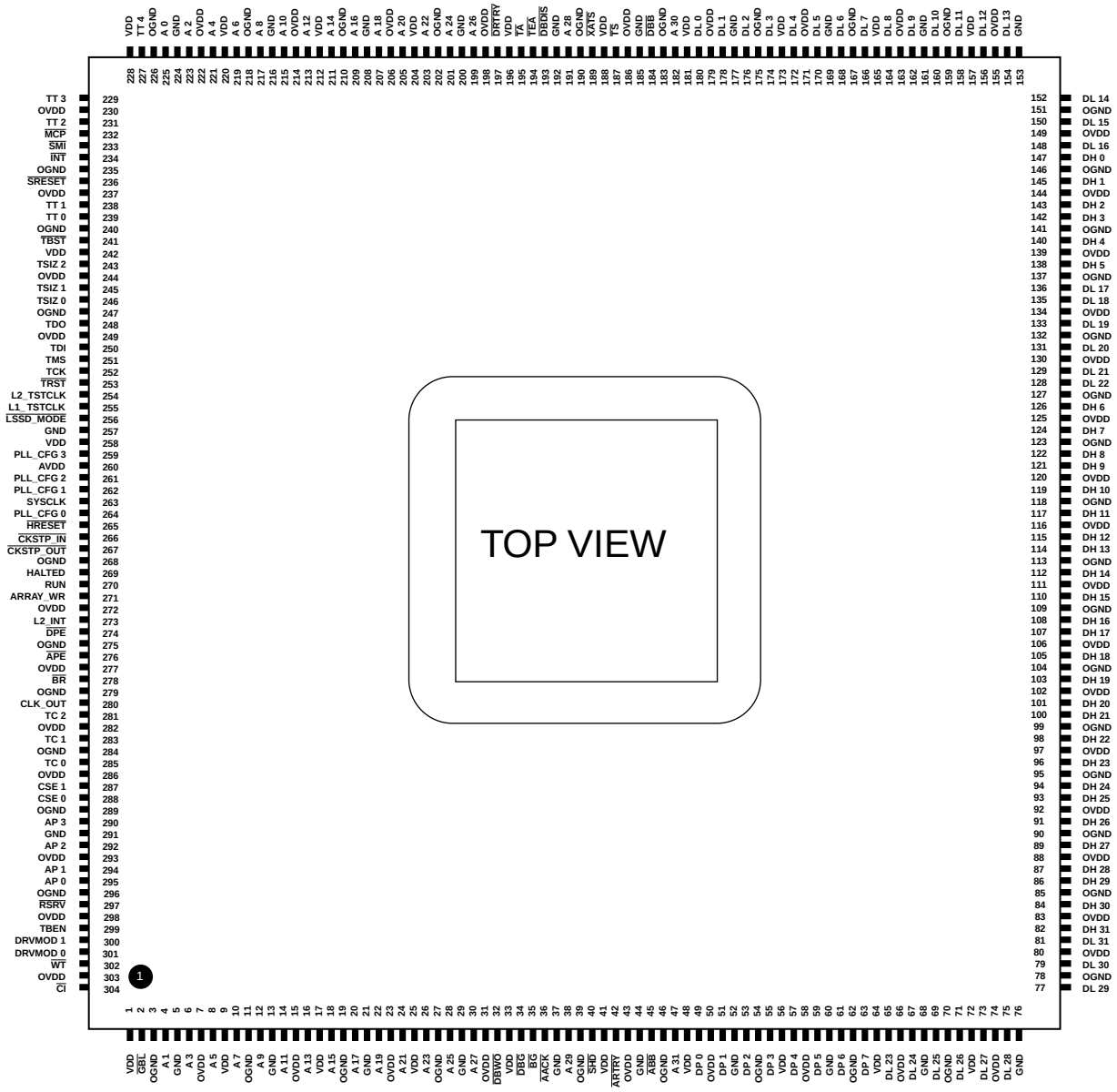
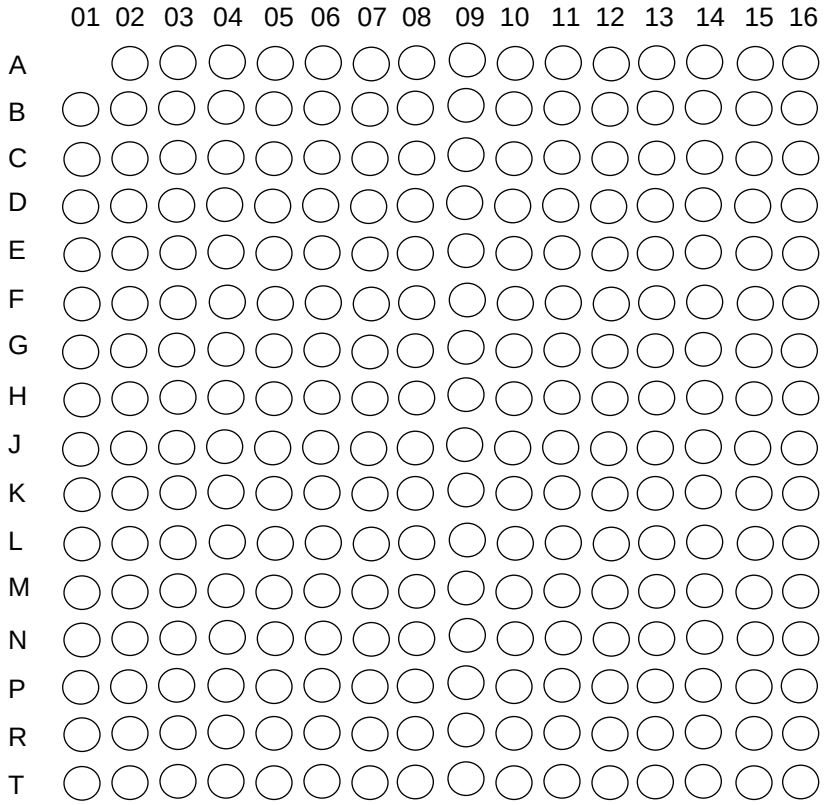


Figure 9. Pinout Diagram of the C4-CQFP Package

1.4.2 Pinout Diagram for the BGA Package

Figure 10 (in part A) shows the pinout of the BGA package as viewed from the top surface. Part B shows the side profile of the BGA package to indicate the direction of the top surface view.



Part B

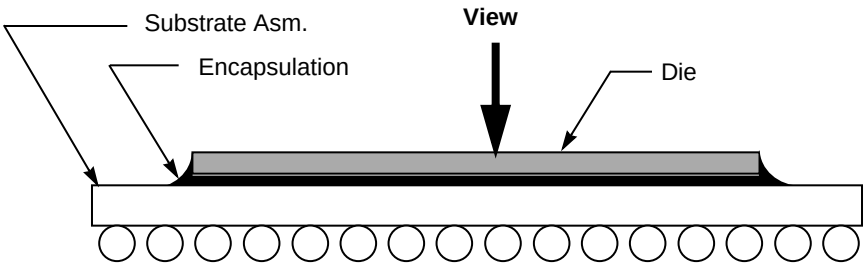


Figure 10. Pinout of the BGA Package as Viewed from the Top Surface

1.5 PowerPC 604 Microprocessor Pinout Listings

The following sections contain the pinout listings for the 604 C4-CQFP and BGA packages.

1.5.1 Pinout Listing for the C4-CQFP Package

Table 9 provides the pinout listing for the 604 C4-CQFP package.

Table 9. Pinout Listing for the C4-CQFP Package

Signal Name	Pin Number	Active	I/O
A0–A31	225, 4, 223, 6, 221, 8, 219, 10, 217, 12, 215, 14, 213, 16, 211, 18, 209, 20, 207, 22, 205, 24, 203, 26, 201, 28, 199, 30, 191, 38, 182, 47	High	I/O
$\overline{\text{AACK}}$	36	Low	Input
$\overline{\text{ABB}}$	45	Low	I/O
AP0–AP3	295, 294, 292, 290	High	I/O
$\overline{\text{APE}}$	276	Low	Output
ARRAY_WR[1]	271	Low	Input
$\overline{\text{ARTRY}}$	42	Low	I/O
AVDD	260	—	—
$\overline{\text{BG}}$	35	Low	Input
$\overline{\text{BR}}$	278	Low	Output
$\overline{\text{CI}}$	304	Low	Output
$\overline{\text{CKSTP\_IN}}$	266	Low	Input
$\overline{\text{CKSTP\_OUT}}$	267	Low	Output
CLK_OUT	280	—	Output
CSE0–CSE1	288, 287	High	Output
$\overline{\text{DBB}}$	184	Low	I/O
$\overline{\text{DBG}}$	34	Low	Input
$\overline{\text{DBDIS}}$	193	Low	Input
$\overline{\text{DBWO}}$	32	Low	Input
DH0–31	147, 145, 143, 142, 140, 138, 126, 124, 122, 121, 119, 117, 115, 114, 112, 110, 108, 107, 105, 103, 101, 100, 98, 96, 94, 93, 91, 89, 87, 86, 84, 82	High	I/O
DL0–DL31	180, 178, 176, 174, 172, 170, 168, 166, 164, 162, 160, 158, 156, 154, 152, 150, 148, 136, 135, 133, 131, 129, 128, 65, 67, 69, 71, 73, 75, 77, 79, 81	High	I/O
DP0–DP7	49, 51, 53, 55, 57, 59, 61, 63	High	I/O

Table 9. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	274	Low	Output
$\overline{\text{DRTRY}}$	197	Low	Input
DRVMOD0–DRVMOD1 [2]	301, 300	High	Input
$\overline{\text{GBL}}$	2	Low	I/O
GND	5, 13, 21, 29, 37, 44, 52, 60, 68, 76, 153, 161, 169, 177, 185, 192, 200, 208, 216, 224, 257, 291	—	—
HALTED	269	High	Output
$\overline{\text{HRESET}}$	265	Low	Input
$\overline{\text{INT}}$	234	Low	Input
L1_TSTCLK [1]	255	Low	Input
L2_INT	273	High	Input
L2_TSTCLK [1]	254	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	256	Low	Input
$\overline{\text{MCP}}$	232	Low	Input
OGND	3, 11, 19, 27, 39, 46, 54, 62, 70, 78, 85, 90, 95, 99, 104, 109, 113, 118, 123, 127, 132, 137, 141, 146, 151, 159, 167, 175, 183, 190, 202, 210, 218, 226, 235, 240, 247, 268, 275, 279, 284, 289, 296	—	—
OVDD [3]	7, 15, 23, 31, 43, 50, 58, 66, 74, 80, 83, 88, 92, 97, 102, 106, 111, 116, 120, 125, 130, 134, 139, 144, 149, 155, 163, 171, 179, 186, 198, 206, 214, 222, 230, 237, 244, 249, 272, 277, 282, 286, 293, 298, 303	—	—
PLL_CFG0–PLL_CFG3	264, 262, 261, 259	High	Input
$\overline{\text{RSRV}}$	297	Low	Output
RUN	270	High	Input
$\overline{\text{SHD}}$	40	Low	I/O
$\overline{\text{SMI}}$	233	Low	Input
$\overline{\text{SRESET}}$	236	Low	Input
SYSCLK	263	—	Input
$\overline{\text{TA}}$	195	Low	Input
TBEN	299	High	Input
$\overline{\text{TBST}}$	241	Low	I/O
TC0–TC2	285, 283, 281	High	Output

Table 9. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
TCK	252	High	Input
TDI	250	High	Input
TDO	248	High	Output
$\overline{\text{TEA}}$	194	Low	Input
TMS	251	High	Input
$\overline{\text{TRST}}$	253	Low	Input
$\overline{\text{TS}}$	187	Low	I/O
TSIZ0–TSIZ2	246, 245, 243	High	I/O
TT0–TT4	239, 238, 231, 229, 227	High	I/O
$\overline{\text{WT}}$	302	Low	Output
VDD [3]	1, 9, 17, 25, 33, 41, 48, 56, 64, 72, 157, 165, 173, 181, 188, 196, 204, 212, 220, 228, 242, 258	—	—
$\overline{\text{XATS}}$	189	Low	I/O

Notes:
1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance with these specifications.
3. In the Motorola 604 C4-CQFP package, there is no electrical distinction between the OVDD and the VDD pins. These signals are internally shorted together. The OVDD and VDD signals have been listed separately to maintain compatibility with future parts.

1.5.2 Pinout Listing for the BGA Package

Table 10 provides the pinout listing for the 604 BGA package.

Table 10. Pinout Listing for the BGA Package

Signal Name	Pin Number	Active	I/O
A0–A31	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP0–AP3	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
ARRAY_WR [1]	B07	Low	Input
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—

Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{BG}$	L01	Low	Input
$\overline{BR}$	B06	Low	Output
$\overline{CI}$	E01	Low	Output
$\overline{CKSTP\_IN}$	D08	Low	Input
$\overline{CKSTP\_OUT}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE0–CSE1	B01, B05	High	Output
$\overline{DBB}$	J14	Low	I/O
$\overline{DBG}$	N01	Low	Input
$\overline{DBDIS}$	H15	Low	Input
$\overline{DBWO}$	G04	Low	Input
DH0–31	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL0–DL31	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP0–DP7	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{DPE}$	A05	Low	Output
$\overline{DRTRY}$	G16	Low	Input
DRVMOD0–DRVMOD1 [2]	D05, C03	High	Input
$\overline{GBL}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
HALTED	B08	High	Output
$\overline{HRESET}$	A07	Low	Input
$\overline{INT}$	B15	Low	Input
L1_TSTCLK [1]	D11	Low	Input
L2_INT	D06	High	Input
L2_TSTCLK [1]	D12	Low	Input
$\overline{LSSD\_MODE}$ [1]	B10	Low	Input
$\overline{MCP}$	C13	Low	Input
OVDD [3]	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—

Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
PLL_CFG0–PLL_CFG3	A08, B09, A09, D09	High	Input
$\overline{\text{RSRV}}$	D01	Low	Output
RUN	C08	High	Input
$\overline{\text{SHD}}$	H04	Low	I/O
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC0–TC2	A02, A03, C06	High	Output
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ0–TSIZ2	A13, D10, B12	High	I/O
TT0–TT4	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD [3]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
$\overline{\text{XATS}}$	J16	Low	I/O

Notes:

1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance to these specifications.
3. In the 604 BGA package, there is no electrical distinction between the OVDD and the VDD pins. These signals are internally shorted together. The OVDD and VDD signals have been listed separately to maintain compatibility with future parts.

1.6 PowerPC 604 Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the 604.

1.6.1 C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the C4-CQFP package.

1.6.1.1 Motorola C4-CQFP Package Parameters

The package parameters for the Motorola C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
C4 encapsulation	Glass-filled Epoxy
Maximum module height	3.25 mm
Co-planarity specification	0.10 mm

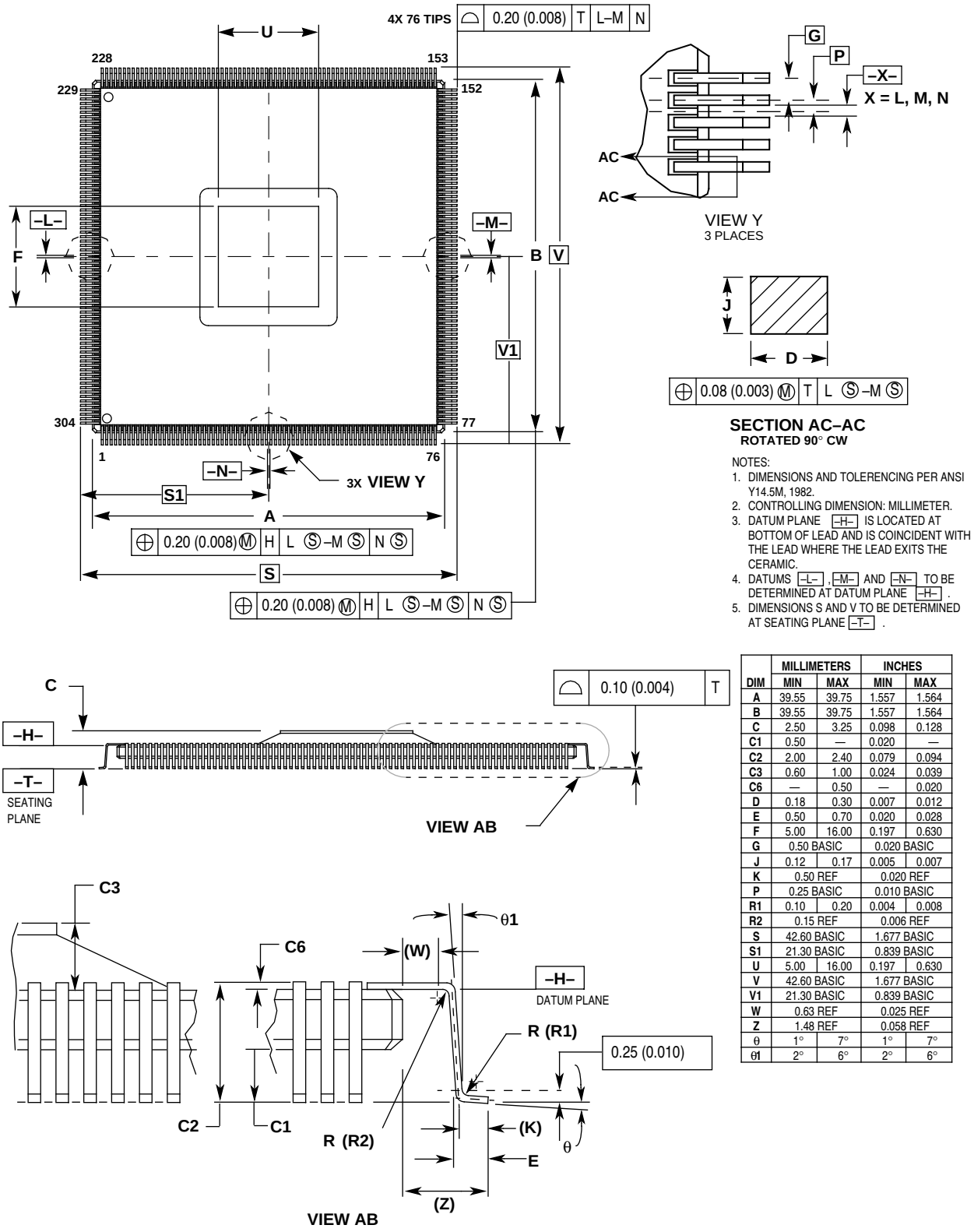
1.6.1.2 IBM C4-CQFP Package Parameters

The package parameters for the IBM C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
Lead encapsulation	Glass-filled Epoxy
C4 encapsulation	Glass-filled Epoxy
Maximum module height	2.92 mm
Co-planarity specification	0.08 mm

1.6.1.3 Mechanical Dimensions of the Motorola C4-CQFP Package

Figure 11 shows the mechanical dimensions of the Motorola C4-CQFP package.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.55	39.75	1.557	1.564
B	39.55	39.75	1.557	1.564
C	2.50	3.25	0.098	0.128
C1	0.50	—	0.020	—
C2	2.00	2.40	0.079	0.094
C3	0.60	1.00	0.024	0.039
C6	—	0.50	—	0.020
D	0.18	0.30	0.007	0.012
E	0.50	0.70	0.020	0.028
F	5.00	16.00	0.197	0.630
G	0.50 BASIC		0.020 BASIC	
J	0.12	0.17	0.005	0.007
K	0.50 REF		0.020 REF	
P	0.25 BASIC		0.010 BASIC	
R1	0.10	0.20	0.004	0.008
R2	0.15 REF		0.006 REF	
S	42.60 BASIC		1.677 BASIC	
S1	21.30 BASIC		0.839 BASIC	
U	5.00	16.00	0.197	0.630
V	42.60 BASIC		1.677 BASIC	
V1	21.30 BASIC		0.839 BASIC	
W	0.63 REF		0.025 REF	
Z	1.48 REF		0.058 REF	
θ	1°	7°	1°	7°
θ1	2°	6°	2°	6°

Figure 11. Mechanical Dimensions of the Motorola C4-CQFP Package

1.6.1.4 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 12 shows the mechanical dimensions for the IBM C4-CQFP package.

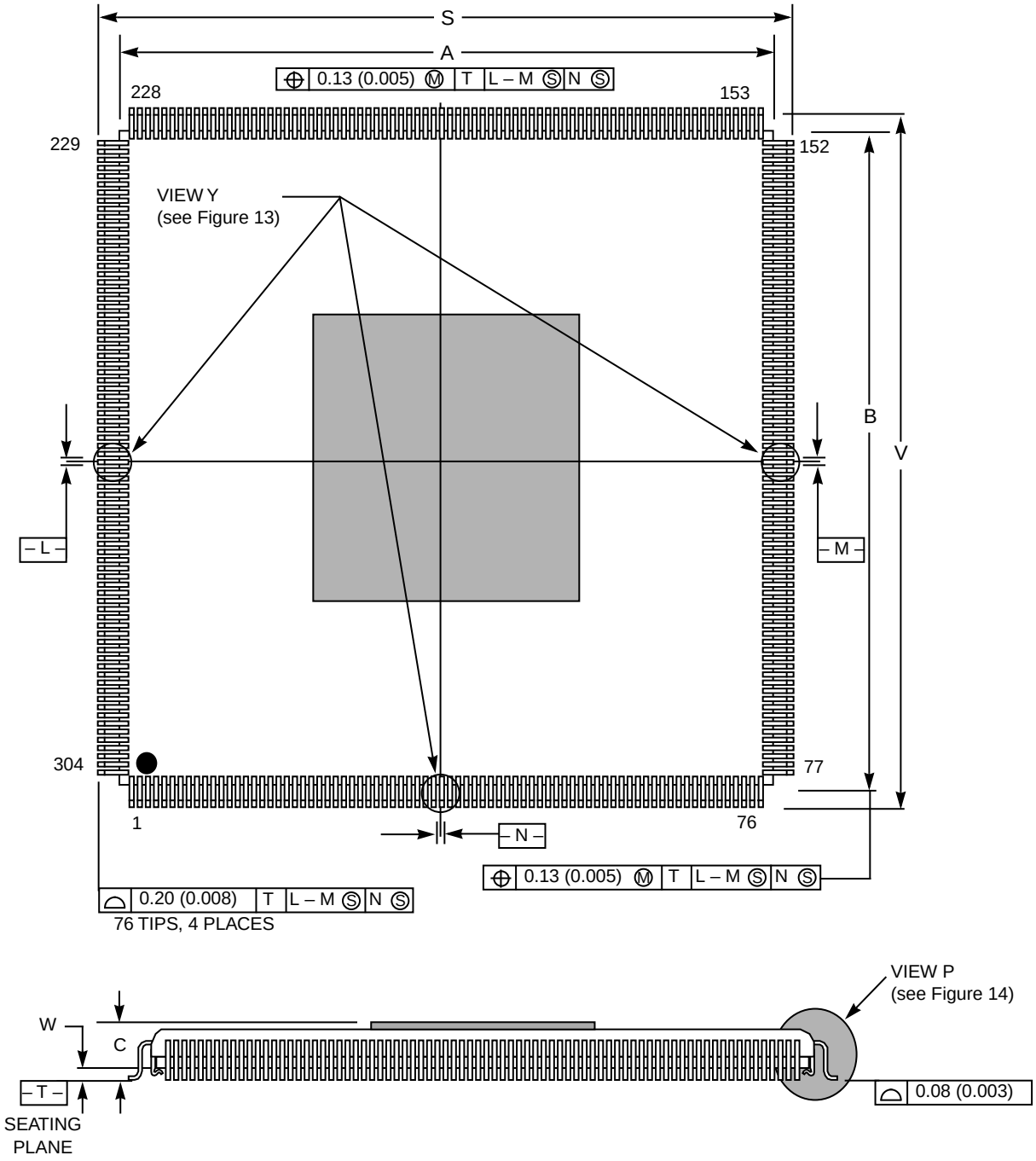


Figure 12. Mechanical Dimensions of the IBM C4-CQFP Package

Figure 13 and Figure 14 provide a more detailed representation of portions of IBM C4-CQFP package.

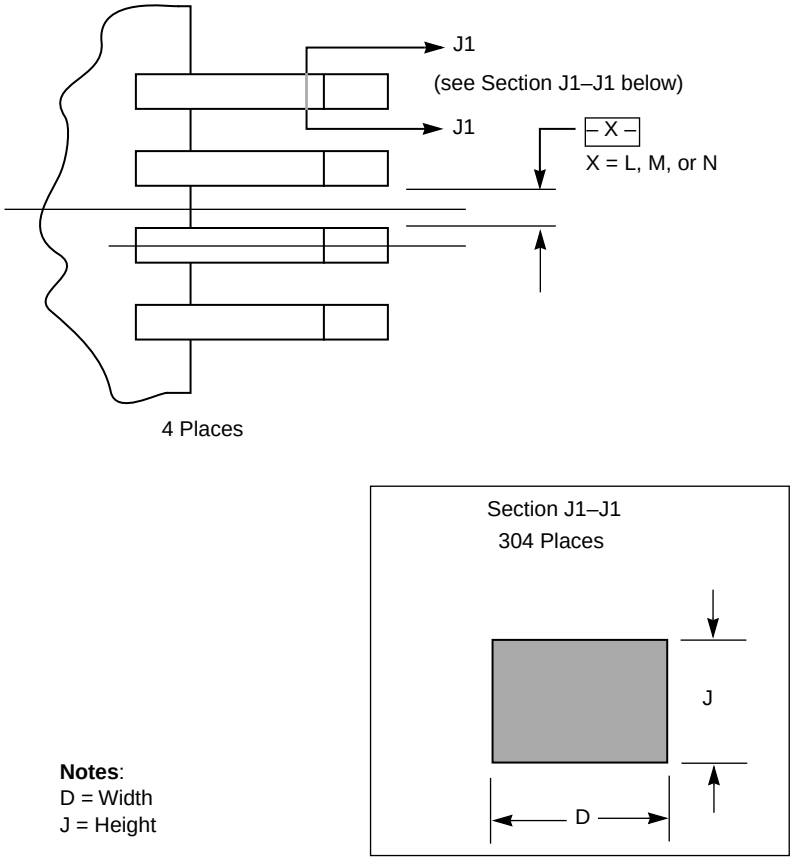


Figure 13. IBM C4-CQFP Mechanical Dimensions—View Y

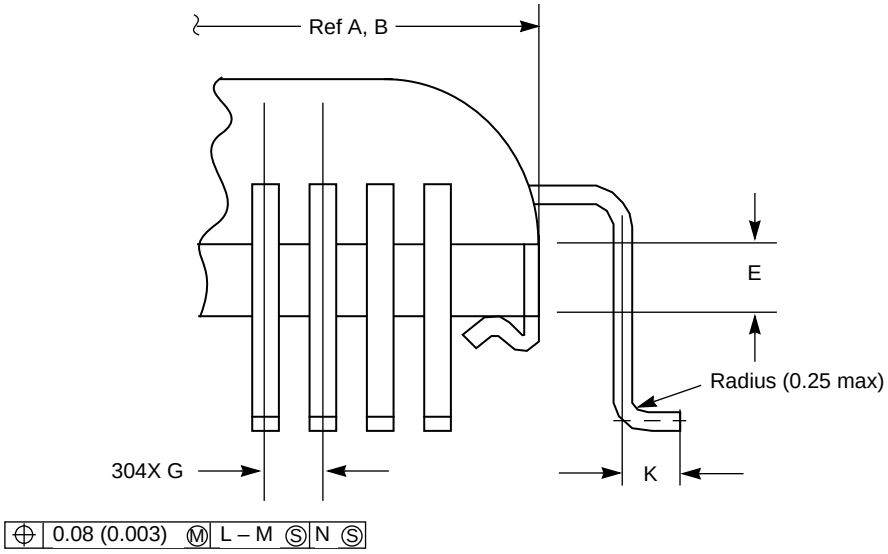


Figure 14. IBM C4-CQFP Mechanical Dimensions—View P

Table 11 lists the mechanical dimensions values for the IBM C4-CQFP package.

Table 11. Mechanical Dimensions Values

Dim	Millimeters	
	Min	Max
A	39.93	40.08
B	39.93	40.08
C	2.32	2.92
D	0.23	0.28
E	0.635 REF	
G	0.5 BSC	
J	0.12	0.20
K	0.40	0.60
S	42.4	42.8
V	42.4	42.8
W	0.35	—

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimension—millimeter.
3. Datums – L –, –M –, and – N – to be determined at seating plane.
4. Dimensions S and V to be determined at seating plane – T–.
5. Dimensions A and B to outside of lead clip.

1.6.2 BGA Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM and Motorola BGA packages.

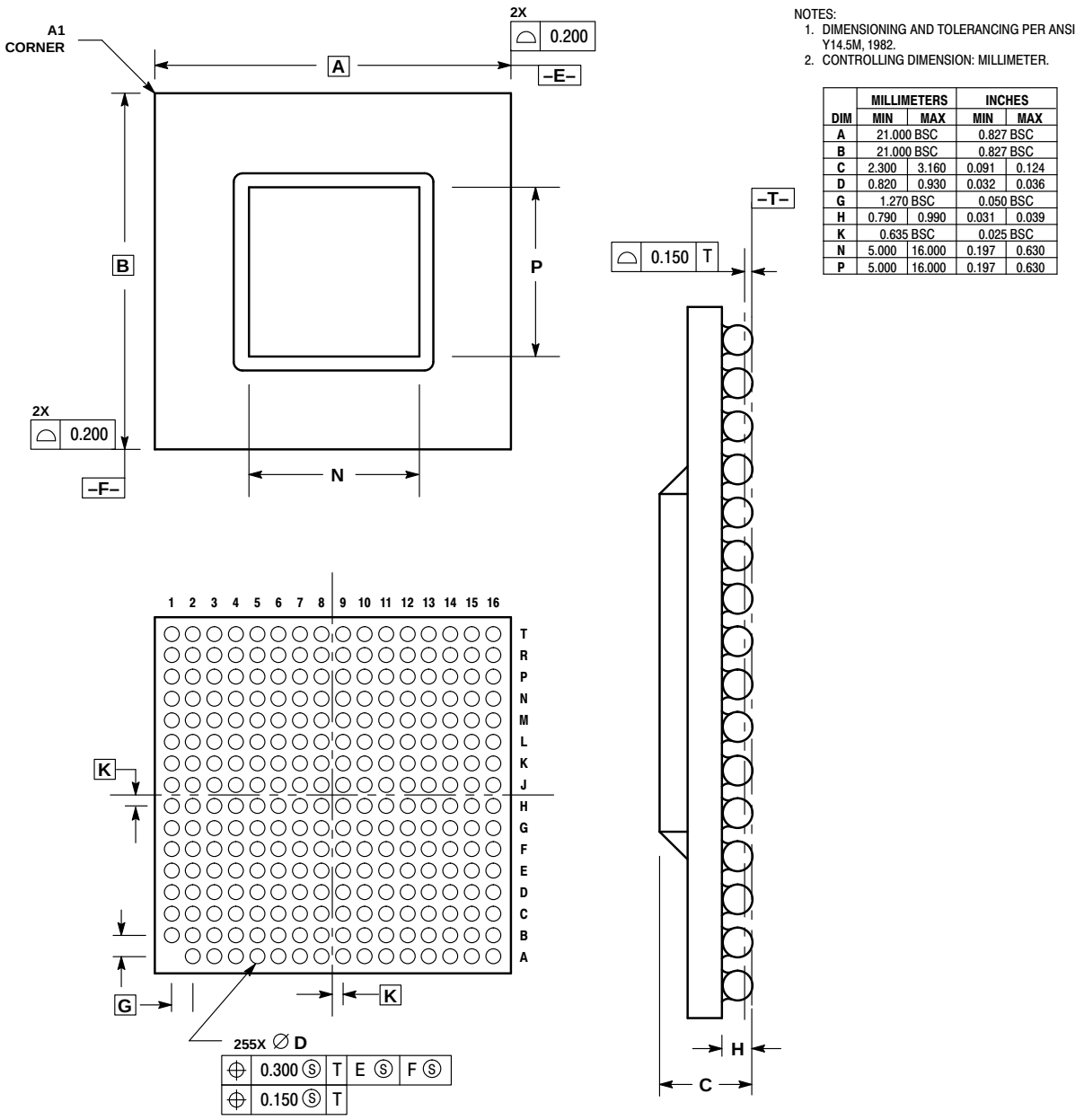
1.6.2.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 256-lead ceramic ball grid array (BGA).

Package outline	21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3.16 mm

1.6.2.2 Mechanical Dimensions of the BGA Package

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the IBM and Motorola BGA package.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.300	3.160	0.091	0.124
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature of the BGA Package

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 604.

1.7.1 PLL Configuration

The SYSCLK input determines the external bus frequency at which the 604 will operate. The internal PLL can be configured to provide an internal (processor core) frequency that is a multiple of the external bus clock frequency. The PLL is configured by the PLL_CFG0–PLL_CFG3 signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU frequency of operation as shown in Table 12.

Table 12. PLL Configuration

PLL_CFG0 to PLL_CFG3	Bus, CPU and VCO Frequencies								
	CPU/ SYSCLK Ratio	**Bus 16.6 MHz**	**Bus 20 MHz**	**Bus 25 MHz**	**Bus 33.3 MHz**	**Bus 40 MHz**	**Bus 50 MHz**	**Bus 60 MHz**	**Bus 66.6 MHz**
0001	1:1	—	—	—	—	—	50 (200)	60 (240)	66.6 (266)
0100	2:1	—	—	—	—	—	100 (200)	120 (240)	133 (266)
0101	2:1	—	—	50 (200)	66.6 (266)	80 (320)	—	—	—
1000	3:1	—	—	—	100 (200)	120 (240)	150 (300)	—	—
1001	3:1	50 (200)	60 (240)	75 (300)					
1100	1.5:1				—	—	—	90 (180)	100 (200)
1101	1:5:1				50 (200)	60 (240)	75 (300)	90 (360)	
0011	PLL Bypass								

Notes:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not useful, not supported, or not tested for by the 604. VCO frequencies (shown in parenthesis in Table 12) should not fall below 180 MHz, and should not exceed 360 MHz.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, and the bus is set for 1:1 mode operation. The PLL-bypass mode is for test purposes only, and is not intended for functional use.
3. PLL_CFG0–PLL_CFG1 select the CPU-to-bus ratio (1:1,1.5:1, 2:1, 3:1), PLL_CFG2–PLL_CFG3 select the CPU-to-PLL multiplier (x2, x4).

1.7.2 PLL Power Supply Filtering

The AVDD power signal is provided on the 604 to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVDD input signal should be filtered using a circuit similar to the one shown in Figure 16. Note that the capacitors should be placed as close as possible to the AVDD input signal.

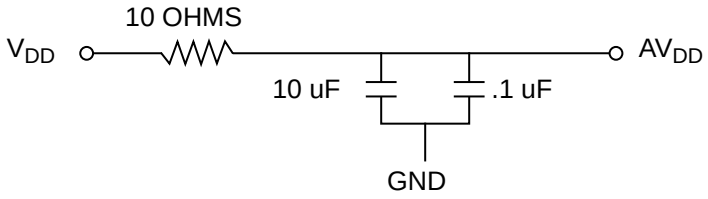


Figure 16. PLL Power Supply Filter Circuit

1.7.3 Decoupling Recommendations

The 604 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 604 system, and the 604 itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin of the 604.

These capacitors should range in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantalum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance in the traces. Power and ground connections must be made to all external Vdd and GND pins of the 604.

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) pins must remain unconnected.

1.8 Thermal Management Information

This section provides thermal management information for the C4-CQFP and the BGA packages. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, airflow and the thermal interface material. Heat sinks are typically attached to a chip package by means of a spring clip to holes in the printed-circuit board; see Figure 17.

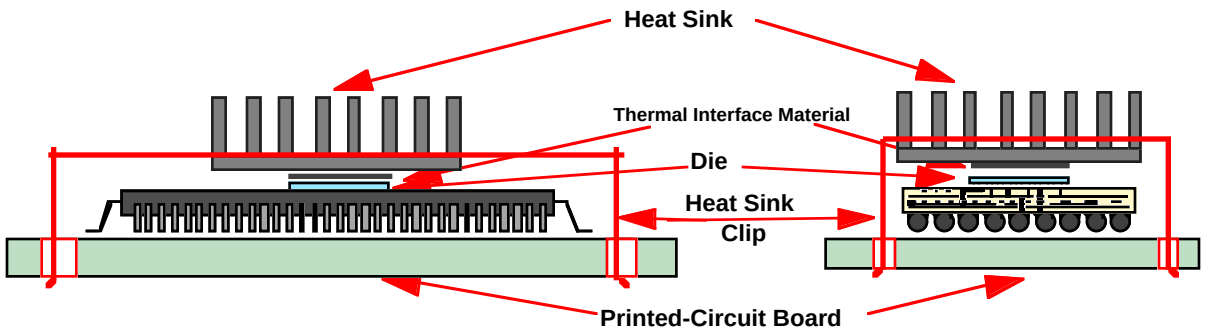


Figure 17. C4-CQFP and BGA Exploded Cross-Sectional View with Heat Sink

The board designer can choose between several types of heat sinks to place on the 604. There are several commercially-available heat sinks for the 604 provided by the following vendors:

Thermalloy
2021 W. Valley View Lane 214-243-4321
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation (IERC)
135 W. Magnolia Blvd.
Burbank, CA 91502 818-842-7277

Aavid Engineering 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Ultimately, the final selection of an appropriate heat sink for the 604 depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

These parameters are shown in Table 13.

Table 13. Package Thermal Resistance

Thermal Metric	C4-CQFP	BGA
Junction-to-case thermal resistance	0.03 °C/W	0.03 °C/W
Junction-to-lead (ball) thermal resistance	18.0 °C/W	2.2 °C/W

Figure 18 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

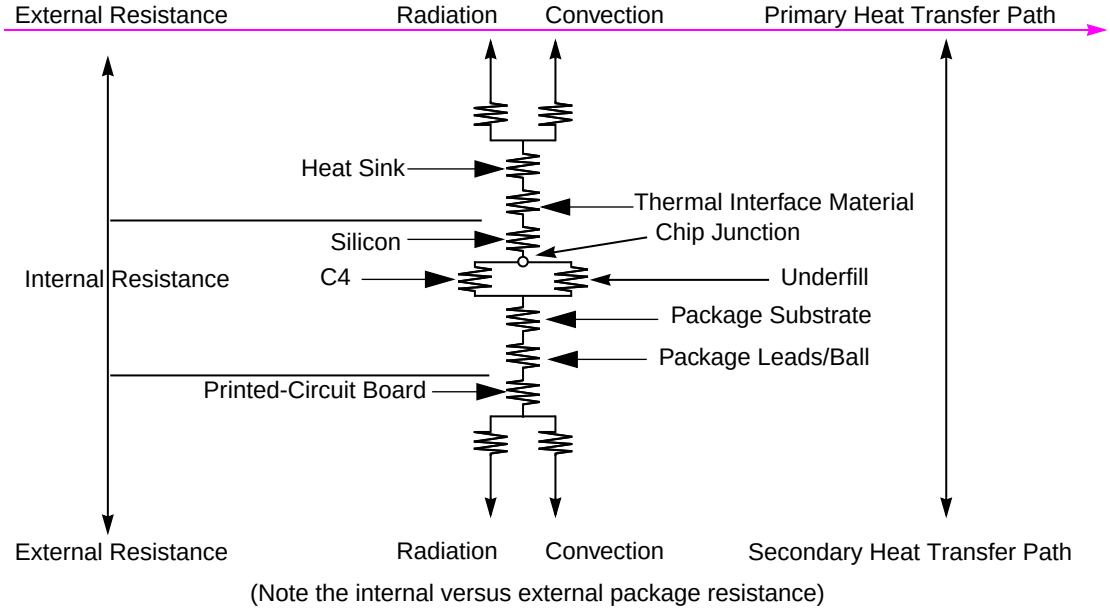


Figure 18. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms. The following section provides a thermal management example for the 604 using one of the commercially available heat-sinks.

1.8.2 Thermal Management Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (R_{\theta jc} + R_a + R_{sa}) * Q$$

Where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the system cabinet
$R_{\theta jc}$ is the die-junction-to-case (top of die) thermal resistance of the device
R_a is the thermal resistance of the thermal interface material (thermal grease or thermal compound)
R_{sa} is the heat sink-to-ambient thermal resistance
Q is the power dissipated by the device

Typical die-junction temperatures (T_j) should be maintained less than 105 °C. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. A computer cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The thermal resistance of the interface material (R_a) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, and a power dissipation (Q) of 18 watts, the following expression for T_j is obtained:

Junction temperature: $T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + R_{sa}) * 18\ W$

For a Thermalloy heat sink #2333B, the heatsink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 19.

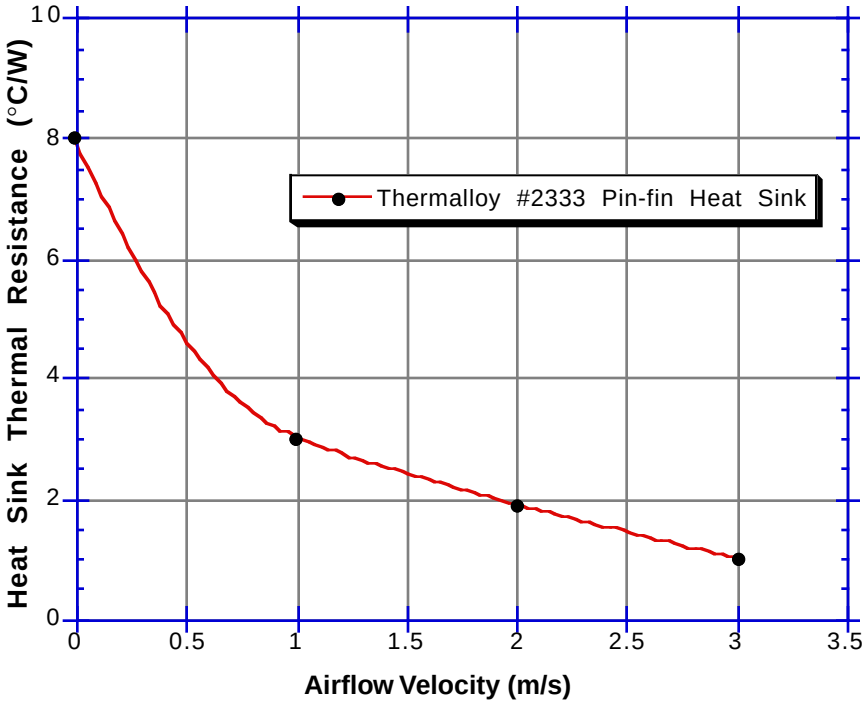


Figure 19. Thermalloy #2333B Pin-Fin Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Assuming an air velocity of 1 m/s, we have an effective R_{sa} of 3 °C/W, thus

$$T_j = 30°C + 5°C + (0.03\ °C/W + 1.0\ °C/W + 3\ °C/W) * 18\ W,$$

resulting in a junction temperature of approximately 107 °C which is more than the maximum operating temperature of the part. To ensure maximum reliability, it is desirable to operate the 604 well within its operating temperature range. Thus, to keep an 18-watts 604 within its proper operating range, an air velocity greater than 1 m/s should be used with the Thermalloy #2333B pin-fin heat sink.

Other heat sinks offered by Thermalloy, Aavid, Wakefield, and IERC offer different heat sink-to-ambient thermal resistances, and may or may not need air flow. It is necessary to perform an analysis as done above to select the desired heat sink.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs. To expedite system-level thermal analysis, several “compact” thermal-package models are available within FLOTHERM®. These are available upon request.

1.9 Ordering Information

This section provides the part numbering nomenclature for the 604. Note that the individual part numbers correspond to a specific combination of 604 internal/bus frequencies, which must be observed to ensure proper operation of the device. For available frequency combinations, contact your local Motorola or IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier allows for the availability of future enhanced parts (that is, lower voltage, lower power, higher performance, etc.).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

1.9.1 Motorola Part Number Key

Figure 20 provides the Motorola part numbering nomenclature for the 604.

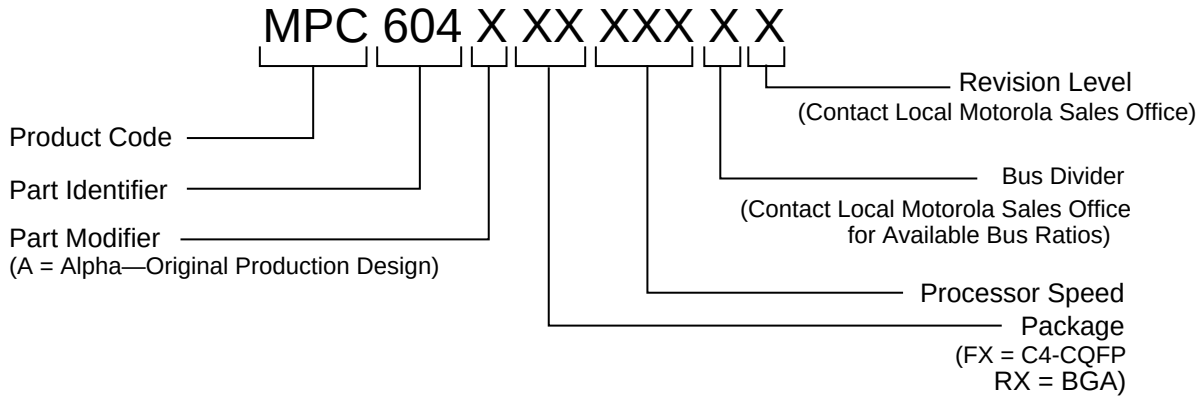


Figure 20. Motorola Part Number Key

1.9.2 IBM Part Number Key

Figure 21 provides the IBM part numbering nomenclature for the 604.

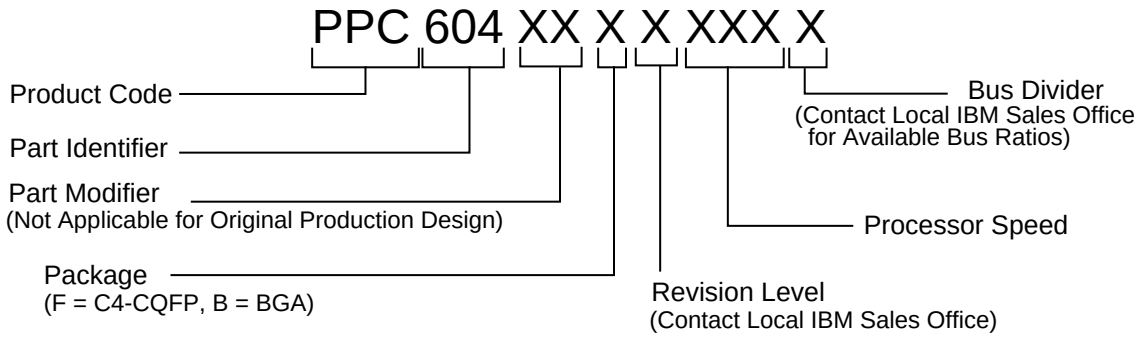


Figure 21. IBM Part Number Key

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