17. High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices

SGX52013-1.2

Introduction

Expansion in the telecommunications market and growth in Internet use requires systems to move more data faster than ever. To meet this demand, system designers rely on solutions such as differential signaling and emerging high-speed interface standards including RapidIO, POS-PHY 4, SFI-4, or XSBI.

These new protocols support differential data rates up to 1 gigabit per second (Gbps) and higher. At these high data rates, it becomes more challenging to manage the skew between the clock and data signals. One solution to this challenge is to use clock data recovery (CDR) to eliminate skew between data channels and clock signals. Another potential solution, dynamic phase alignment (DPA), is beginning to be incorporated by some of these protocols.

The Stratix® GX family of devices are the first FPGA devices to have an embedded dynamic phase aligner. This application note explains how to take advantage of the DPA feature in device high-speed I/O circuitry to increase system efficiencies and bandwidth. It will describe the skew issue in high-speed systems and provide a brief description of the source-synchronous circuitry in Stratix GX devices. The document will then describe an overview of the DPA block, I/O support with DPA, fast PLL support with DPA, a full description of DPA operation, and finally a comparison between CDR and source-synchronous interfaces.

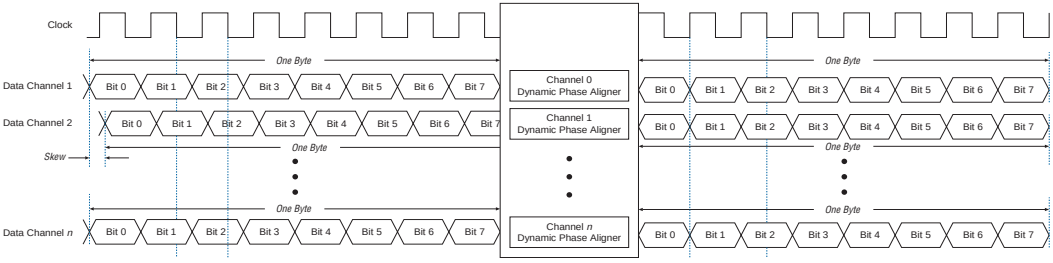
The source-synchronous high-speed interface in Stratix GX devices is a dedicated circuit embedded into the programmable logic device (PLD) allowing for high-speed communications. *AN 202: Using High-Speed Differential I/O Standards in Stratix Devices* provides information on Stratix GX device high-speed I/O standard features and functions.

Skew & Dynamic Phase Alignment

A typical problem designers face with high-speed source-synchronous systems is when clock or data signal transitions occur at different times with respect to each other (see Figure 17–1). When this happens, the receiver does not sample the data at the correct time, causing system errors. This problem is due to the inherent skew of the transmitter device, varying trace lengths and capacitive loading, variations in threshold voltages, transmission-line mis-terminations, or system reconfigurations. This results in inaccurate data transmission from one point to another and interrupted communication between components within the system.

A dynamic clock-data synchronization or phase alignment solution is optimal for high-speed systems because it provides a better tolerance to signal noise without the higher power consumption of devices which correct for skew using an individual analog PLL for each receiver channel. The dynamic phase aligner in Stratix GX devices shares the same components across many receiver channels, therefore reducing power consumption.

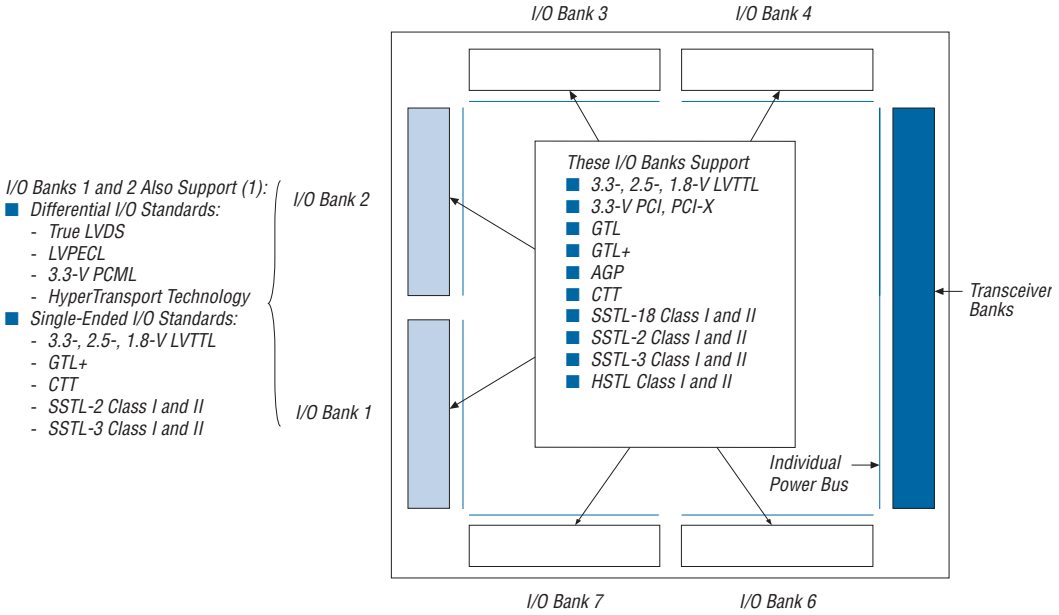
Figure 17–1. Clock to Data Skew



Stratix GX I/O Banks

Stratix GX devices contain seven I/O banks, as shown in Figure 17–2. I/O banks one and two support high-speed LVDS, LVPECL, 3.3-V PCML, HSTL class I and II, and SSTL-2 class I and II inputs and outputs. These two banks also incorporate an embedded dynamic phase aligner within the source-synchronous interface (see Figure 17–2). The dynamic phase aligner corrects for the phase difference between the clock and data lines caused by skew. The dynamic phase aligner operates automatically and continuously without requiring a fixed training pattern, and allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-clock skew.

Figure 17–2. DPA Support in Stratix GX Devices



Note to Figure 17–2:
(1) You can only use the differential receiver and clock input pins as inputs for single-ended standards.

Dedicated Source-Synchronous Circuitry

The differential I/O channels in Stratix GX I/O banks 1 and 2 can interface with LVDS, LVPECL, or 3.3-V PCML I/O standards in source-synchronous mode. Stratix GX devices transmit or receive serial channels along with clocks. The receiving Stratix GX device can multiply the low-speed clock by a factor of 1, 2, 4, 8, or 10 for serializer/deserializer (SERDES) operation. The SERDES factor (*J*) can be 4, 8, or 10 (only 8 or 10 with DPA) and determines the width of the bus driving into the logic array. The SERDES factor (*J*) does not have to equal the clock-multiplication value (*W*). The Stratix GX device can bypass the dedicated SERDES for a serialization or deserialization factor of 1 or 2. If the serialization/deserialization factor is 2, the I/O element (IOE) uses the

double data rate (DDR) input and output. Table 17–1 shows the clock multiplication factors and the SERDES factors supported by Stratix GX devices.

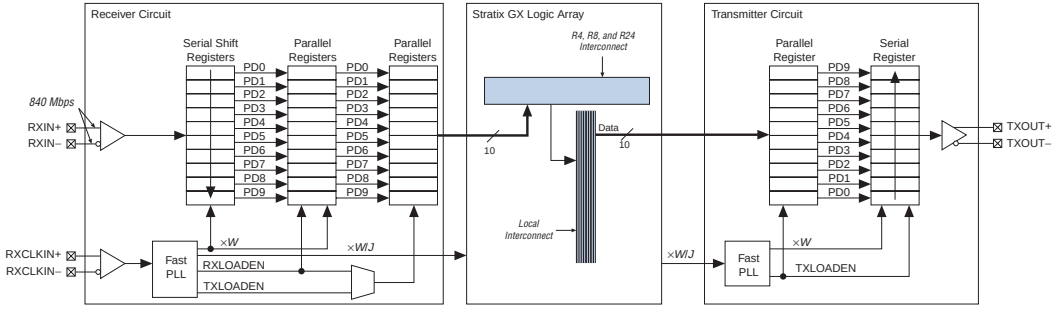
Table 17–1. Clock Multiplication Factors

Factor	Integer
Clock Multiplication *W*	1, 2, 4, 8, or 10
SERDES *J*	4, 8, or 10 *(1)*

Note to Table 17–1:
(1) The SERDES factor *J* can only be 8 or 10 when using DPA.

In the receiver circuitry, the fast PLL generates the high-frequency clock to deserialize the serial data through a shift register. The parallel data is synchronized with the low-frequency clock, and the receiver sends both to the logic array. On the transmitter side, the parallel data from the logic array is first fed into a parallel-in, serial-out shift register synchronized with the low-frequency clock and then transmitted out by the output buffers. Figure 17–3 shows the dedicated receiver and transmitter interface. For more information on the Stratix GX source-synchronous operation, refer to *AN 202: Using High-Speed Differential I/O Interfaces in Stratix Devices*.

Figure 17–3. Source-Synchronous Differential I/O Receiver/Transmitter Interface



The enable signal RXLOADEN loads the parallel data into the next parallel register on the second rising edge of the low-frequency clock in both modes (with or without DPA). Figure 17–4 shows the clock and data relationship in the receiver.

Figure 17–4. Receiver Timing Diagram

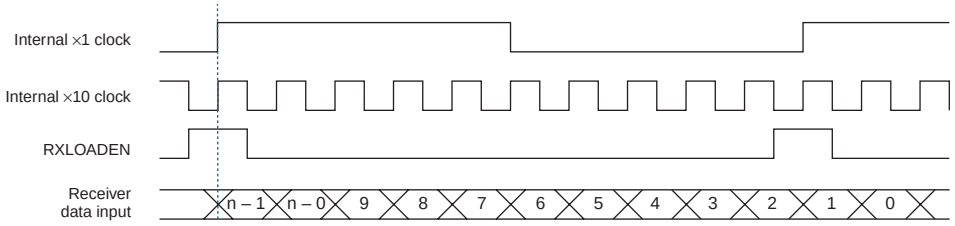
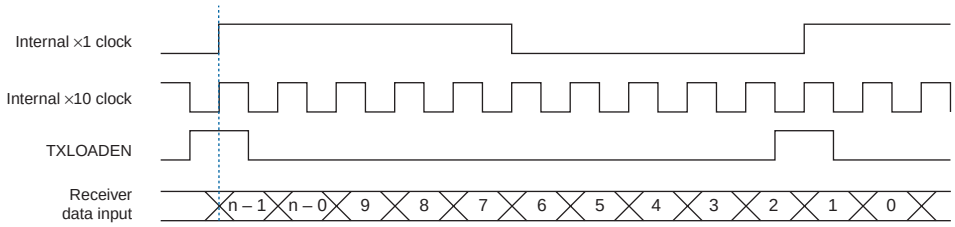


Figure 17–5 shows the timing relationship between the data and clock in the Stratix GX transmitter in ×10 mode.

Figure 17–5. Transmitter Timing Diagram

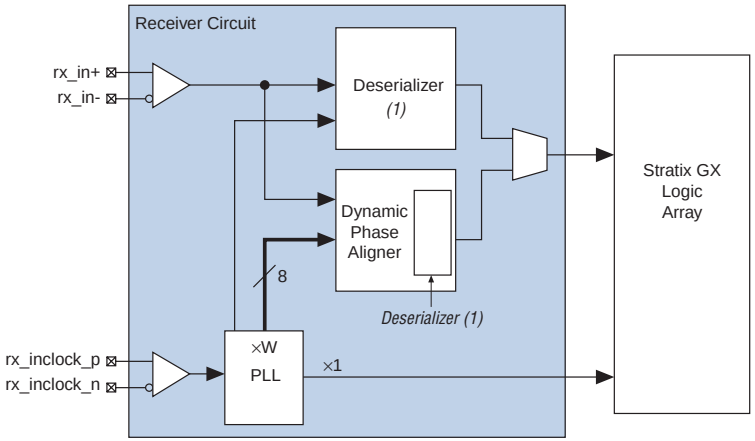


DPA Block Overview

Each Stratix GX receiver channel features a DPA block. The block contains a dynamic phase selector for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel by using a separate deserializer shown in Figure 17–6.

The dynamic phase aligner uses both the source clock and the serial data. The dynamic phase aligner automatically and continuously tracks fluctuations caused by system variations and self-adjusts to eliminate the phase skew between the multiplied clock and the serial data. Figure 17–6 shows the relationship between Stratix GX source-synchronous circuitry and the Stratix GX source-synchronous circuitry with DPA.

Figure 17–6. Source-Synchronous DPA Circuitry



Unlike the de-skew function in APEX™ 20KE and APEX 20KC devices or the clock-data synchronization (CDS) circuit in APEX II devices, you do not have to use a fixed training pattern with DPA in Stratix GX devices or assert a pin to activate the circuit.

DPA Input Support

Stratix GX device I/O banks 1 and 2 contain dedicated circuitry to support differential I/O standards at speeds up to 1 Gbps with DPA (or up to 840 Mbps without DPA). Stratix GX device source-synchronous circuitry supports LVDS, LVPECL, and 3.3-V PCML I/O standards. Additionally, the clock input pins in I/O banks 1 and 2 support differential HSTL. Table 17–2 shows the I/O standards that the dynamic phase aligner supports and their corresponding supply voltage. All Stratix GX device differential receiver input pins and clock pins in I/O banks 1 and 2 are dedicated input pins. Transmitter pins can be either input or output pins for both differential and single-ended I/O standards. Refer to Table 17–3.

Table 17–2. DPA Differential I/O Standards

I/O Standard	V_{CC} I/O (V)
LVDS, LVPECL, 3.3-V PCML	3.3

Table 17–3. Bank 1 & 2 Input Pins

Input Pin Type	I/O Standard	Receiver Pin	Transmitter Pin
Differential	Differential	Input only	Output only
Single ended	Single ended	Input only	Input or output

Interface & Fast PLL

This section describes the number of channels that support DPA and their relationship with the PLL in Stratix GX devices. EP1SGX10 and EP1SGX25 devices have two dedicated fast PLLs and EP1SGX40 devices have four dedicated fast PLLs for clock multiplication. Table 17–4 shows the maximum number of channels in each Stratix GX device that support DPA.

Table 17–4. Stratix GX Source-Synchronous Differential I/O Resources

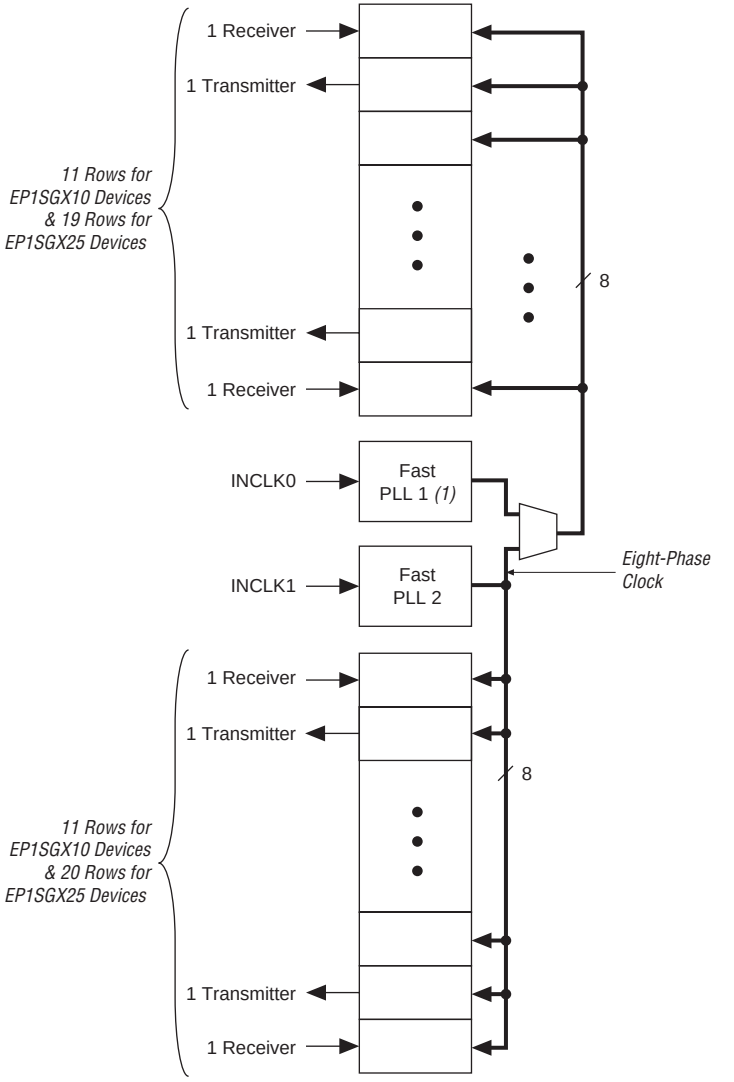
Device	Fast PLLs	Pin Count	Receiver Channels *(1)*	Transmitter Channels *(1)*	Receiver & Transmitter Channel Speed (Gbps) *(2)*	LEs
EP1SGX10C	2 *(3)*	672	22	22	1	10,570
EP1SGX10D	2 *(3)*	672	22	22	1	10,570
EP1SGX25C	2	672	39	39	1	25,660
EP1SGX25D	2	672	39	39	1	25,660
		1,020	39	39	1	25,660
EP1SGX25F	2	1,020	39	39	1	25,660
EP1SGX40D	4 *(4)*	1,020	45	45	1	41,250
EP1SGX40G	4 *(4)*	1,020	45	45	1	41,250

Notes to Table 17–4:

(1) This is the number of receiver or transmitter channels in the source-synchronous (I/O bank 1 and 2) interface of the device.
(2) Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps.
(3) One of the two fast PLLs in EP1SGX10C and EP1SGX10D devices supports DPA.
(4) Two of the four fast PLLs in EP1SGX40D and EP1SGX40G devices support DPA

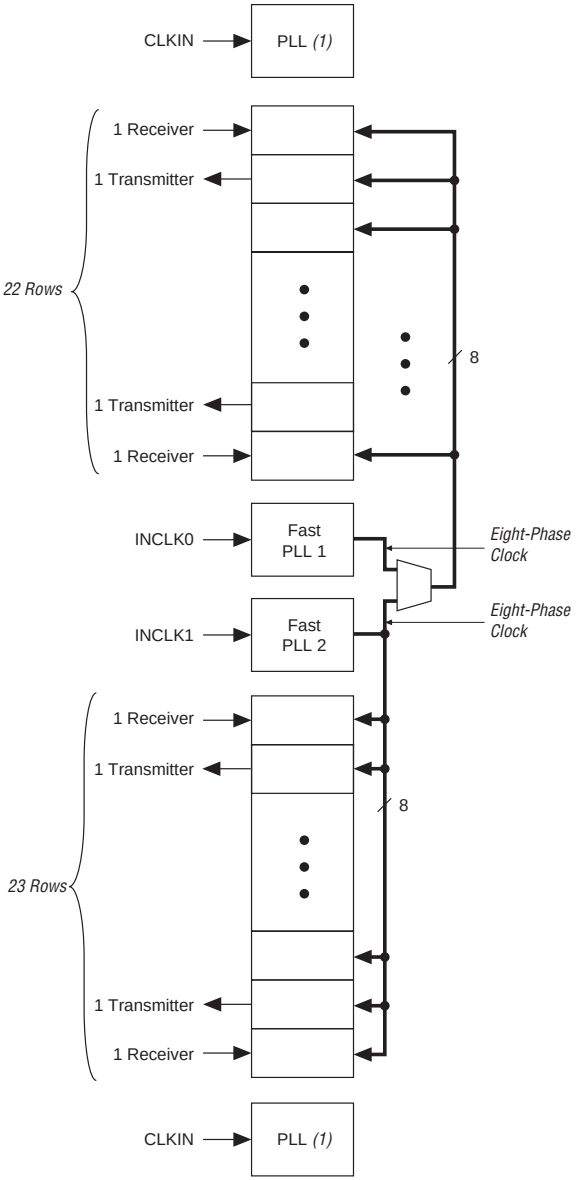
The receiver and transmitter channels are interleaved so that each I/O row in I/O banks 1 and 2 of the device has one receiver channel and one transmitter channel per row. Figures 17–7 and 17–8 show the fast PLL and channels with DPA layout in EP1SGX10, EP1SGX25, and EP1SGX40 devices. In EP1SGX10 devices, only fast PLL 2 supports DPA operations.

Figure 17–7. PLL & Channel Layout in EP1SGX10 & EP1SGX25 Devices



Note to Figure 17–7:
(1) Fast PLL 1 in EP1SGX10 devices does not support DPA.

Figure 17–8. PLL & Channel Layout in EP1SGX40 Devices *Notes (1), (2), (3)*



Notes to Figure 17–8:

(1) Corner PLLs do not support DPA.

(2) Not all eight phases are used by the receiver channel or transmitter channel in non-DPA mode.

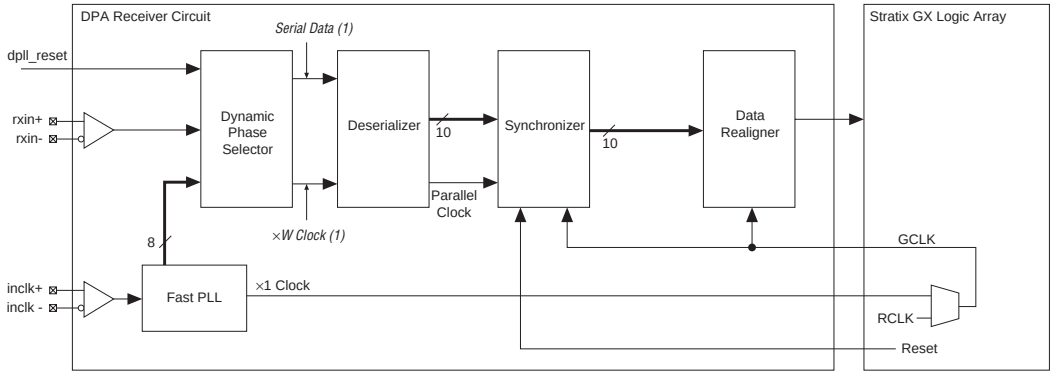
(3) The center PLLs can only clock 20 transceivers in either direction. Using Fast PLL2, you can clock a total of 40 transceivers, 20 in each direction.

DPA Operation

The DPA receiver circuitry contains the dynamic phase selector, the deserializer, the synchronizer, and the data realigner (see Figure 17–9). This section describes the DPA operation, synchronization and data realignment. You can enable or disable DPA operation on a channel-to-channel basis. In the SERDES with DPA mode, the source clock is fed to the fast PLL through the dedicated clock input pins. This clock is multiplied by the multiplication value *W* to match the serial data rate.

For information on the deserializer, see "Dedicated Source-Synchronous Circuitry" on page 17–3.

Figure 17–9. DPA Receiver Circuit

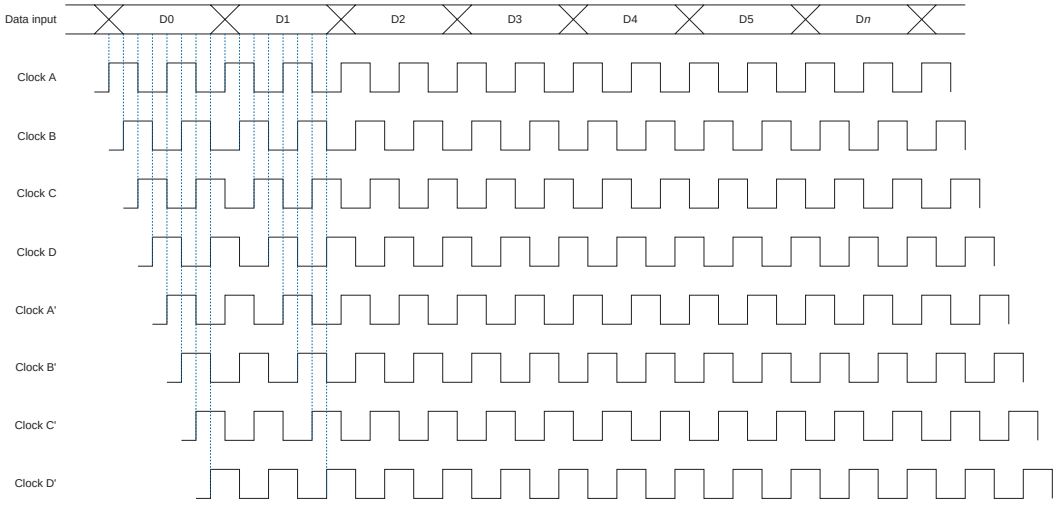


Note to Figure 17–9:
(1) These are phase-matched and retimed high-speed clocks and data.

The dynamic phase selector matches the phase of the high-speed clock and data before sending them to the deserializer.

The fast PLL supplies eight phases of the same clock (each a separate tap from a four-stage differential voltage-controlled oscillator (VCO)) to all the differential channels associated with the selected fast PLL. The DPA circuitry inside each channel locks to a phase closest to the serial data's phase and sends the retimed data and the selected clock to the deserializer. Each channel's DPA circuit can independently choose a different clock phase. The data phase detection and the clock phase selection process is automatic and continuous. The eight phases of clock gives the DPA circuit a granularity of one eighth of the unit interval (UI) or 125 ps at 1 Gbps. Figure 17–10 illustrates the clocks generated by the fast PLL circuitry and their relationship to a data stream.

Figure 17–10. Fast PLL Clocks & Data Input



Protocols, Training Pattern & DPA Lock Time

The dynamic phase aligner uses a fast PLL for clock multiplication, and the dynamic phase selector for the phase detection and alignment. The dynamic phase aligner uses the high-speed clock out of the dynamic phase selector to deserialize high-speed data and the receiver's source synchronous operations.

At each rising edge of the clock, the dynamic phase selector determines the phase difference between the clock and the data and automatically compensates for the phase difference between the data and clock.

The actual lock time for different data patterns varies depending on the data's transition density (how often the data switches between 1 and 0) and jitter characteristic. The DPA circuitry is designed to lock onto any data pattern with sufficient transition density, so the circuitry will work with current and future protocols. Experiments and simulations show that the DPA circuitry locks when the data patterns listed in Table 17–5 are repeated for the specified number of times. There are other suitable patterns not shown in Table 17–5 and/or pattern lengths, but the lock time may vary. The circuit can adjust for any phase variation that may occur during operation.

If the dynamic phase selector loses lock, the DPA circuitry sends a loss-of-lock signal for each channel to the logic array. You can then pull the dynamic phase selector RESET signal low to reset the dynamic phase selector. You can also reset the DPA operation by asserting the DPA RESET node.

Table 17–5. Training Patterns for Different Protocols

Protocols	Training Pattern	Number of Repetitions
SPI-4, NPSI	Ten 0's, ten 1's (0000000000111111111)	256
RapidIO	Four 0's, four 1's (00001111) or one 1, two 0's, one 1, four 0's (10010000)	
Other designs	Eight alternating 1's and 0's (10101010 or 01010101)	
SFI-4, XSBI	Not specified	

Phase Synchronizer

Each receiver has its own dynamic phase synchronizer. The receiver dynamic phase synchronizer aligns the phase of the parallel data from all the receivers to one global clock. The synchronizers in each channel consist of a first-in first-out (FIFO) buffer clocked by the global clock (GCLK) and parallel clock. The global clock (GCLK) and parallel clock input into the synchronizers must have identical frequency and differ only in phase. Therefore, the operation does not require an empty/full flag or read/write enable signals. The dynamic phase selector aligns each data signal with one of the eight phases of the global clock, so each signal has the same frequencies. Each synchronizer is written with a different clock phase, depending on the phase of the received data. The global clock reads all synchronizers, so all data is the same phase for use in the logic array.

Receiver Data Realignment In DPA Mode

While DPA operation aligns the incoming clock phase to the incoming data phase, it does not guarantee the parallelization boundary or byte boundary. When the dynamic phase aligner realigns the data bits, the bits may be shifted out of byte alignment, as shown in Figure 17–11.

Figure 17–11. Misaligned Captured Bit

The dynamic phase selector and synchronizer align the clock and data based on the power-up of both communicating devices, and the channel to channel skew. However, the dynamic phase selector and synchronizer cannot determine the byte boundary, and the data may need to be byte-aligned. The dynamic phase aligner's data realignment circuitry shifts data bits to correct bit misalignments.

The Stratix GX circuitry contains a data-realignment feature controlled by the logic array. Stratix GX devices perform data realignment on the parallel data after the deserialization block. The data realignment can be performed per channel for more flexibility. The data alignment operation requires a state machine to recognize a specific pattern. The procedure requires the bits to be slipped on the data stream to correctly align the incoming data to the start of the byte boundary.

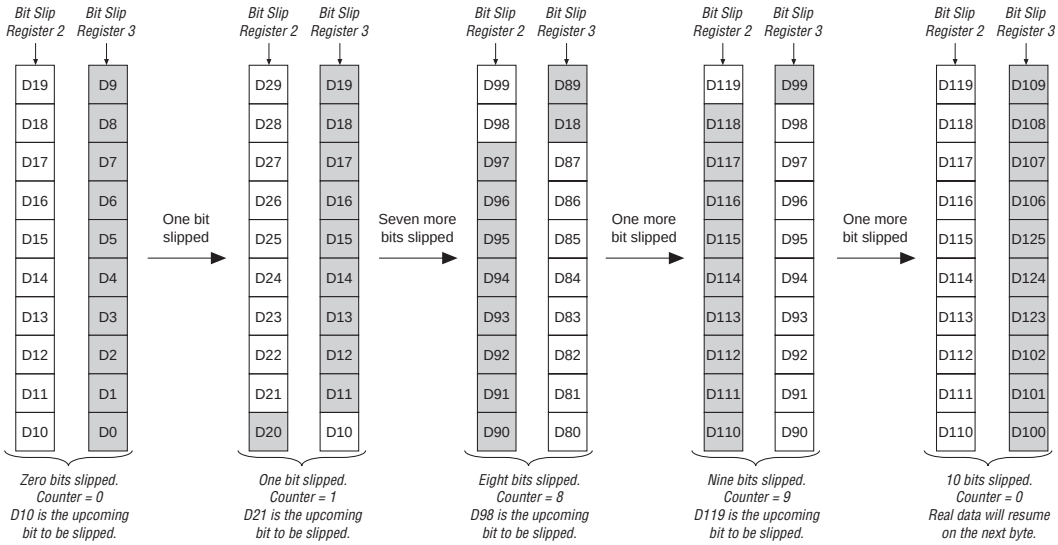
The DPA uses its realignment circuitry and the global clock for data realignment. Either a device pin or the logic array asserts the internal `rx_channel_data_align` node to activate the DPA data-realignment circuitry. Switching this node from low to high activates the realignment circuitry and the data being transferred to the logic array is shifted by one bit.

A state machine and additional logic can monitor the incoming parallel data and compare it against a known pattern. If the incoming data pattern does not match the known pattern, you can activate the `rx_channel_data_align` node again. Repeat this process until the realigner detects the desired match between the known data pattern and incoming parallel data pattern.

The DPA data-realignment circuitry allows further realignment beyond what the *J* multiplication factor allows. You can set the *J* multiplication factor to be 8 or 10. However, since data must be continuously clocked in on each low-speed clock cycle, the upcoming bit to be realigned and previous *n* –1 bits of data will be selected each time the data realignment logic's counter passes *n* –1. At this point the data is selected entirely from bit-slip register 3 (see Figure 17–12) as the counter is reset to 0. The logic

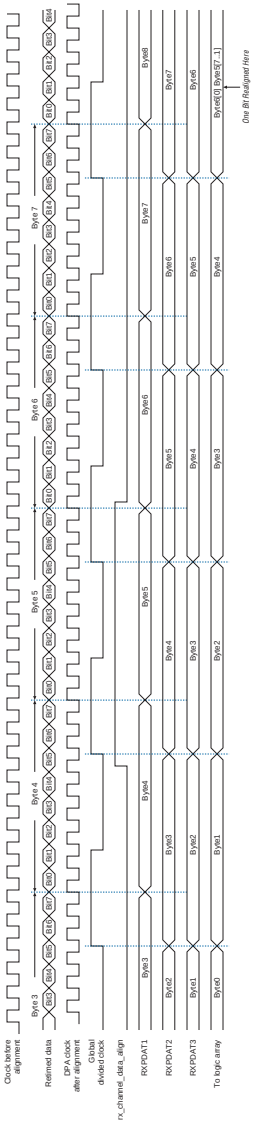
array receives a new valid byte of data on the next divided low-speed clock cycle. Figure 17–12 shows the data realignment logic output selection from data in the data realignment register 2 and data realignment register 3 based on its current counter value upon continuous request of data slipping from the logic array.

Figure 17–12. DPA Data Realigner



Use the rx_channel_data_align signal within the device to activate the data realigner. You can use internal logic or an external pin to control the rx_channel_data_align signal. To ensure the rising edge of the rx_channel_data_align signal is latched into the control logic, the rx_channel_data_align signal should stay high for at least two low-frequency clock cycles. Figure 17–13 shows the timing diagram of the DPA circuit. The byte boundary of the data is shifted by one bit on each rising-edge of the rx_channel_data_align signal. Thus one bit will be lost every time the data is slipped.

Figure 17–13. Data Realignment to Clock Timing Relationship



In order to manage the alignment procedure, a state machine should be built in the FPGA logic array to generate the realignment signal. The following guidelines outline the requirements for this state machine.

- The design must include an input synchronizing register to ensure that data is synchronized to the ×*W*/*J* clock.
- After the state machine, use another synchronizing register to capture the generated `rx_channel_data_align` signal and synchronize it to the ×*W*/*J* clock.
- The skew in the path from the output of this synchronizing register to the PLL is undefined, so the state machine must generate a pulse that is high for two ×*W*/*J* clock periods.
- The `rx_channel_data_align` generator circuitry only generates a single fast clock period pulse for each `rx_channel_data_align` pulse, so you cannot generate additional `rx_channel_data_align` pulses until the signal comparing the incoming data to the alignment pattern is reset low.
- To guarantee the state machine does not incorrectly generate multiple `rx_channel_data_align` pulses to shift a single bit, the state machine must hold the `rx_channel_data_align` signal low for at least three ×1 clock periods between pulses.

Source-Synchronous Circuitry with DPA vs. CDR

The DPA feature and source-synchronous channels are complementary features within Stratix GX devices to be used with high-speed transceiver blocks. The channels on the transceiver side of the device use an embedded circuit dedicated for receiving and transmitting serial data streams to and from the system board at frequencies up to 3.125 Gbps. These channels are clustered in serial transceiver blocks that contain four channels each and handle complex encoding and decoding schemes. If your system requires more than twenty channels, but your data rate is between 0.622 and 1.0 Gbps and you don't require the complex coding or decoding schemes, you can use the channels in banks 1 and 2 to implement the source-synchronous channels with DPA.

Software Support

You can configure the Stratix GX LVDS transmitter and receiver blocks using the MegaWizard® Plug-In Manager in the Quartus® II software. The wizard is a GUI-based ports and parameter selector for the `altlvds` megafunction. This section describes the available options for the Stratix GX LVDS transmitter and receiver.

Figure 17–14 shows the first page of the MegaWizard Plug-In Manager. With this page you can create a new megafunction, edit an existing megafunction, or copy an existing megafunction to create a variant. This section describes how to create a new megafunction.

Figure 17–14. MegaWizard Plug-In Manager (Page 1)

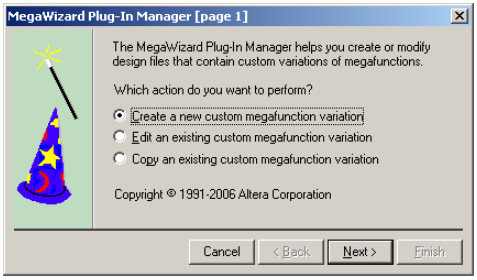
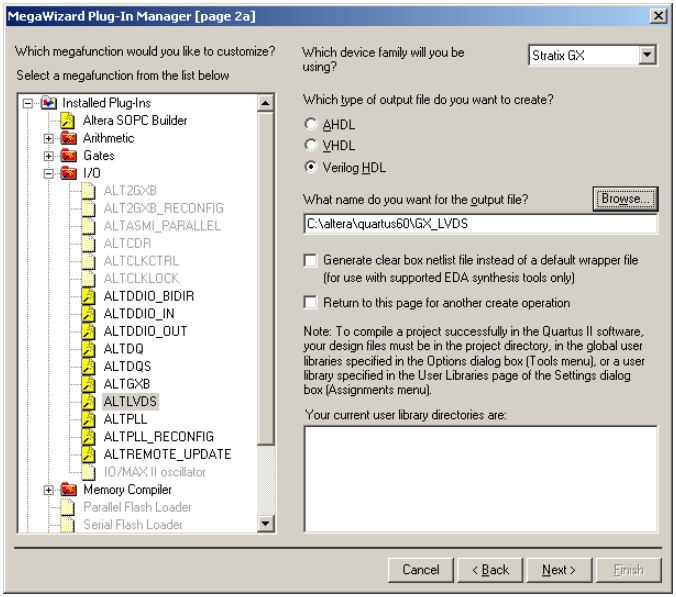


Figure 17–15 allows you to choose the megafunction to configure and the device family. You can also choose the HDL language you want the output file to be compatible with. For schematic entry, any HDL can be selected. You must provide a base name for the output files. Figure 17–15 shows the second page of the wizard.

Figure 17–15. MegaWizard Plug-In Manager (Page 2a)



Stratix GX Transmitter

Stratix GX transmitter setup starts on the page shown in Figure 17–16.

On this page, you select which device the megafunction is for in **Use which device family?** This selection activates available options for each device family. For example, for Stratix GX devices, the DPA option is available, but the Use External PLL option is not.

You can also set the number of channels and the deserialization factor. The deserialization factor determines the parallel clock frequency and the word width in the PLD logic array.

Figure 17–16. MegaWizard Plug-In Manager - altlvds Transmitter

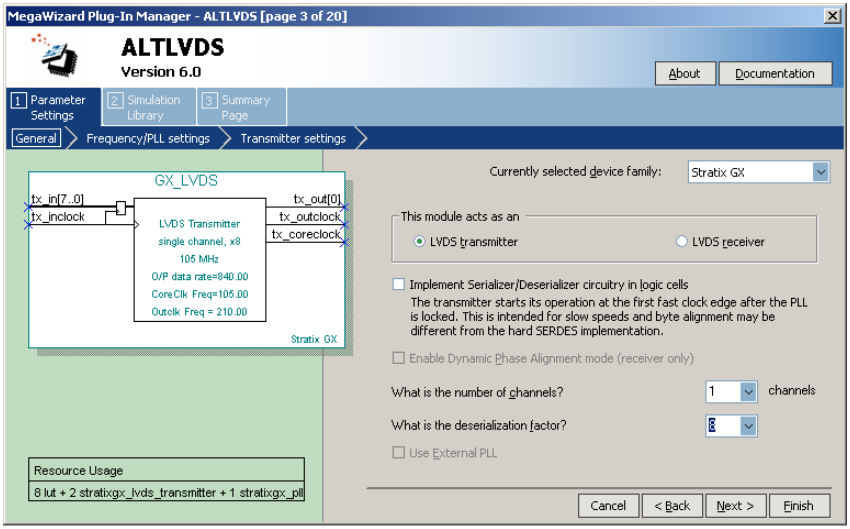


Figure 17–17 shows the `altlvds` MegaWizard Plug-In Manager page where you select the data rate and the transmitter clocking. The maximum input clock frequency is 717 MHz.

You can adjust the phase relation of the incoming data and reference clock in the **What is the phase alignment of data with respect to the rising edge of tx_inclock? (in degrees)** option.

You can enable the `tx_pll_enable` and `pll_areaset` ports. The `tx_pll_enable` port disables or enables the fast PLL used for the current instance. The `pll_areset` port resets all the counters to the fast PLL.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the correct conditions (the same data rate, SERDES factor, and input clock frequency).

Use the **Register `tx_in` input port using** option as necessary to transfer data from the PLD to the transmitter. Turn off this option if the design already contains a layer of registers before the PLD to transmitter interface. The clock feeding the register is fed by `tx_inclock` or `tx_coreclock`, depending on what feeds the data path in the PLD logic array.

Figure 17–17. MegaWizard Plug-In Manager - altlvds Transmitter

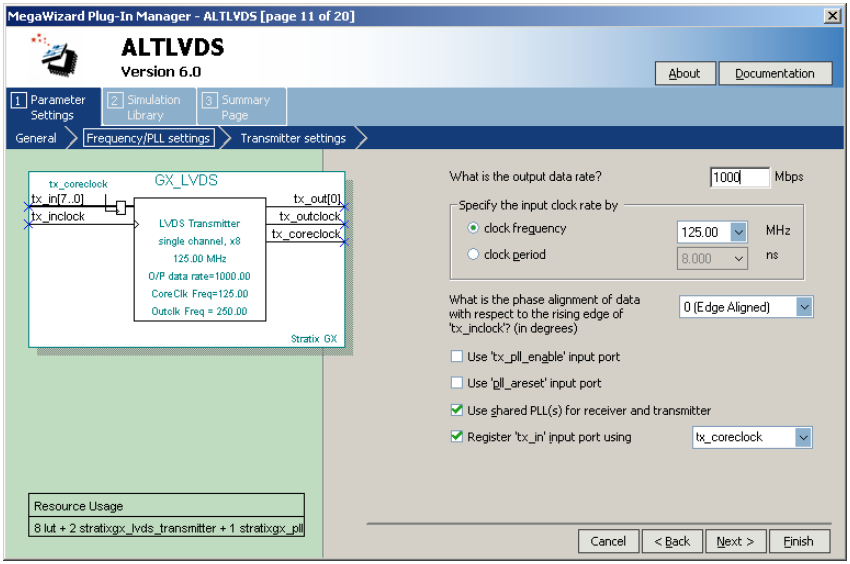
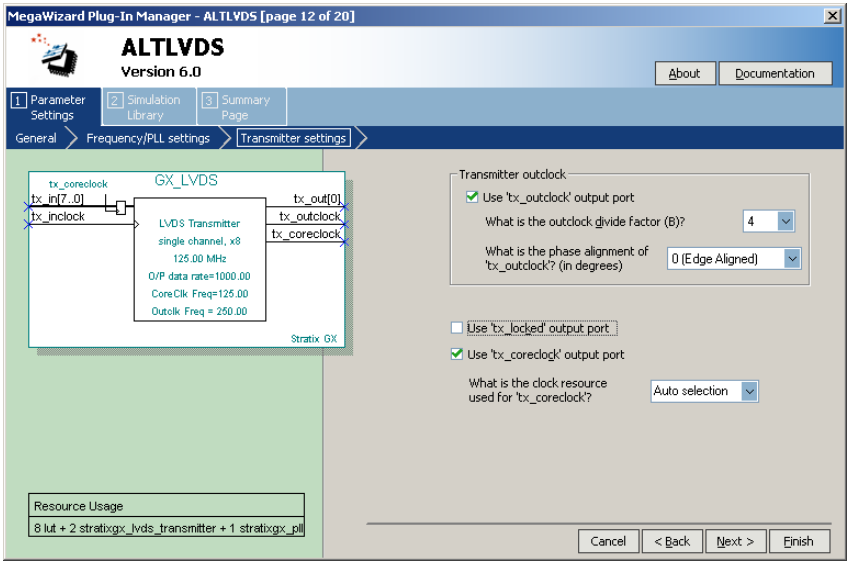


Figure 17–18 shows the last transmitter options page of the wizard. On this page you can enable the `tx_locked` and `tx_coreclock` ports. The `tx_locked` port indicates if the fast PLL is locked to the reference clock. The `tx_coreclock` port supplies the PLD with a clock, and is useful when the frequency of `tx_inclock` does not match the data rate divided by the SERDES factor.

You can set `tx_coreclock` to use a specific clock resource or, if you choose Auto selection, the Quartus II software automatically allocates an available clock resource. You set up the division factor and phase of the output clock independently of the input clock.

Figure 17–18. MegaWizard Plug-In Manager - altlvds Transmitter



Stratix GX Receiver Without DPA

Stratix GX receiver setup without DPA starts on the page shown in Figure 17–19. The number of channels and deserialization factor are similar to those of the transmitter. The DPA option is available for the Stratix GX family. In Figure 17–19, DPA mode is not selected.

Figure 17–19. MegaWizard Plug-In Manager - altlvds Receiver Without DPA

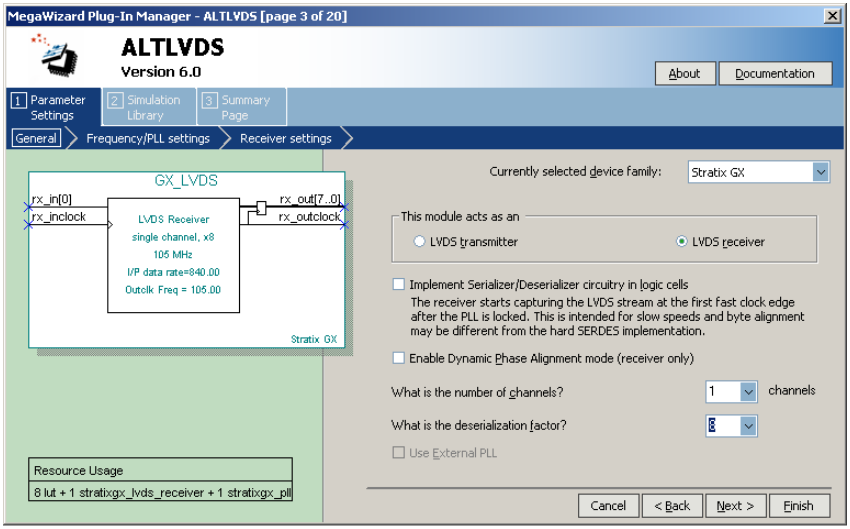


Figure 17–20 shows the page of the wizard where you can select the data rate and the receiver clocking. The maximum input clock frequency is 717 MHz. The maximum data rate for non-DPA operations is 840 Mbps. With DPA, the maximum data rate is 1000 Mbps.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the correct conditions (the same data rate, SERDES factor, and input clock frequency).

You can select the phase relationship of `rx_inclock` and `rx_in` using the **What is the phase alignment of data with respect to the rising edge of rx_inclock (in degrees)?** option.

Figure 17–20. MegaWizard Plug-In Manager - altlvds Receiver Without DPA

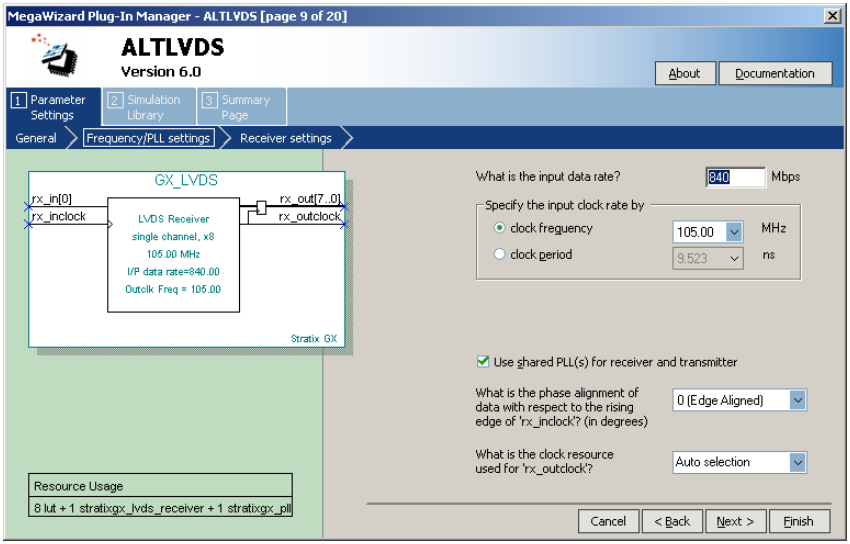
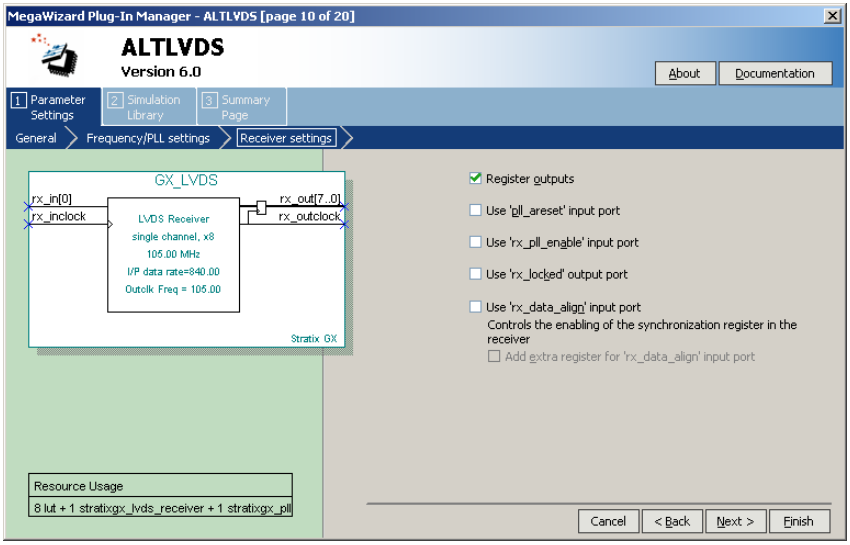


Figure 17–21 shows the last configuration page for the `altlvds` receiver without DPA.

On this page, turn on the **Register outputs** option to facilitate proper SERDES to PLD data transfer. You can turn off this option if there is already a layer of registers before the SERDES to reduce latency.

You can enable the `pll_areset`, `rx_pll_enable`, `rx_locked`, and `rx_data_align` ports on this page. The `pll_areset` port resets the counters in the fast PLL. The `rx_pll_enable` port disables or enables the fast PLL in this receiver instance. The `rx_locked` port indicates when the PLL is locked to the `rx_inclock` frequency and phase. The `rx_data_align` port pauses the fast PLL clock, thereby skipping the reception of the next bit. The `rx_data_align` port affects all channels of the receiver instance at the same time.

Figure 17–21. MegaWizard Plug-In Manager - altlvds Receiver Without DPA



Stratix GX Receiver with DPA

Stratix GX receiver setup with DPA starts on page three. The number of channels and the deserialization factor are similar to those of the transmitter. The DPA option is available for the Stratix GX family. Figure 17–22 shows the page of the `altlvds` MegaWizard Plug-In Manager with DPA selected.

Figure 17–22. MegaWizard Plug-In Manager - altlvds Receiver with DPA

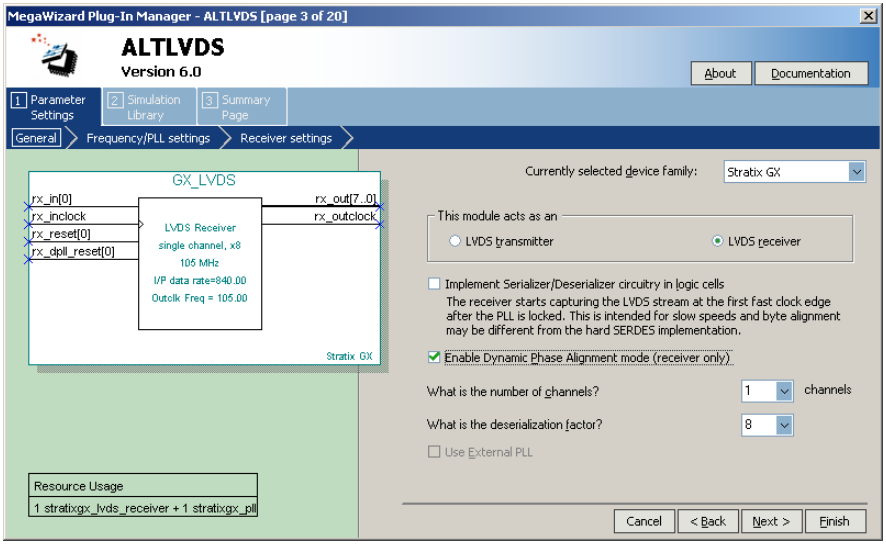


Figure 17–23 shows the page where you select the data rate and input clocking for the receiver. The maximum data rate is 1000 Mbps and the maximum input clock frequency is 717 MHz.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the right conditions (the same data rate, SERDES factor, and input clock frequency).

You can set `rx_outclock` to use a specific clock resource or, if you select Auto selection, the Quartus II software automatically allocates an available clock resource.

You must turn on **Enable the FIFO for DPA channels** option when in DPA mode. This FIFO buffer compensates for any phase differences between the selected phase in the DPA block and `rx_outclock`. There might be data errors if this option is turned off.

Figure 17–23. MegaWizard Plug-In Manager - altlvds Receiver with DPA

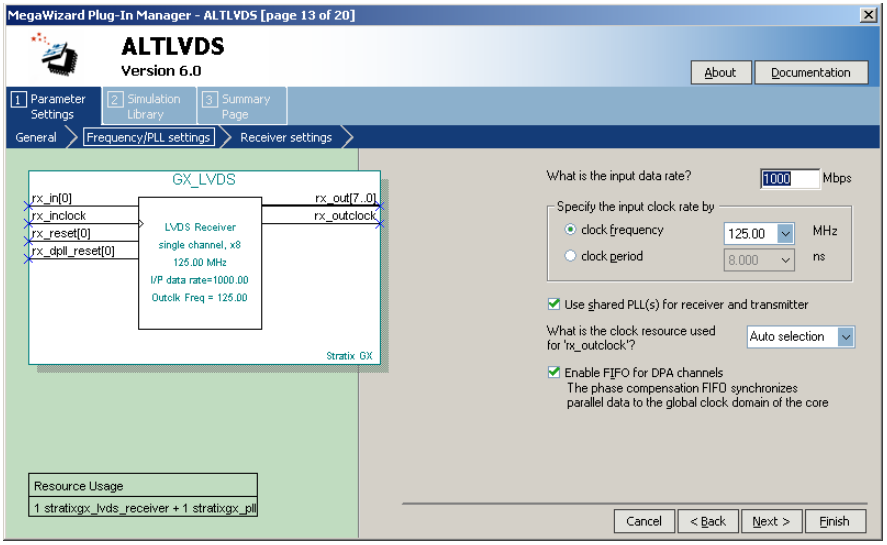


Figure 17–24 shows the last configuration page for the receiver in DPA mode.

Turn on the **Register outputs** option unless there is a layer of register in the user logic right before the SERDES block.

The `pll_areset` port resets the counters in the fast PLL. The `rx_pll_enable` port disables or enables the fast PLL in this receiver instance.

The `rx_channel_data_align` port is a channel-driven port that slips a bit for every rising edge on this port. Each DPA receiver channel has its own `rx_channel_data_align` port that can be used independently of each other.

The `rx_coreclk` and `rx_locked` ports operate the same as in the non-DPA receiver channel. The `rx_locked` port indicates when the PLL is locked to the `rx_inclock` frequency and phase. Turn on the `rx_coreclk` input port option to synchronize the `rx_outdata` to a local PLD clock instead of the parallel clock generated by the fast PLL.

Figure 17–24. MegaWizard Plug-In Manager - altlvds Receiver with DPA

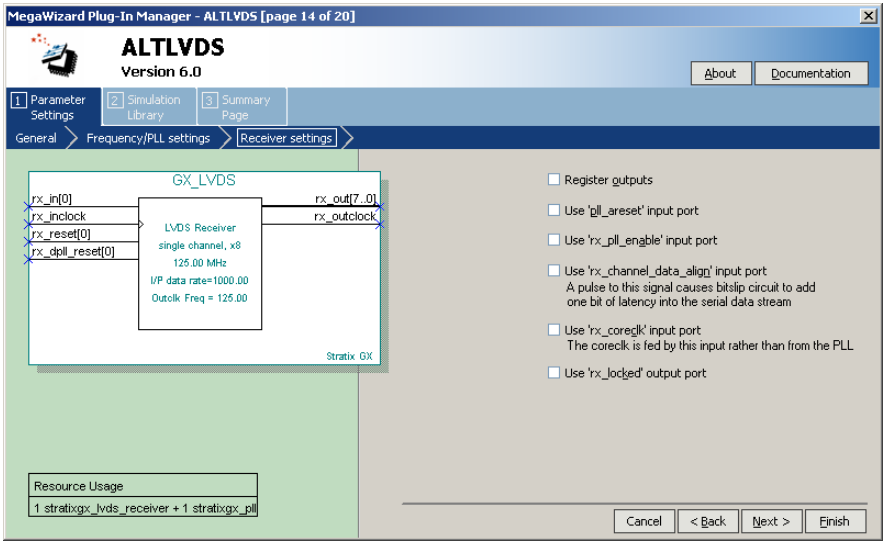


Figure 17–25 shows the Simulation Libraries page of the wizard.

Figure 17–25. MegaWizard Plug-In Manager - altlvds

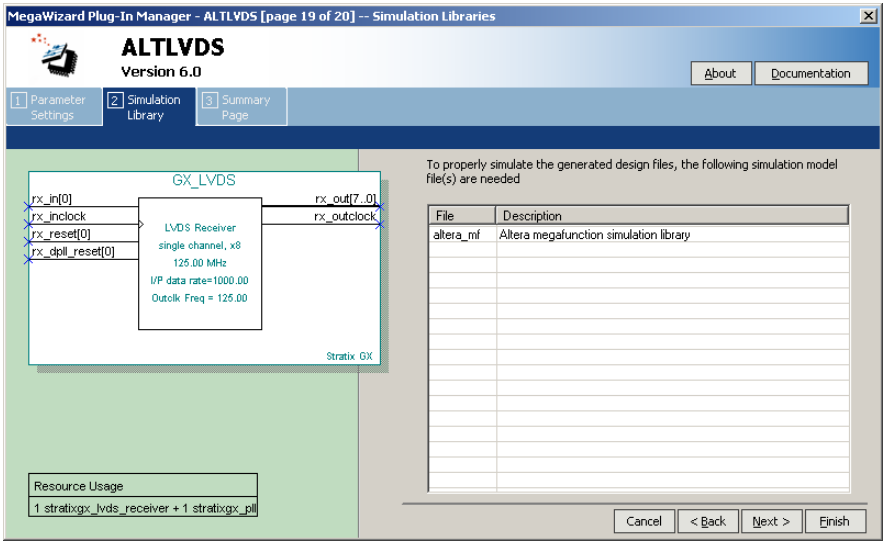
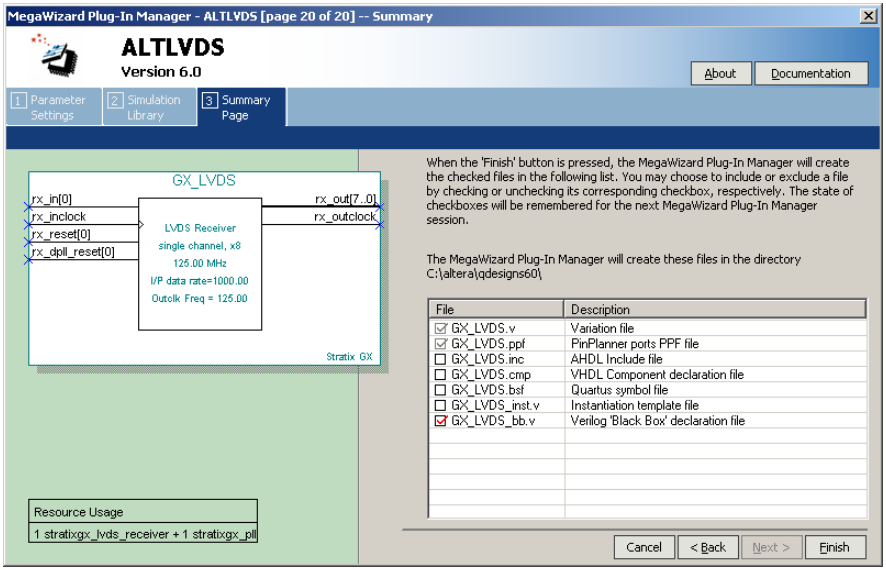


Figure 17–26 shows the last page of the MegaWizard Plug-In Manager. This page shows the files the Quartus II software generates with the options you selected on previous pages.

Figure 17–26. MegaWizard Plug-In Manager - altlvds Receiver



Summary

DPA technology eliminates the restriction of phase-matching the serial data and the source clock at the receiver channels. As a result, DPA eliminates tight board routing and topology restrictions, simplifies channel-to-channel skew calculation, and improves system performance. The combination of DPA technology with 3.125-Gbps transceivers allows Stratix GX devices to address a variety of applications and to effectively implement silicon bridges between protocols.