

MCR12DSM, MCR12DSN

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Device Marking: Logo, Device Type, e.g., R12DSM, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage ⁽¹⁾ (T _J = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM} , V _{RRM}	600 800	Volts
On-State RMS Current (180° Conduction Angles; T _C = 75°C)	I _{T(RMS)}	12	Amps
Average On-State Current (180° Conduction Angles; T _C = 75°C)	I _{T(AV)}	7.6	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T _J = 110°C)	I _{TSM}	100	Amps
Circuit Fusing Consideration (t = 8.3 msec)	I ² t	41	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T _C = 75°C)	P _{GM}	5.0	Watts
Forward Average Gate Power (t = 8.3 msec, T _C = 75°C)	P _{G(AV)}	0.5	Watts
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T _C = 75°C)	I _{GM}	2.0	Amps
Operating Junction Temperature Range	T _J	-40 to 110	°C
Storage Temperature Range	T _{stg}	-40 to 150	°C

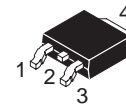
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



ON Semiconductor

<http://onsemi.com>

SCRs
12 AMPERES RMS
600 thru 800 VOLTS



D-PAK
CASE 369A
STYLE 4

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
MCR12DSMT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)
MCR12DSNT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)

Preferred devices are recommended choices for future use and best overall value.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.2	$^{\circ}C/W$
— Junction to Ambient	$R_{\theta JA}$	88	
— Junction to Ambient ⁽¹⁾	$R_{\theta JA}$	80	
Maximum Lead Temperature for Soldering Purposes ⁽²⁾	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ⁽³⁾ ($V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}; R_{GK} = 1.0 \text{ K}\Omega$)	I_{DRM}, I_{RRM}	—	—	10	μA
$T_J = 25^{\circ}C$		—	—	500	
$T_J = 110^{\circ}C$		—	—		

ON CHARACTERISTICS

Peak Reverse Gate Blocking Voltage ($I_{GR} = 10 \mu A$)	V_{GRM}	10	12.5	18	Volts
Peak Reverse Gate Blocking Current ($V_{GR} = 10 \text{ V}$)	I_{GRM}	—	—	1.2	μA
Peak Forward On-State Voltage ⁽⁴⁾ ($I_{TM} = 20 \text{ A}$)	V_{TM}	—	1.3	1.9	Volts
Gate Trigger Current (Continuous dc) ⁽⁵⁾ ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	I_{GT}	5.0	12	200	μA
$T_J = 25^{\circ}C$		—	—	300	
$T_J = -40^{\circ}C$					
Gate Trigger Voltage (Continuous dc) ⁽⁵⁾ ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	V_{GT}	0.45	0.65	1.0	Volts
$T_J = 25^{\circ}C$		—	—	1.5	
$T_J = -40^{\circ}C$		0.2	—	—	
$T_J = 110^{\circ}C$					
Holding Current ($V_D = 12 \text{ V}, \text{Initiating Current} = 200 \text{ mA}, \text{Gate Open}$)	I_H	0.5	1.0	6.0	mA
$T_J = 25^{\circ}C$		—	—	10	
$T_J = -40^{\circ}C$					
Latching Current ($V_D = 12 \text{ V}, I_G = 2.0 \text{ mA}$)	I_L	0.5	1.0	6.0	mA
$T_J = 25^{\circ}C$		—	—	10	
$T_J = -40^{\circ}C$					
Turn-On Time (Source Voltage = 12 V, $R_S = 6.0 \text{ K}\Omega$, $I_T = 16 \text{ A(pk)}$, $R_{GK} = 1.0 \text{ K}\Omega$) ($V_D = \text{Rated } V_{DRM}$, Rise Time = 20 ns, Pulse Width = 10 μs)	tgt	—	2.0	5.0	μs

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off-State Voltage ($V_D = 0.67 \times \text{Rated } V_{DRM}$, Exponential Waveform, $R_{GK} = 1.0 \text{ K}\Omega$, $T_J = 110^{\circ}C$)	dv/dt	2.0	10	—	V/ μs

(1) Surface mounted on minimum recommended pad size.

(2) 1/8" from case for 10 seconds.

(3) Ratings apply for negative gate voltage or $R_{GK} = 1.0 \text{ K}\Omega$. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(4) Pulse Test: Pulse Width $\leq 2.0 \text{ msec}$, Duty Cycle $\leq 2\%$.

(5) R_{GK} current not included in measurement.

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Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

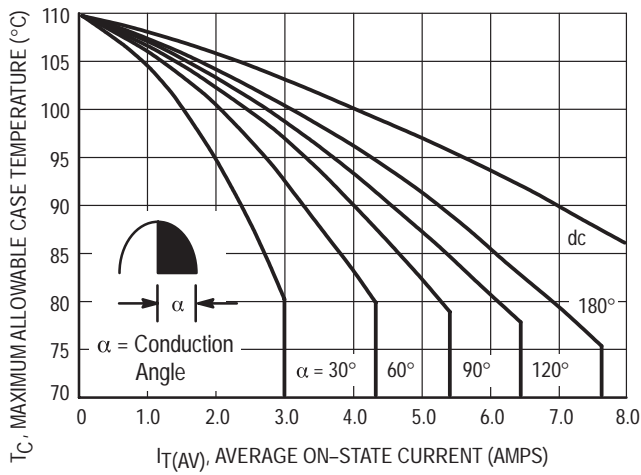
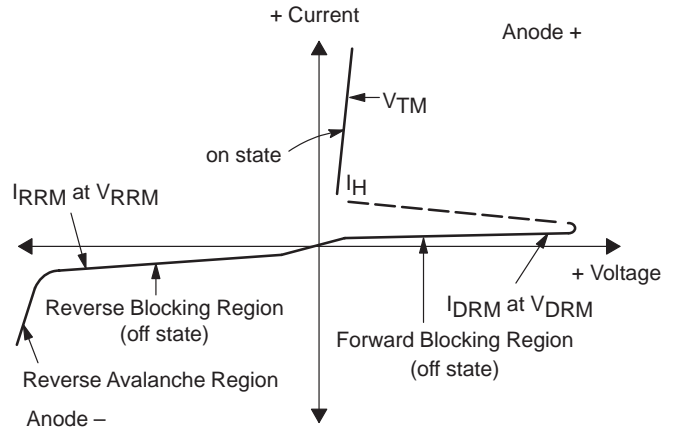


Figure 1. Average Current Derating

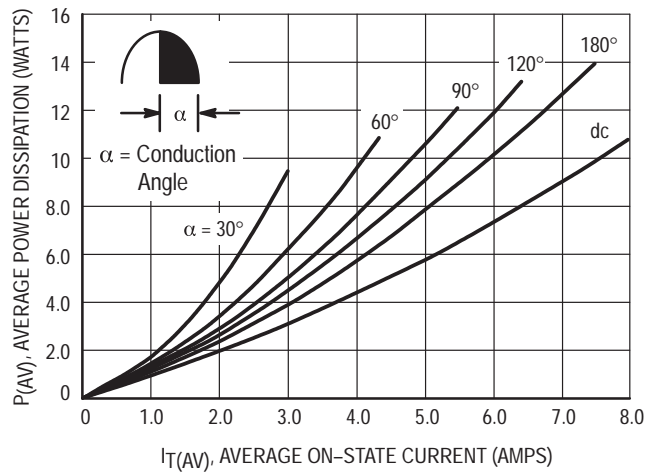


Figure 2. On-State Power Dissipation

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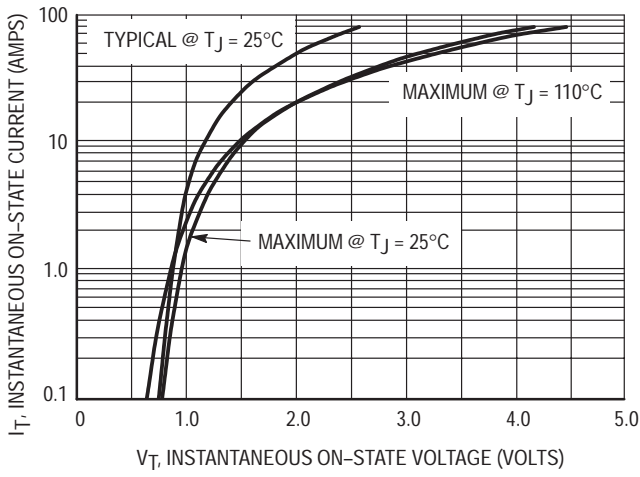


Figure 3. On-State Characteristics

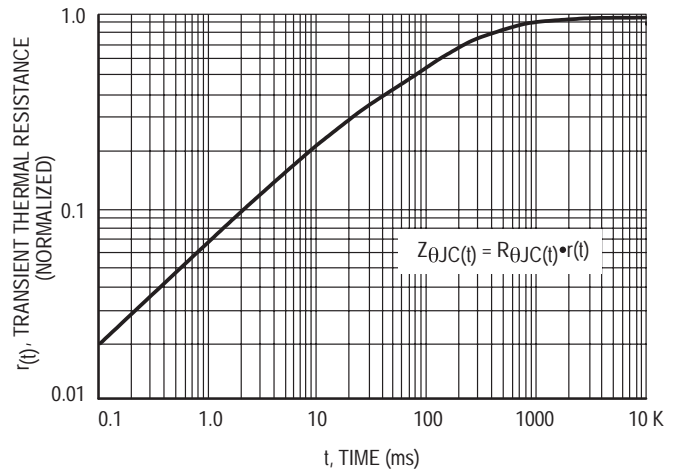


Figure 4. Transient Thermal Response

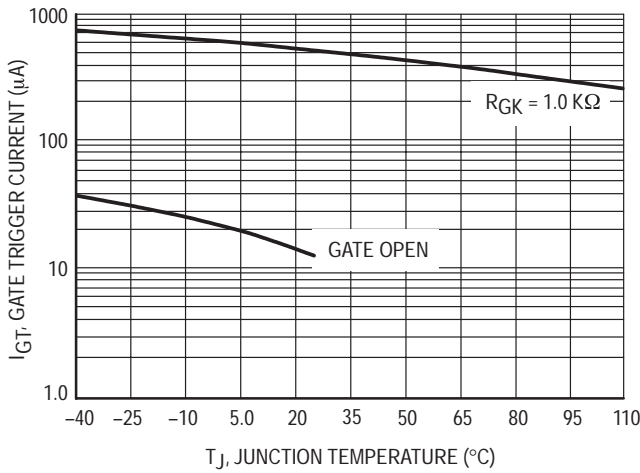


Figure 5. Typical Gate Trigger Current versus Junction Temperature

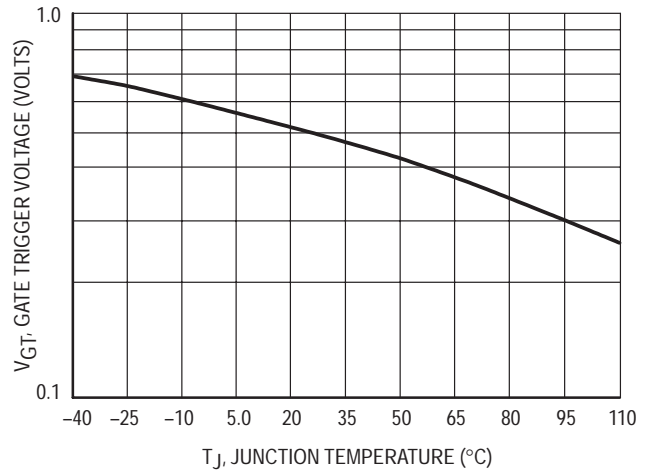


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

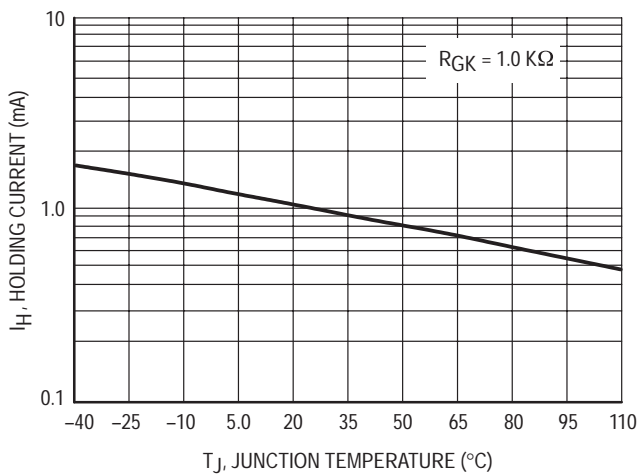


Figure 7. Typical Holding Current versus Junction Temperature

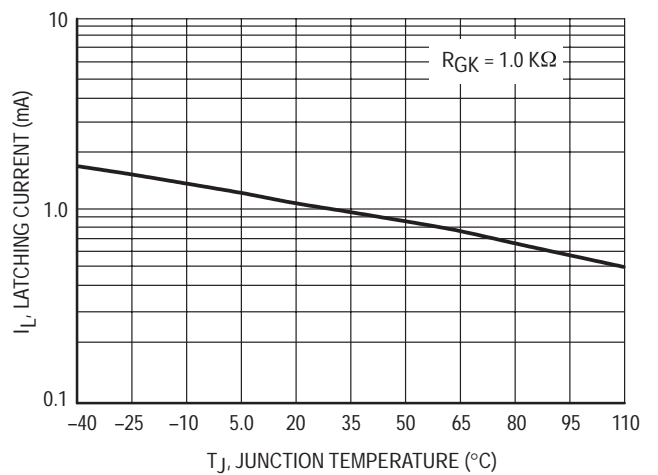


Figure 8. Typical Latching Current versus Junction Temperature

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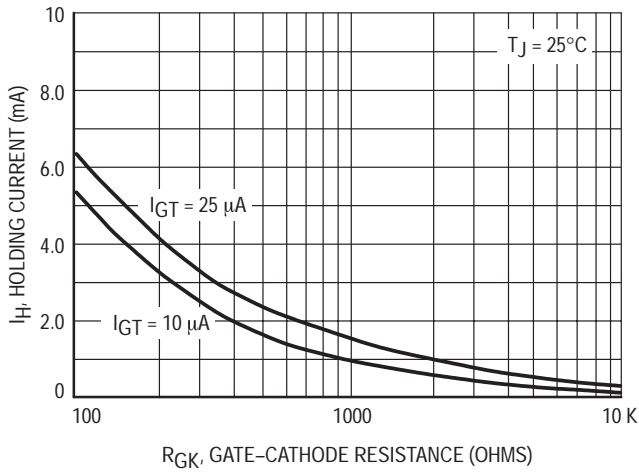


Figure 9. Holding Current versus Gate-Cathode Resistance

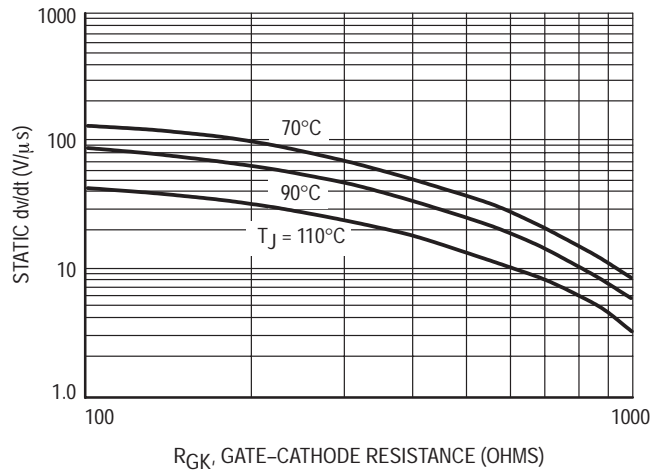


Figure 10. Exponential Static dv/dt versus Gate-Cathode Resistance and Junction Temperature

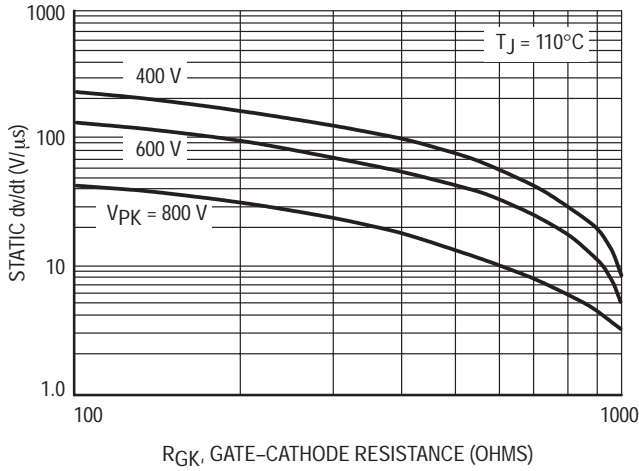


Figure 11. Exponential Static dv/dt versus Gate-Cathode Resistance and Peak Voltage

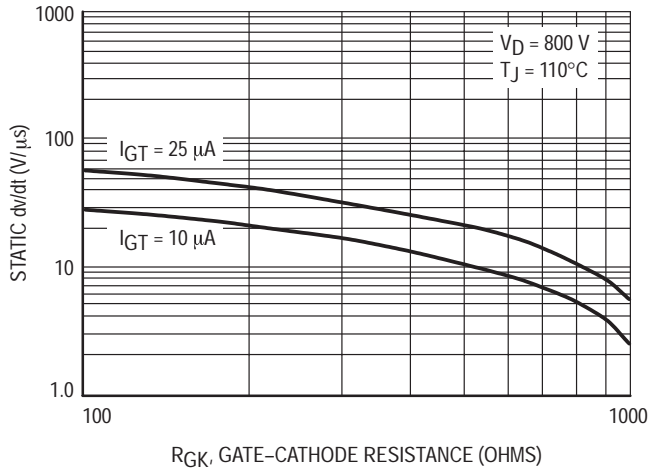


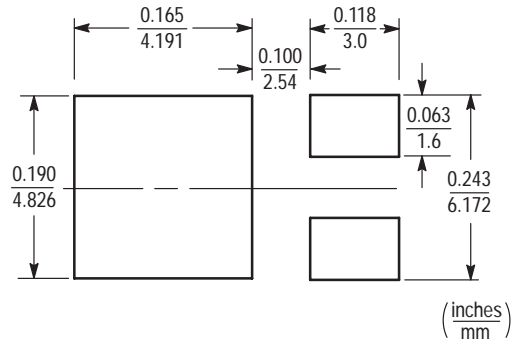
Figure 12. Exponential Static dv/dt versus Gate-Cathode Resistance and Gate Trigger Current Sensitivity

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MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

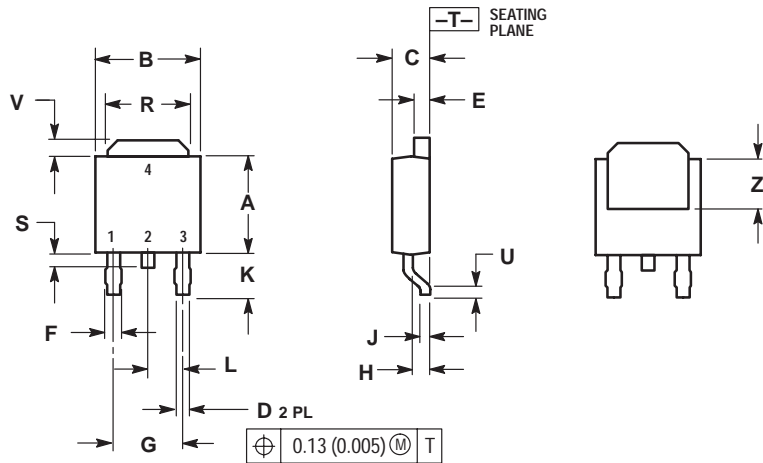


DPAK

MCR12DSM, MCR12DSN

PACKAGE DIMENSIONS

D-PAK CASE 369A-13 ISSUE Z



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

- STYLE 4:
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE

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Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

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