National Semiconductor

December 1994

LMC1992 Digitally-Controlled Stereo Tone and Volume Circuit with Four-Channel Input-Selector

General Description

The LMC1992 is a monolithic integrated circuit that provides four stereo inputs, bass and treble tone controls, and volume, balance, and front-rear fader controls. These functions are digitally controlled through a three-wire communication interface. All of the LMC1992s functions are achieved with only three external capacitors per channel. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of 0 dB.

The internal design is optimized for external capacitors having values of 0.1 μF or less. This allows the use of chip capacitors for coupling and tone control functions.

Low noise and distortion result from using analog switches and thin-film silicon-chromium resistor networks in the signal path.

Volume and fader are at minimum and tone controls are flat when supply voltage is first applied.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1992's select-out/select-in external processor loop.

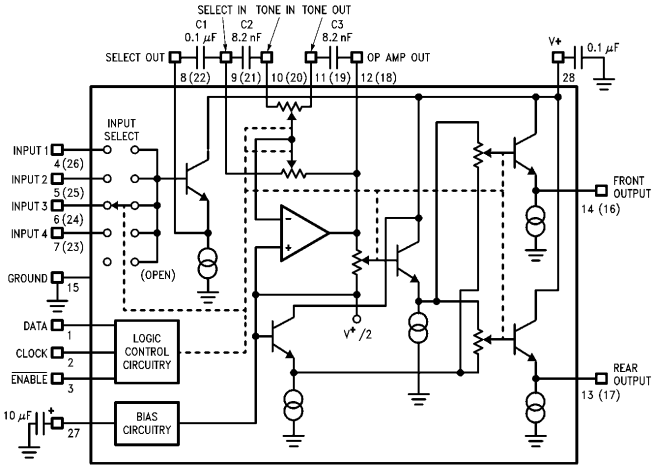
Features

- Low noise and distortion
- Four stereo inputs
- 40 volume levels including mute
- 20 fader levels
- All attenuators have a 2 dB of attenuation per step
- Front/back fade control
- External processor loop
- Only three external components per channel
- Serial programmable: standard MICROWIRE™ interface
- Single supply operation: 6V to 12V supply voltage
- Protection address (similar to DS8906)
- DC-coupled inputs
- Single supply operation

Applications

- Automotive audio systems
- Sound reinforcement systems
- Home entertainment—stereo television and music reproduction systems
- Electronic music (MIDI)

Block and Connection Diagrams



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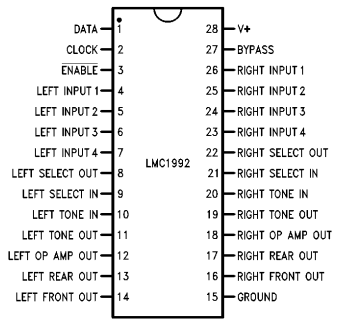
Left channel shown. Pin numbers in parentheses are for the right channel.



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Order Number LMC1992CCN
See NS Package Number N28B

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RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at Any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, Soldering, 10 sec.	+260°C
ESD Susceptibility (Note 5)	2000V
Pins 9, 10, 11, 19, 20, 21	850V

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1992CCN	$0°C \le T_A \le 70°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
I_S	Supply Current			27.0	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 8, 22)	2.3	2.0	V_{rms}(min)
V_{OUT}	Output Voltage	Clipping Level (1.0% THD), Outputs (Pins 13, 14, 16, 17)	1.2	0.65	V_{rms}(min)
THD	Total Harmonic Distortion	All Four Channels Volume Attenuator at 0 dB, Input Level 0.3 V_{rms} Volume Attenuator at −20 dB, Input Level 0.6 V_{rms}	 0.15 0.03	 0.3 0.1	 % (max) % (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$	6.5	30.0	μV_{rms} (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$ Volume Attenuator = −80 dB	5.0	20.0	μV_{rms} (max)
R_{OUT}	DC Output Impedance	Pins 8, 22 Pins 13, 14, 16, 17	100 80	150 120	Ω (max) Ω (max)
R_{IN}	DC Input Impedance	Pins 4, 5, 6, 7, 23, 24, 25, 26	2		MΩ
	Volume Attenuator Range	Pins 16, 17; Volume Attenuation at 0101110100X (0 dB); (Absolute Gain) 01011000000 (80 dB); (Relative to Attenuation at the 0 dB setting)	 −1.0 80.0	 −1.5 75.0	 dB (max) dB (min)
	Volume Step Size	All Volume Attenuation Settings from 01011001010 (60 dB) to 0101110100X (0 dB) (Note 9)	2.0	0.7 4.3	dB (min) dB (max)
	Channel-to-Channel Volume Tracking Error	Fader Attenuation from 1XXX000000 (40 dB) to 1XXX1010X (0 dB)	±0.5	±1.0	dB (max)
	Fader Attenuation Range	Pins 16, 17; Fader Attenuation at 011XXX1010X (0 dB); (Absolute Gain) 011XXX00000 (40 dB); (Relative to Attenuation at the 0 dB setting)	 −1.0 40	 −1.5 38.0	 dB (max) dB (min)
	Fader Step Size	All Fader Attenuation Settings from 011XXX00000 (40 dB) to 011XXX1010X (0 dB) (Note 10)	2.0	1.0 4.5	dB (min) dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 14, 16	±12	±10.0	dB (min)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 14, 16	±0.1	±1.0	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 14, 16	±12	±10.0	dB (min)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 14, 16	±0.1	±1.0	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Frequency Response	−3 dB −0.3 dB (Relative to Signal Amplitude at 1 kHz)	450	 20	kHz kHz (min)
	Channel Separation	V_{IN} = 1.0 V_{rms}	97	70	dB (min)
	Input-Input Isolation	V_{IN} = 1.0 V_{rms} (Note 8)	90	70	dB (min)
PSRR	Power Supply Rejection Ratio	V^+ = 8 V_{DC}; 100 mV_{P-P}, 100 Hz Sinewave Applied to Pin 28	40	31	dB (min)
f_{CLK}	Clock Frequency		1.0	0.5	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage		1.3	2.0	V (min)
$V_{IN(0)}$	Logic "0" Input Voltage		0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, ϕ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1992CCN, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

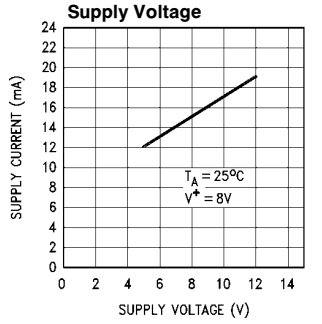
Note 8: The Input-Input Isolation is tested by driving one input and measuring the front outputs when the undriven inputs are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

Note 10: The Fader Step Size is defined as the change in attenuation between any two adjacent fader attenuation settings. The nominal Volume Step Size is 2 dB.

Typical Performance Characteristics

Quiescent Current vs Supply Voltage



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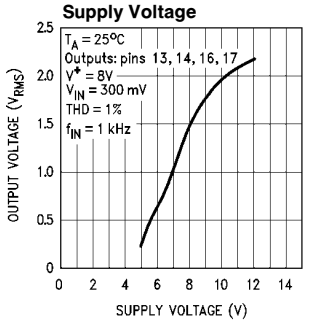
Maximum Output Swing vs Supply Voltage



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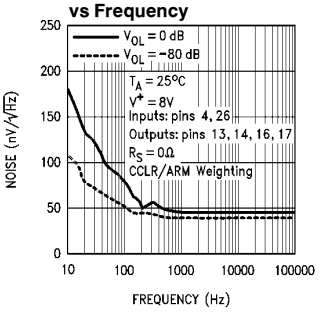
Output Noise Voltage vs Frequency



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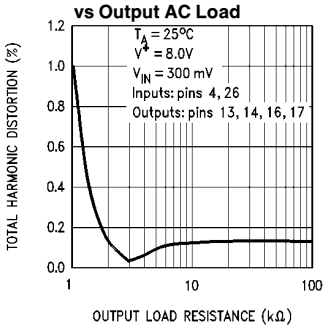
Total Harmonic Distortion vs Output AC Load



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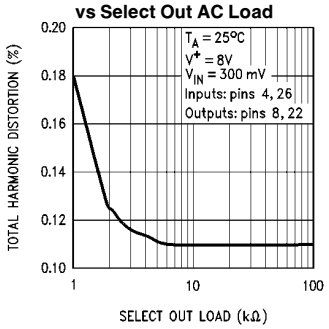
Total Harmonic Distortion vs Select Out AC Load



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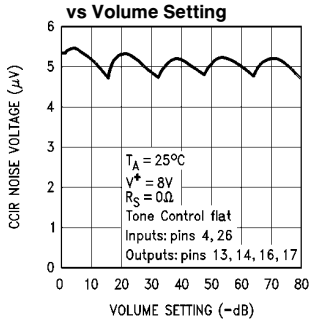
CCIR Output Noise Voltage vs Volume Setting



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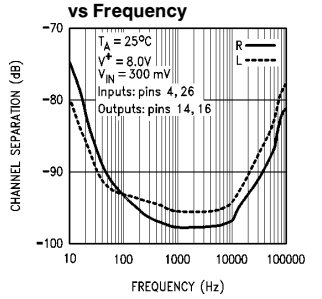
Channel Separation vs Frequency



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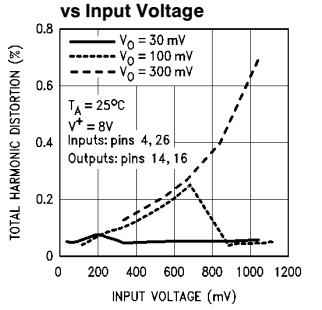
Total Harmonic Distortion vs Input Voltage



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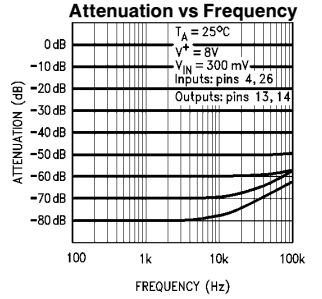
Attenuation vs Frequency



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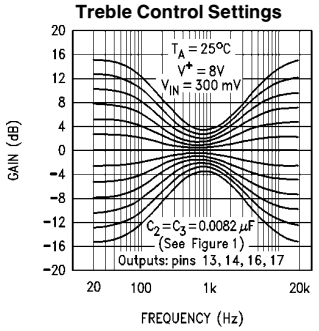
Typical Performance Characteristics (Continued)

Tone Control Response with Equal Bass and Treble Control Settings



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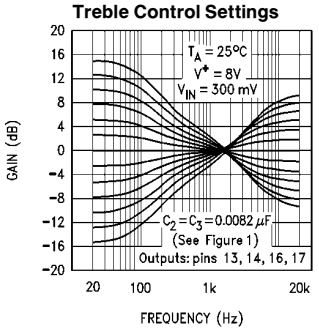
Tone Control Response with Reciprocal Bass and Treble Control Settings



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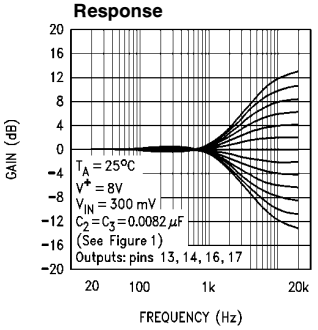
Treble Tone Control Response



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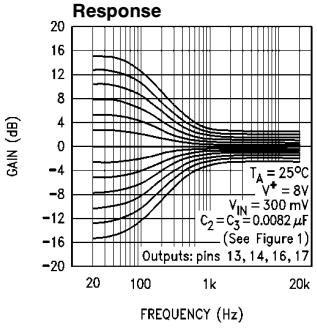
Bass Tone Control Response



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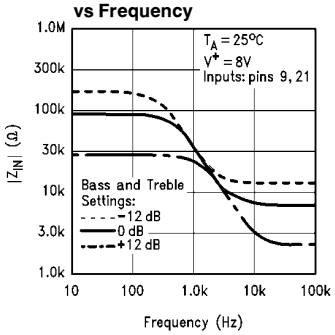
Select In Impedance vs Frequency



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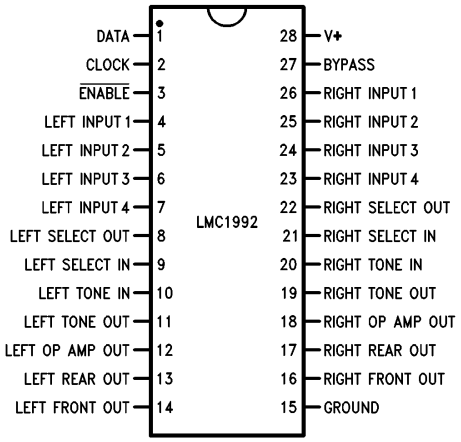
Connection Diagram



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Pin Description

DATA(1) This is the serial data input for communications sent by a controller. The data rate has a maximum frequency of 500 kHz. The LMC1992 requires 11 bits of data to control or change a function: the first two bits, a 1 and 0, select the LMC1992, the next three bits select a function, and the final six bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

CLOCK(2) The CLOCK input accepts a TTL or CMOS level clocking signal. The input is used to clock the DATA input signal and determines when a data bit is valid.

$\overline{\text{ENABLE}}$(3) This input accepts a logic low signal when a controller is addressing the LMC1992. When $\overline{\text{ENABLE}}$ is active, the LMC1992 responds to input signals present on the DATA and CLOCK inputs.

INPUT 1–4 (4–7, 23–26) Four two-channel analog inputs are available on the LMC1992. These pins should be dc-biased to mid-supply.

SELECT OUT (8, 22) The selected INPUT signal is available at this output. This feature allows the use of external signal processing such as noise reduction or graphic equalizers. This output can typically sink 1 mA.

SELECT IN (9, 21) This is the input that an external signal processor uses to return a signal to the LMC1992.

TONE IN (10, 20) This is the input to the tone control amplifier. See the Application Information section titled ''Tone Control Response''.

TONE OUT (11, 19) Tone control amplifier output. See the Application Information section titled ''Tone Control Response''.

OP AMP OUT (12, 18) This output is used externally with the tone control capacitors. Internally, this output is applied to the volume attenuators.

REAR OUT (13, 17) This pin's output signal is intended for the rear amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

FRONT OUT (14, 16) This pin's output signal is intended for the front amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

GROUND (15) This is the system ground connection.

V^+ (28) This is the power supply connection. The LMC1992 is operational with supply voltages from 6V to 12V. It is recommended that this pin is bypassed with 0.1 μF capacitor.

BYPASS (27) A 10 μF capacitor is connected between this pin and ground.

General Information

The LMC1992 is a CMOS/bipolar high quality building block intended for high fidelity audio signal processing. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of −1 dB. While the LMC1992 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and SiCr resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment.

The LMC1992 has internal decoding logic that allows a computer (μP) to communicate directly to the audio control circuitry through a standard MICROWIRE interface. This three-wire interface consists of a DATA input line, a CLOCK input line, and an $\overline{\text{ENABLE}}$ line. When the $\overline{\text{ENABLE}}$ line is low, data can be serially shifted from the controller to the LMC1992. As the $\overline{\text{ENABLE}}$ line goes through the low-to-high transition, any additional data is ignored. Data present in the internal shift register is latched and the instruction is executed.

Figure 1 shows the connection diagram of a typical LMC1992 application.

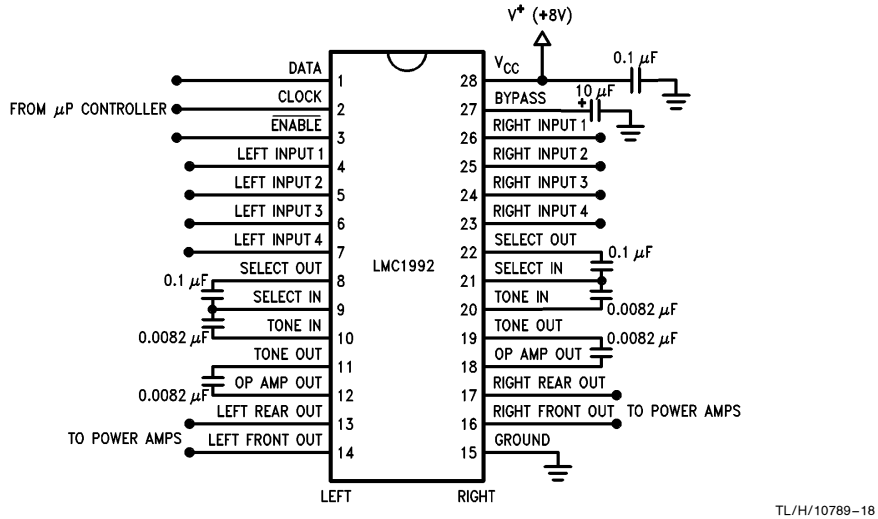

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FIGURE 1. Typical Connection Diagram

Applications Information

MINIMUM LOAD IMPEDANCE

The LMC1992 employs emitter-follower buffers at pins 8 and 22 (SELECT OUT), 13 and 14 (LEFT FRONT and REAR OUTPUTs), and 16 and 17 (RIGHT FRONT-and-REAR OUTPUTs) that buffer output signals. Typical bias current of 1 mA is used for the SELECT OUTPUT buffers and 350 μA for the LEFT-and-RIGHT, FRONT-and-REAR OUTPUT buffers.

The Electrical Specifications table lists a maximum input signal of 2.3 V_{rms} (3.25 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum ac load impedance seen by the SELECT OUT pin is 3.25 kΩ (3.25V/1 mA). For the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the typical maximum output is 1.2 V_{rms} (1.55 V_{peak}). Therefore, the minimum load impedance is 4.43 kΩ (1.55 V/0.35 mA). Trying to use a lower impedance results in a clipped output signal. Therefore, *the chance of clipping can be greatly reduced and much lower distortion levels can be achieved by using load impedances that are an order of magnitude higher than shown here.*

For applications that require dc coupling and the INPUTs biased to $V^+/2$, the minimum load impedance will differ from that detailed in the above discussion. The emitter followers may be potentially operating at high currents because there is a dc voltage $V^+/2 - 0.7V$ at the SELECT OUT pins; dc resistance to ground will result in increased current flow. Latch-up may occur if the total emitter current exceeds 5 mA. This current is a combination of the emitter follower's 1 mA current source and 4 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 0.7V)}{4\ mA} = 1638\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$

To allow for variations and part tolerances, 2.0 kΩ is a good choice for this minimum dc load impedance.

When dc coupling is used at the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the output emitter followers will be operating at a nominal dc voltage of $V^+/2 - 2(0.7V)$. Latch-up may occur if the total emitter current exceeds 1 mA. This current is a combination of the emitter follower's 0.35 mA current source and 0.65 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 2(0.7V))}{0.65\ mA} = 9\ k\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$

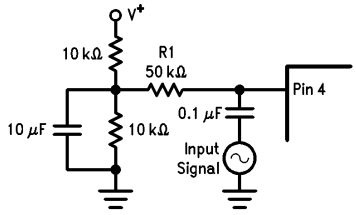

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FIGURE 2. Input Bias Network

To allow for variations and part tolerances, 10 kΩ is a good choice for this minimum dc load impedance.

INPUT IMPEDANCE

For ac coupled input signals the input impedance value is determined by bias resistor R1, as shown in *Figure 2.* A directly coupled input signal will see an emitter follower's nominal input impedance of 2 MΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 96 kΩ at dc and 27 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 28 kΩ at dc and 24 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 8 kΩ and, with the tone controls at maximum boost, is 3 kΩ.

STEREO SIGNAL INPUTS

When operating with a single supply voltage, the stereo signal inputs must be dc biased to one-half of the supply voltage, as shown in *Figure 2.* As an example, with a supply voltage of 8V, all signal sources should have a dc bias of 4V. The maximum input signal level of 6.5 V_{p-p} (for 1% THD) would then swing from 0.75V to 7.25V. Input-to-input crosstalk can be minimized by using a separate dc bias circuit for each stereo input pair.

EXTERNAL SIGNAL PROCESSING

The signal present at the selected input will be available at the SELECT OUT pins 8 (left) and 22 (right). The dc bias voltage at those pins will be one base-emitter voltage, approximately 0.7 V_{dc}, below the source because of the internal emitter follower. Therefore, if the selected input has a bias of 4.0 V_{dc} the dc component at pins 8 and 22 will be about 3.3 V_{dc}.

The LMC1992's SELECT OUT emitter followers allow additional signal sources using emitter follower outputs (such as multiple LMC1992s) to be ''wired-ORed'' together. When this feature is in use, the input channel of the LMC1992 not in use should be set to ''open'' input codes 01000XX0000 or 01000XX011X.

Applications Information (Continued)

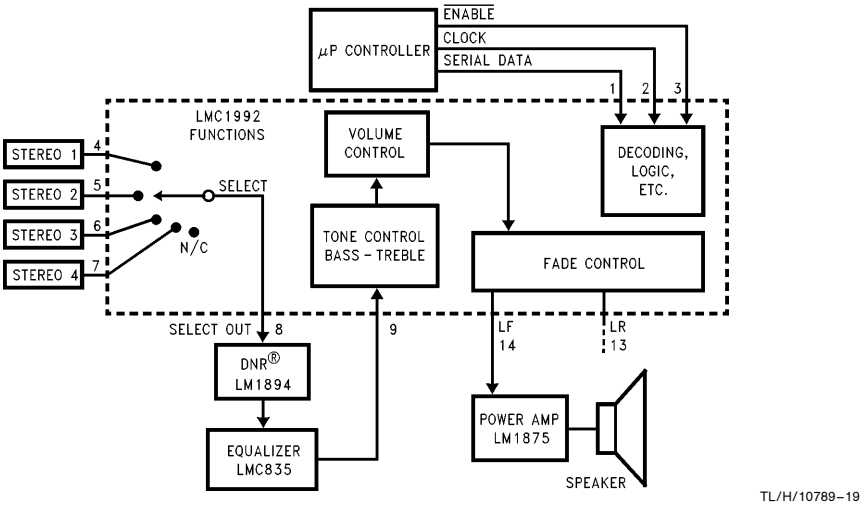

FIGURE 3. System Block Diagram Showing Inclusion of DNR® Noise Reduction (LM1894) and Equalizer (LMC835) (One Channel Only—LMC1992)

The SELECT OUT pins (8 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or mulit-band graphic equalizers (LMC835). It is important to ensure that if both are used, the noise reduction circuitry precede the equalization circuits. Failure to do so will result in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

AUDIO MUTE

A mute function with attenuation of 100 dB is possible with the volume control set to −80 dB and the INPUT select code set to 01000XX0000 (open circuit).

TONE CONTROL RESPONSE

Base and treble tone controls are included in the LMC1992. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 *(Figure 4)* and internal resistors in the feedback loop of the internal tone amplifier. The maximum amplitude boost or cut is determined by the data sent to the LMC1992 (see Table I).

The typical tone control response shown in the Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to ''flat'', the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response will be referred to as the turn-over frequency. With C = C2 = C3, the LMC1992's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14.2\ k\Omega)}$$

The base turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(27.7\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(2.3\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(164.1\ k\Omega)}$$

Applications Information (Continued)

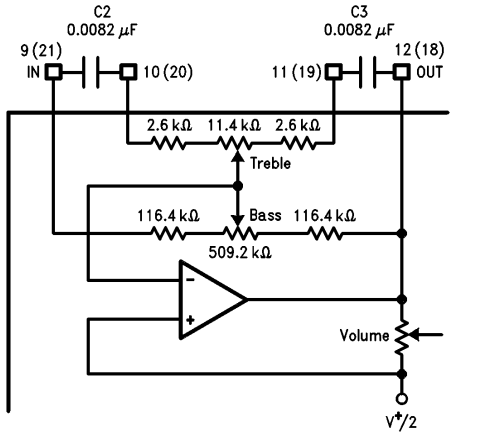

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FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

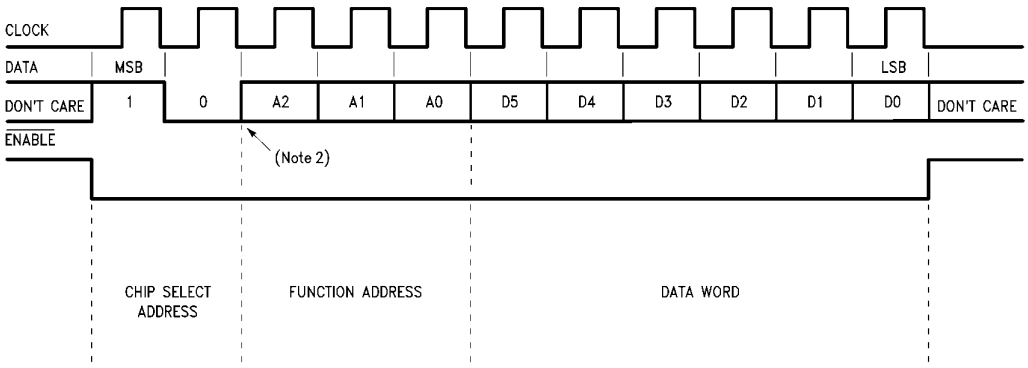
FADER FUNCTION

The four fader functions are all independently adjustable and therefore no balance control is needed. Emulating a balance control is accomplished through software by simultaneously changing a channel's front and rear faders by equal amounts. To satisfy normal balance requirements the faders have an attenuation range of 40 dB.

SERIAL COMMUNICATION INTERFACE

Figure 5 shows the LMC1992's timing diagram for its three wire MICROWIRE interface. A controller's data stream can be any length; once the correct device address is received by the LMC1992, any number of data bits can be sent; the last nine bits occurring before $\overline{\text{ENABLE}}$ goes high are used by the LMC1992. The first two bits in a valid data stream are decoded and used as device address bits. The LMC1992 uses a unique address of 1,0. The LMC1992 will not respond to information on the DATA line if any other address is used. This allows other MICROWIRE serially programmable devices to share the same three-wire communication bus. When $\overline{\text{ENABLE}}$ goes high, any further serial data is ignored and the contents of the shift register is transferred to the data latches. Only when information is received by the data latches do any function or setting changes take place. The first three of nine bits select one of the LMC1992s functions. The remaining six bits set the selected function to the desired value or position.

A data bit is accepted as valid and clocked into an internal shift register on each rising edge of the signal appearing at the LMC1992s CLOCK input pin. Proper data interpretation and operation is ensured when $\overline{\text{ENABLE}}$ makes its falling transition during the time when CLOCK is low. Erroneous operation will result if the $\overline{\text{ENABLE}}$ signal makes its falling transition at any other time.



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Note 1: Negative transition on $\overline{\text{ENABLE}}$ clears previous address. Clock must be low during transition.

Note 2: Additional don't care states may be inserted here for ease of programming. (Optional.)

Note 3: Positive transition on $\overline{\text{ENABLE}}$ latches in new data if the LMC1992 has been addressed. Clock can either be high or low during transition.

FIGURE 5. Clocking Data into the Standard MICROWIRE Interface (Minimum Number of Bits in Data Stream)

Applications Information (Continued)

TABLE I. Programming Codes for LMC1992

Address			Function	Data						Values
A2	A1	A0		D5	D4	D3	D2	D1	D0	
1	1	1	Left Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	1	0	Right Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	0	1	Left Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 − 20 dB = X01010 0 dB = X1010X
1	0	0	Right Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
0	1	1	Volume	MSB	N	N	N	N	LSB	−80 dB = 000000 −40 dB = 010100 0 dB = 10100X
0	1	0	Treble	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	1	Bass	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	0	Input Select	X	X	0	MSB	N	LSB	OPEN = XX0000 INPUT1 = XX0001 INPUT2 = XX0010 INPUT3 = XX0011 INPUT4 = XX0100

Note 1: All attenuators 2 dB/step.

Note 2: Tone controls 2 dB/step @ 100 Hz and 10 kHz.

Note 3: Use of data that deviates from the values shown in the table may result in erroneous results.

SERIAL DATA FORMAT

Table I displays the required data format needed by the LMC1992. Not shown is the 2-bit device address (10). These two bits of information must precede the final nine-bits used as the data word. The first three of these nine bits is the function address.

The VOLUME, TONE, and FADER controls are designed to increment their settings (in 2 dB steps) as the control data is incremented by one LSB. Disregarding the device address and the function address, the VOLUME input code increases from 000000 (−80 dB) to 10100X (0 dB). The TONE controls' input code increases from XX0000 (−12 dB) to XX0110 (0 dB) to XX1100 (+12 dB). The code for the FADERs starts from X00000 (−40 dB) and goes to X1010X (0 dB).

The table shows that VOLUME is the only function that uses all six bits to choose that function's setting. The remaining functions use less than six bits; the unused bits are shown as ''X''s (''don't care''). While these ''don't care'' bits have no effect on their respective function, the LMC1992 must receive them for proper operation. If neglected, erroneous or unknown results will occur.

Applications Information (Continued)

DATA TRANSFER EXAMPLE

The following routines, based on the flowchart shown in *Figure 6,* are examples of COPS™ microcontroller instruction code that can be used to control the LMC1992 (see National Semiconductor's COPS Microcontrollers Databook for more information). These routines arbitrarily select COPS register 0 for I/O purposes. When these routines are entered, it is assumed that chip select is high, SK (clock) is low, and SO (data) is low. These routines exit with chip select high and SK and SO low. Output port G0 is arbitrarily chosen to send the chip select signal to the LMC1992.

The 11 data bits needed to control the LMC1992 are assumed to be in the 4-bit registers, 13–15, with the 4 MSBs in register 13. With this configuration there is an extra bit for a data stream that is 12 bits long. As previously mentioned, there can be any number of extra bits between the device address and the function address.

DATA TRANSFER ROUTINE 1

This general purpose routine handles all the overhead except loading data into registers 13–15. It sends the data according to the conditions discussed above. The data will be lost at the conclusion of the routine. This routine consumes only 17 ROM memory locations.

```
OUT1:  LBI  0,13  ;POINT TO START OF DATA
                  ;WORD
       SC         ;SET C TO ENABLE SK CLOCK
       OGI  14    ;SELECT EXTERNAL DEVICE G0
                  ;= 0
       LEI  8     ;ENABLE SHIFT REGISTER
                  ;OUTPUT
SEND:  LD
       XAS        ;DATA TRANSMISSION LOOP
       XIS        ;TURN-ON CLOCK
       JP   SEND
       RC
       OGI  15    ;DE-SELECT EXTERNAL
                   DEVICE
       LEI  0     ;SET SO TO 0
       RET
```

DATA TRANSFER ROUTINE 2

This routine performs the same function as routine 1 while preserving the contents of the data registers. This routine takes only 21 ROM memory locations.

```
OUT1:  LBI  0,13  ;POINT TO START OF DATA
                  ;WORD
       SC         ;SET C TO ENABLE SK CLOCK
       OGI  14    ;SELECT EXTERNAL DEVICE
                  G0 ;=0
       LEI  8     ;ENABLE SHIFT REGISTER
                  ;OUTPUT
       JP   SEND2
SEND1: XAS
SEND2: LD         ;DATA TRANSMISSION LOOP
       XIS        ;TURN-ON CLOCK
       JP   SEND1
       XAS        ;SEND LAST DATA
       RC         ;WAIT 4 CYCLES - DATA
                  ;GOING OUT
       CLRA
       NOP
       XAS        ;TURN SK CLOCK OFF
       OGI  15    ;DE-SELECT DEVICE
       LEI  0     ;SET SO TO 0
       RET
```

Applications Information (Continued)

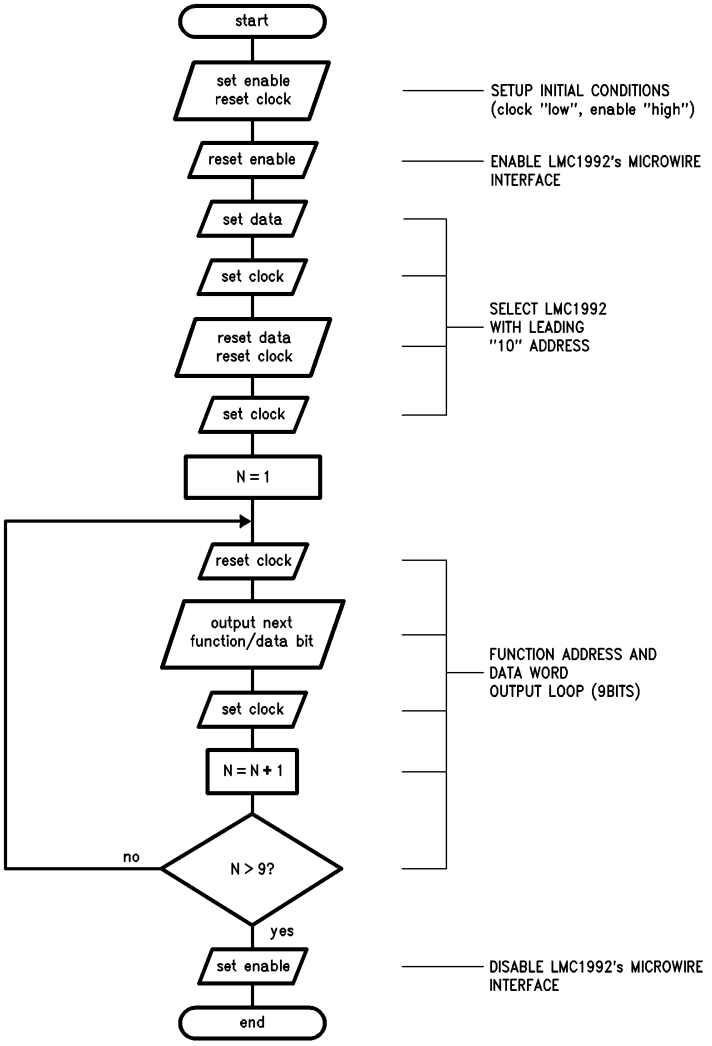

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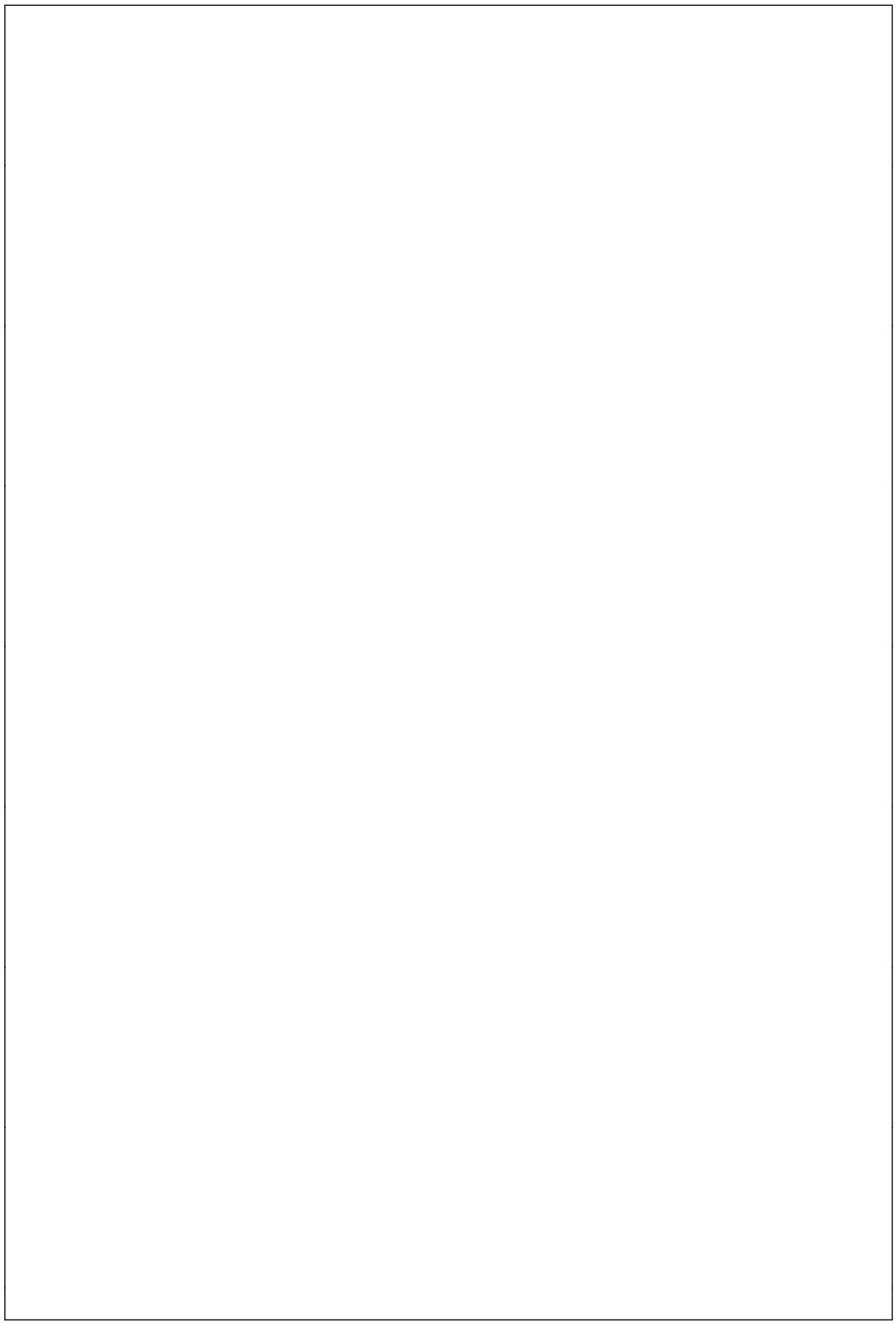
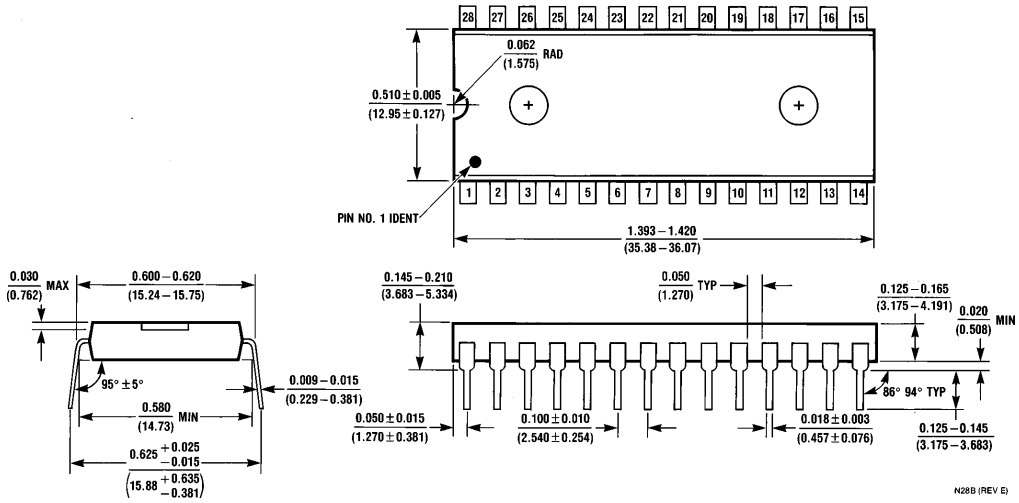
FIGURE 6. General Data Transmission Flowchart to Send Serial Data to the LMC1992's MICROWIRE Compatible Digital Inputs



Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number LMC1992CCN
NS Package Number N28B

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