

NXP BT134-800 4Q Triac datasheet

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Planar passivated four quadrant triac in a SOT82 plastic package intended for use in general purpose bidirectional switching and phase control applications.

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BT134-800

4Q Triac

21 November 2013

Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT82 plastic package intended for use in general purpose bidirectional switching and phase control applications.

2. Features and benefits

- Compact package
- High blocking voltage capability
- Less sensitive gate for improved noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	25	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	4	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G+; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	5	35	mA
		$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	8	35	mA
		$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2- G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	11	35	mA



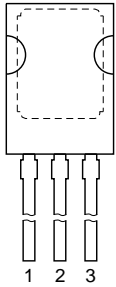
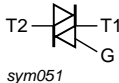
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	30	70	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>SIP3 (SOT82)</p>	
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT134-800	SIP3	plastic single-ended package; 3 leads (in-line)	SOT82

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	25	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	27	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	3.1	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu s$; T2+ G+	-	50	$A/\mu s$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu s$; T2+ G-	-	50	$A/\mu s$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu s$; T2- G-	-	50	$A/\mu s$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu s$; T2- G+	-	10	$A/\mu s$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}C$
T_j	junction temperature		-	125	$^{\circ}C$

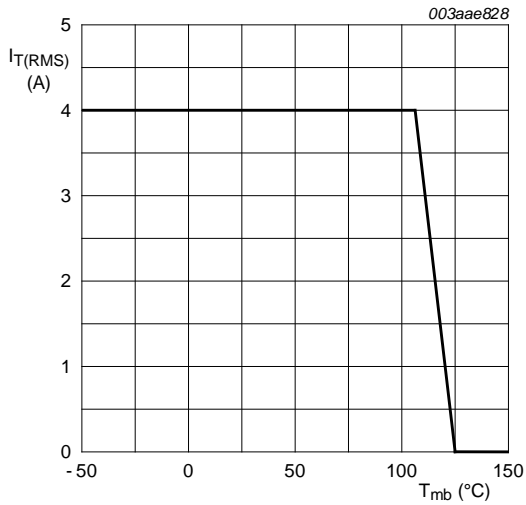
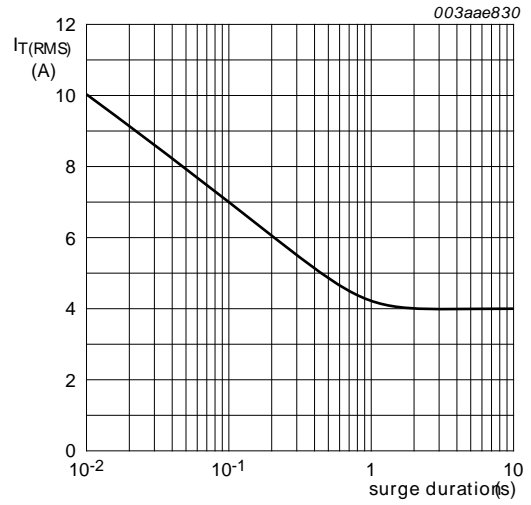
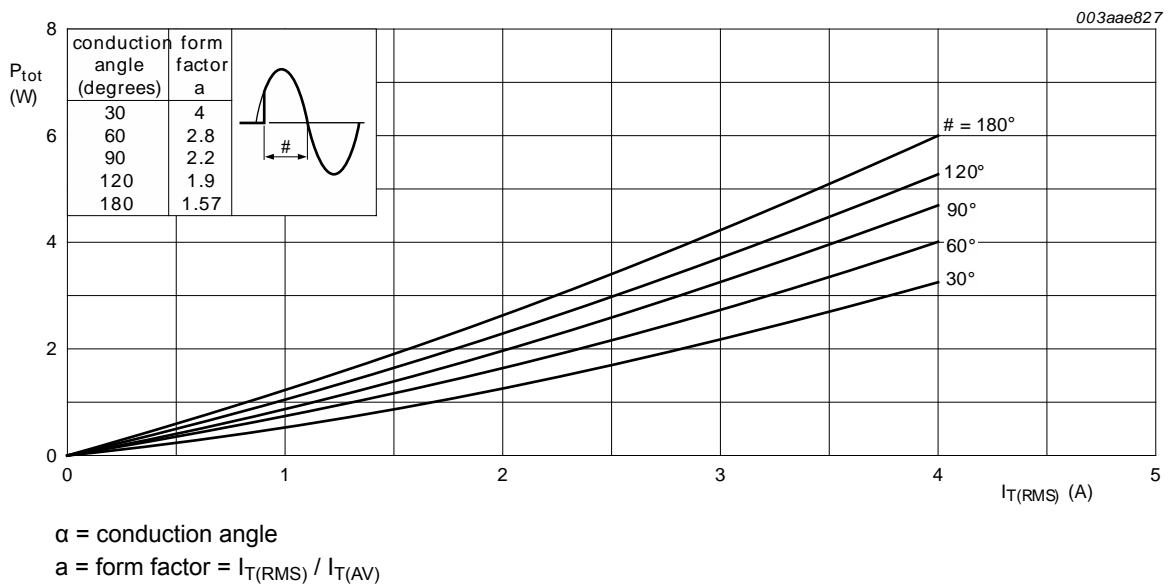


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz
 $T_{mb} \leq 107\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

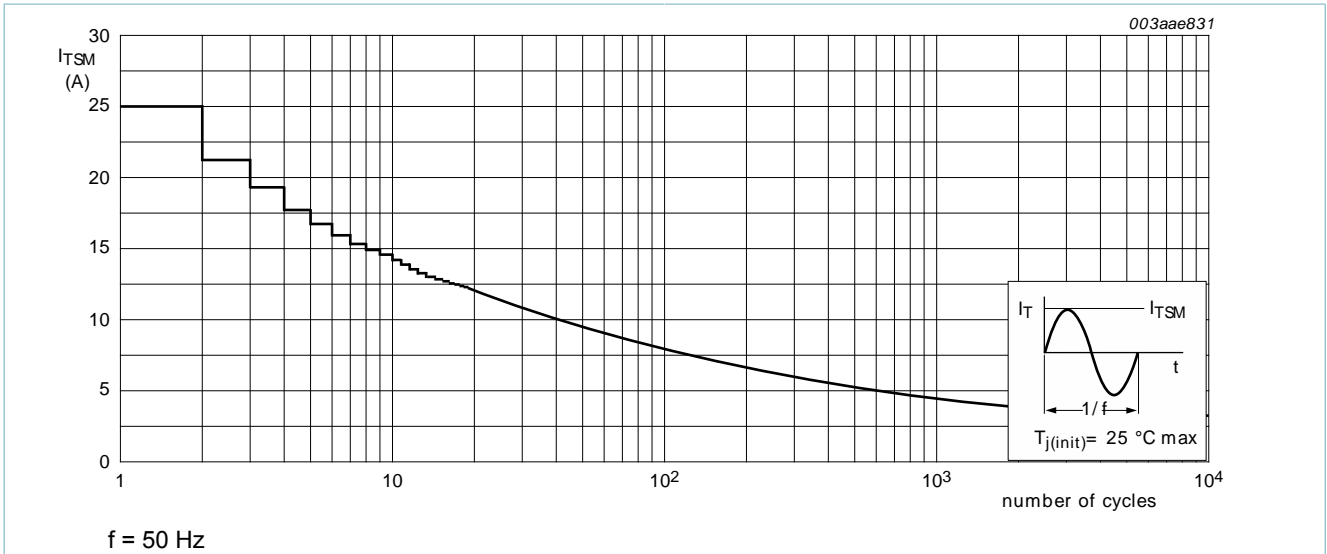


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

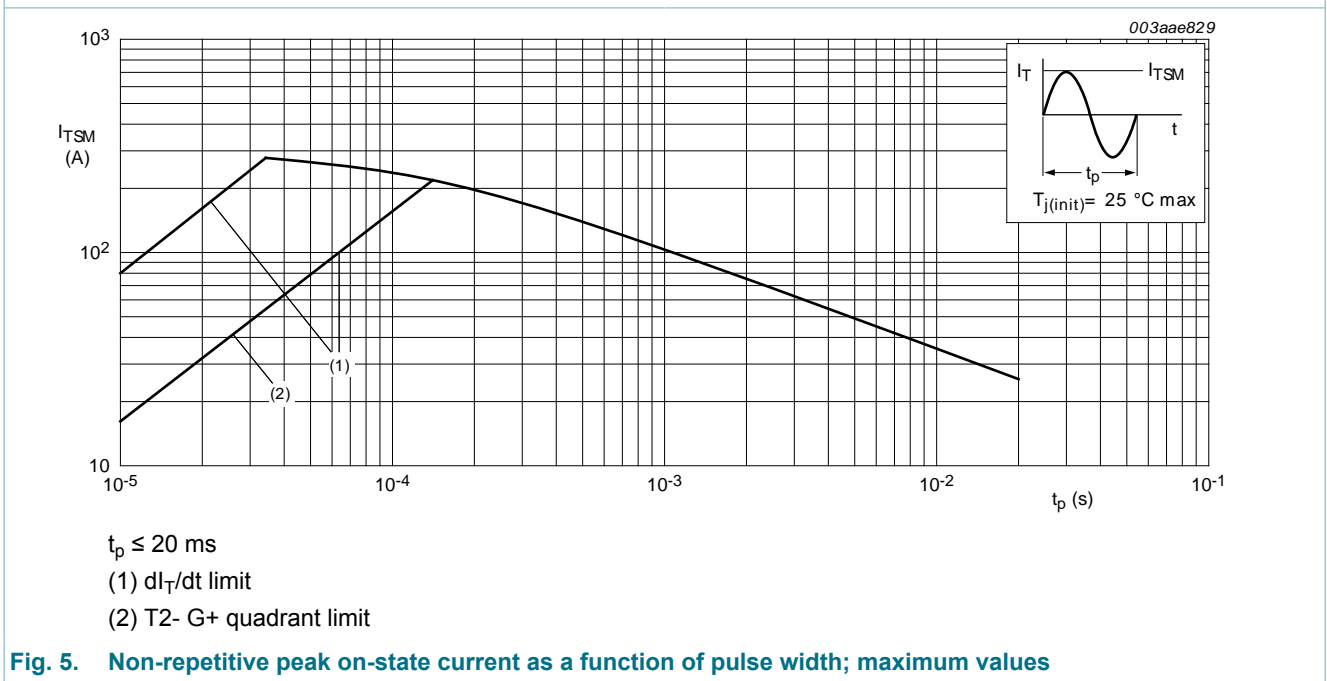


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	3.7	K/W
		full cycle; Fig. 6	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	100	-	K/W

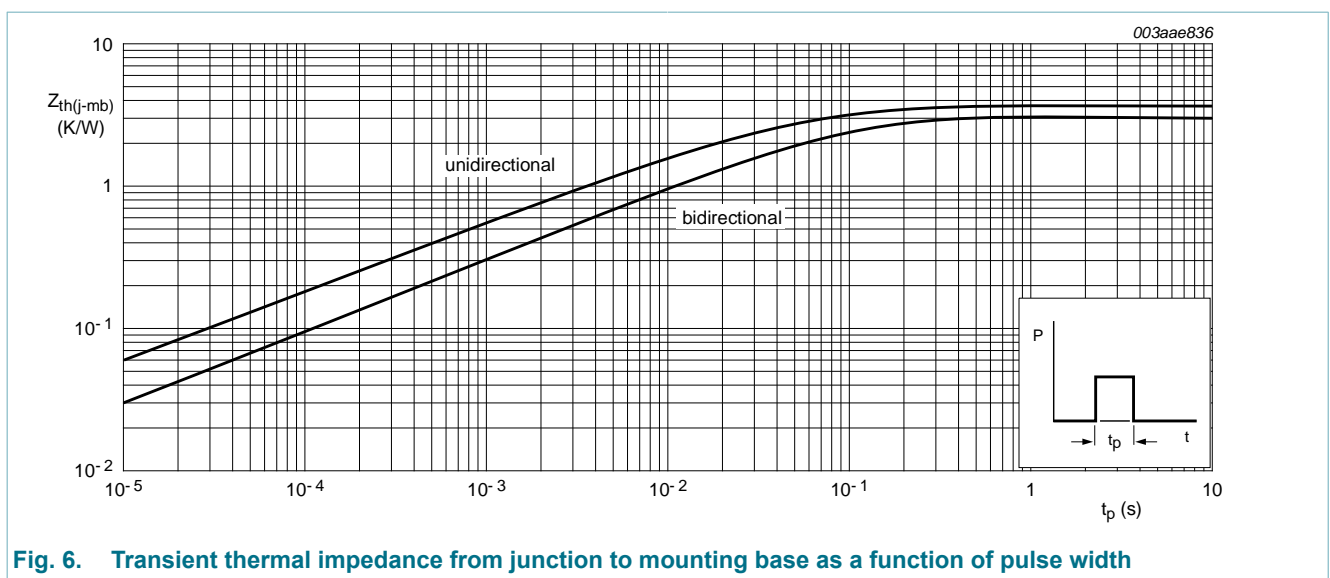
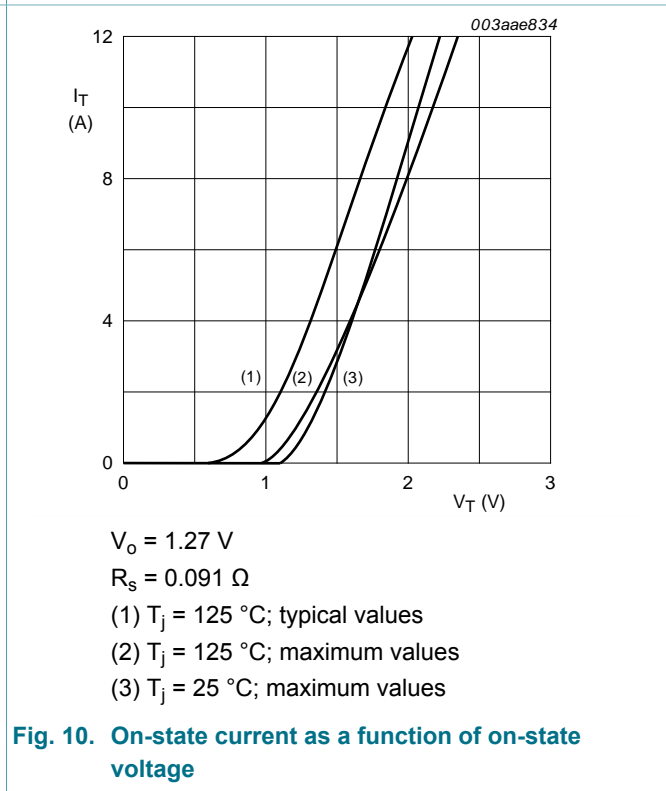
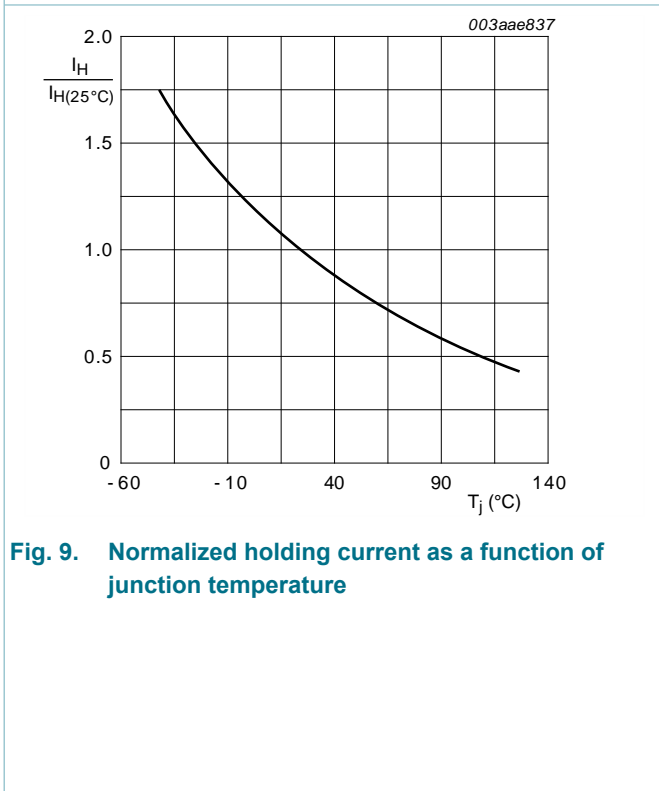
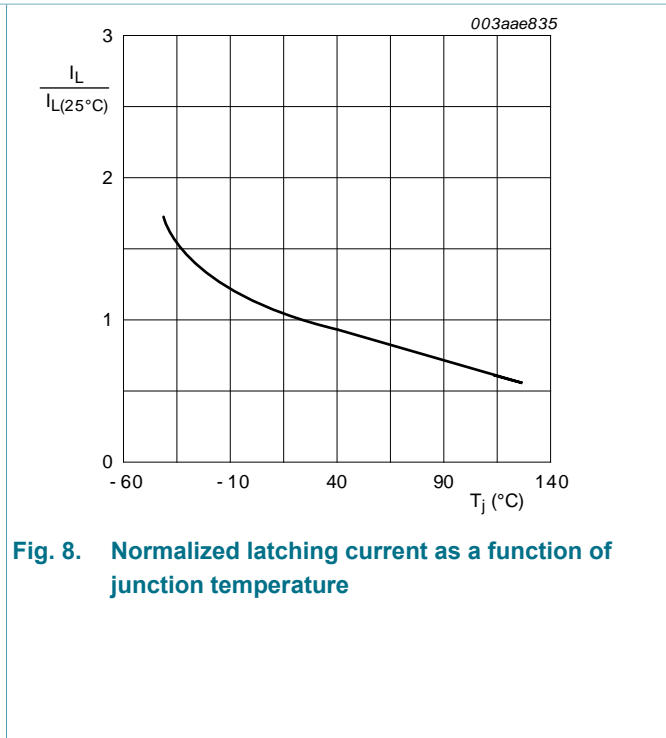
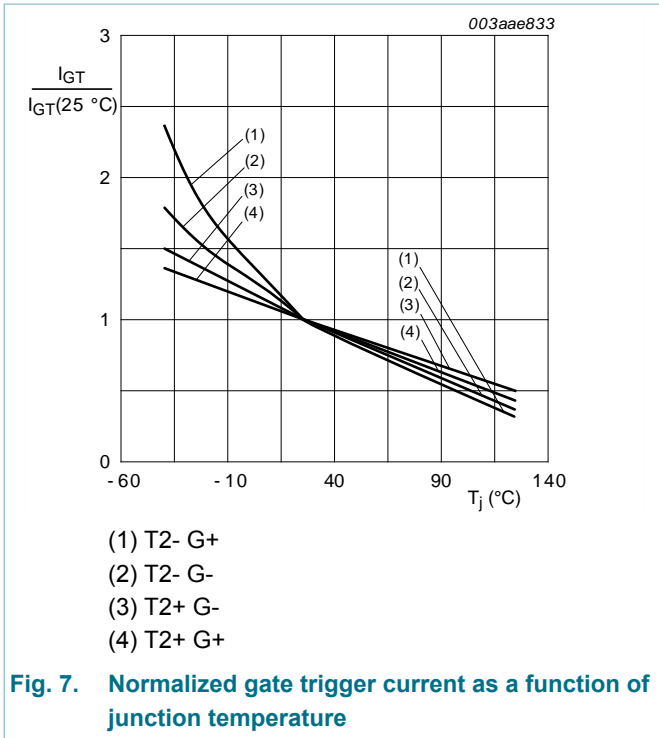


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	5	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	8	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	11	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	-	30	70	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	7	20	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	16	30	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8	-	5	20	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 8	-	7	30	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	5	15	mA
V_T	on-state voltage	$I_T = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.4	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	100	250	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 95\text{ °C}$; $dI_{com}/dt = 1.8\text{ A/ms}$; $I_T = 4\text{ A}$; gate open circuit	-	50	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 6\text{ A}$; $V_D = 800\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu$ s	-	2	-	μ s



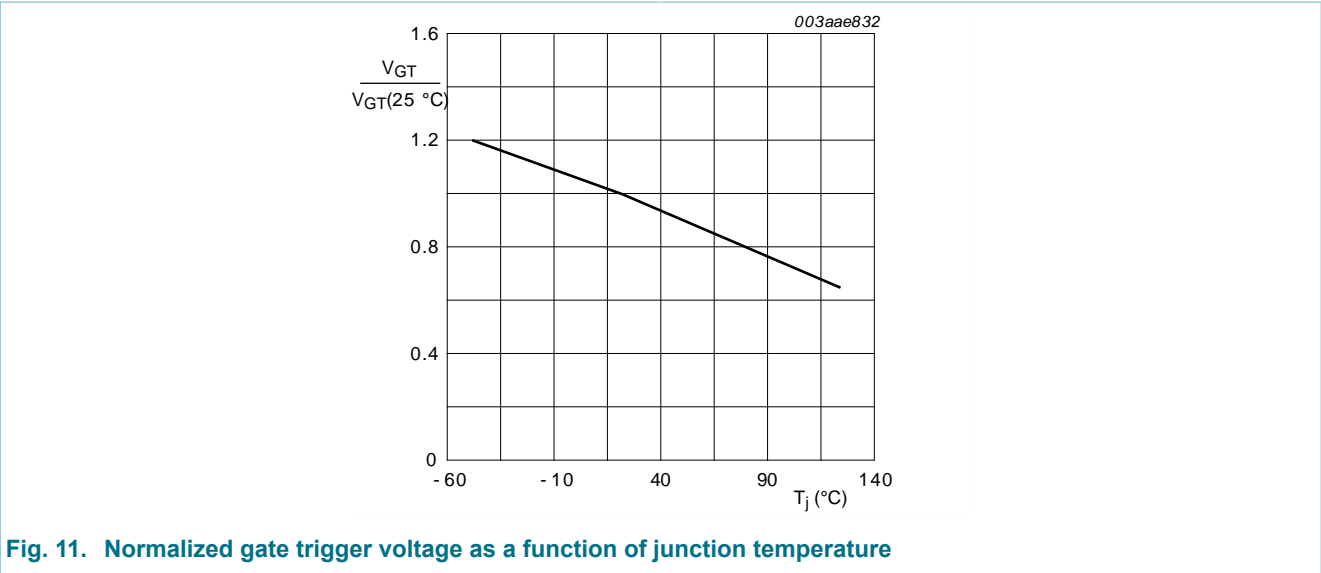


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

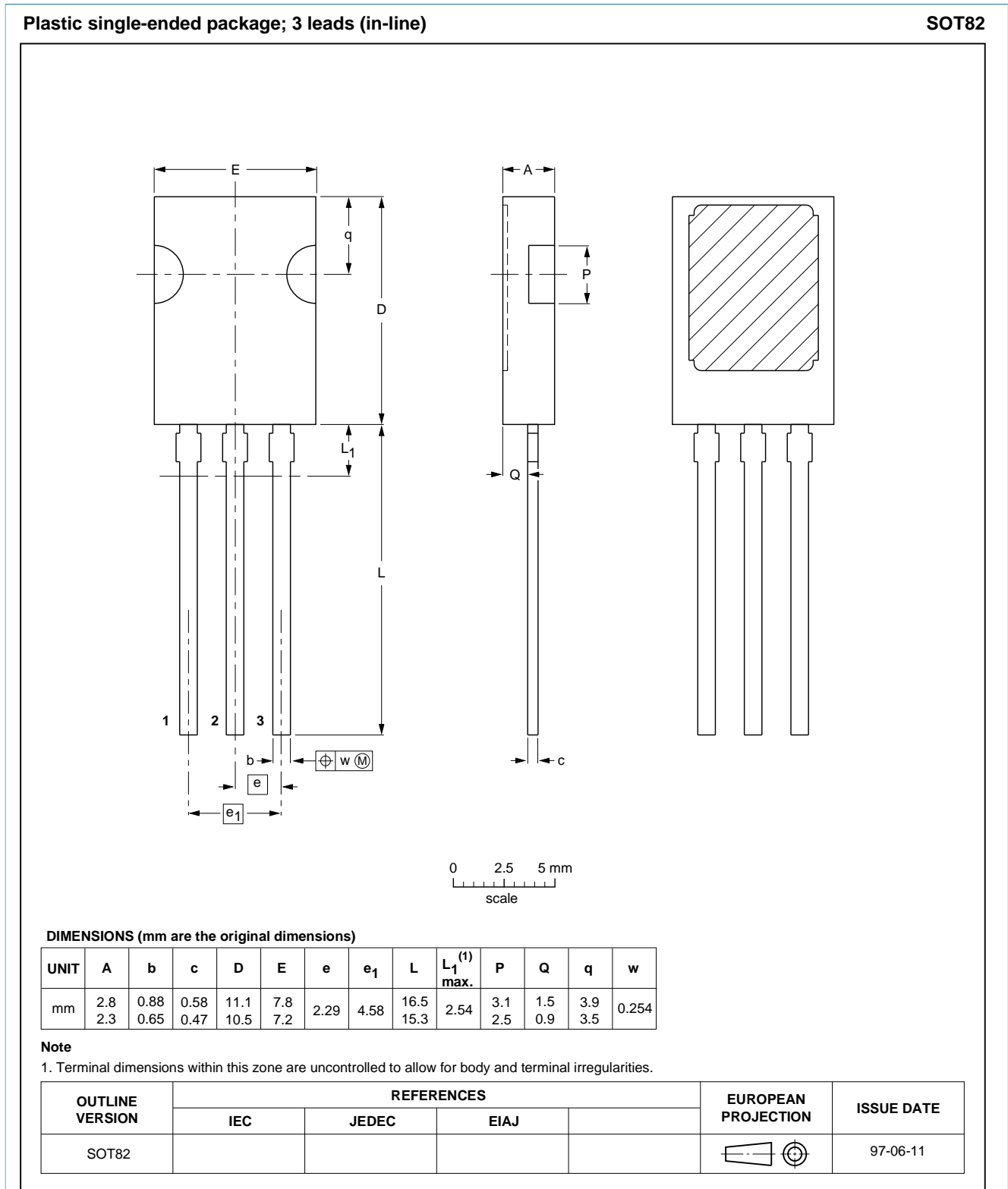


Fig. 12. Package outline SIP3 (SOT82)

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