

NXP BT134-600D 4Q Triac datasheet

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Planar passivated very sensitive gate four quadrant triac in a SOT82 plastic package intended for use in general purpose bidirectional switching and phase control applications where high sensitivity is required in all four quadrants. This "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

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BT134-600D

4Q Triac

21 November 2013

Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT82 plastic package intended for use in general purpose bidirectional switching and phase control applications where high sensitivity is required in all four quadrants. This "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Compact package
- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	25	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	4	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2	5	mA



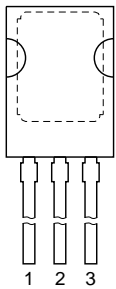

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2.5	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2.5	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	5	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	1.2	10	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>SIP3 (SOT82)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT134-600D	SIP3	plastic single-ended package; 3 leads (in-line)	SOT82

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	25	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	27	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	3.1	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G+	-	50	$\text{A}/\mu\text{s}$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G-	-	50	$\text{A}/\mu\text{s}$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G-	-	50	$\text{A}/\mu\text{s}$
		$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G+	-	10	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$

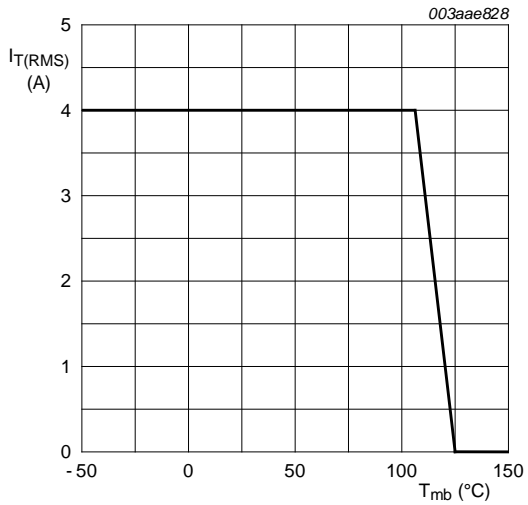
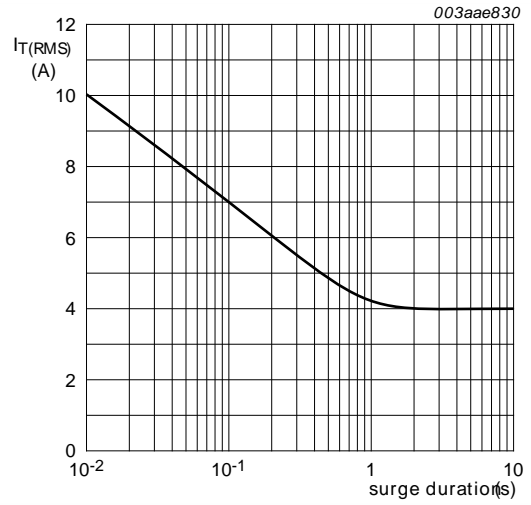
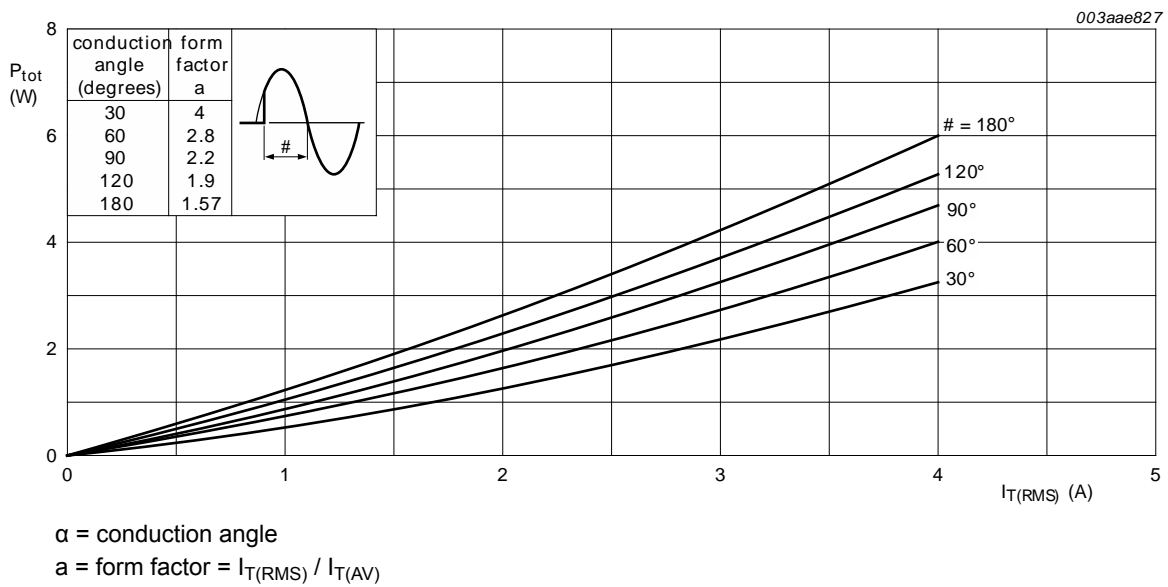


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz
T_{mb} ≤ 107 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle
a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

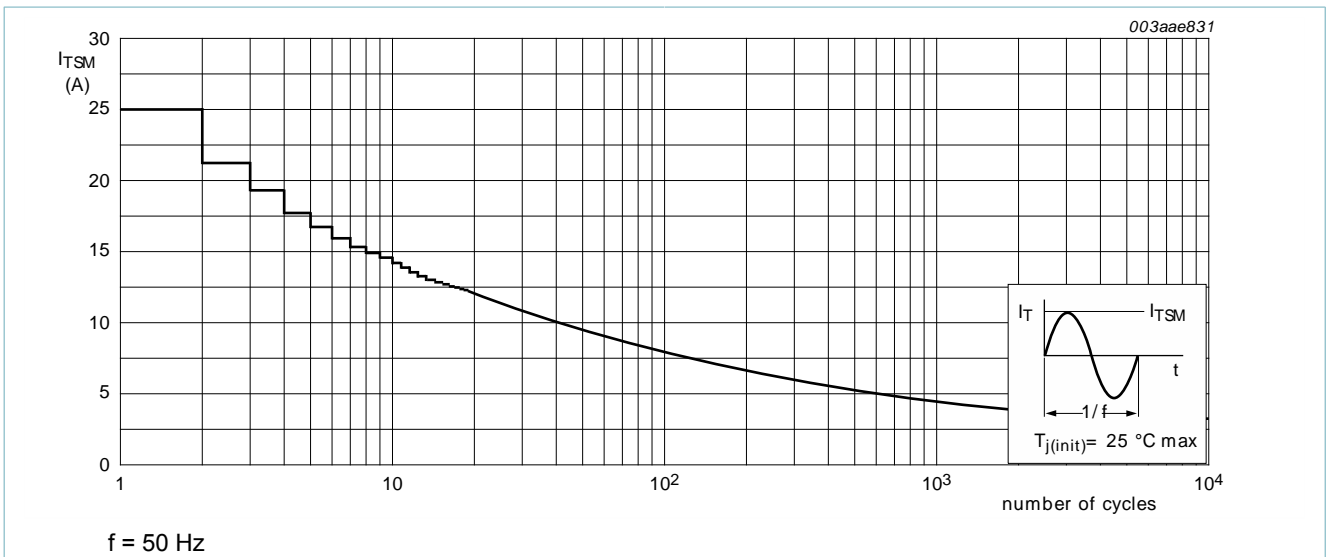


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

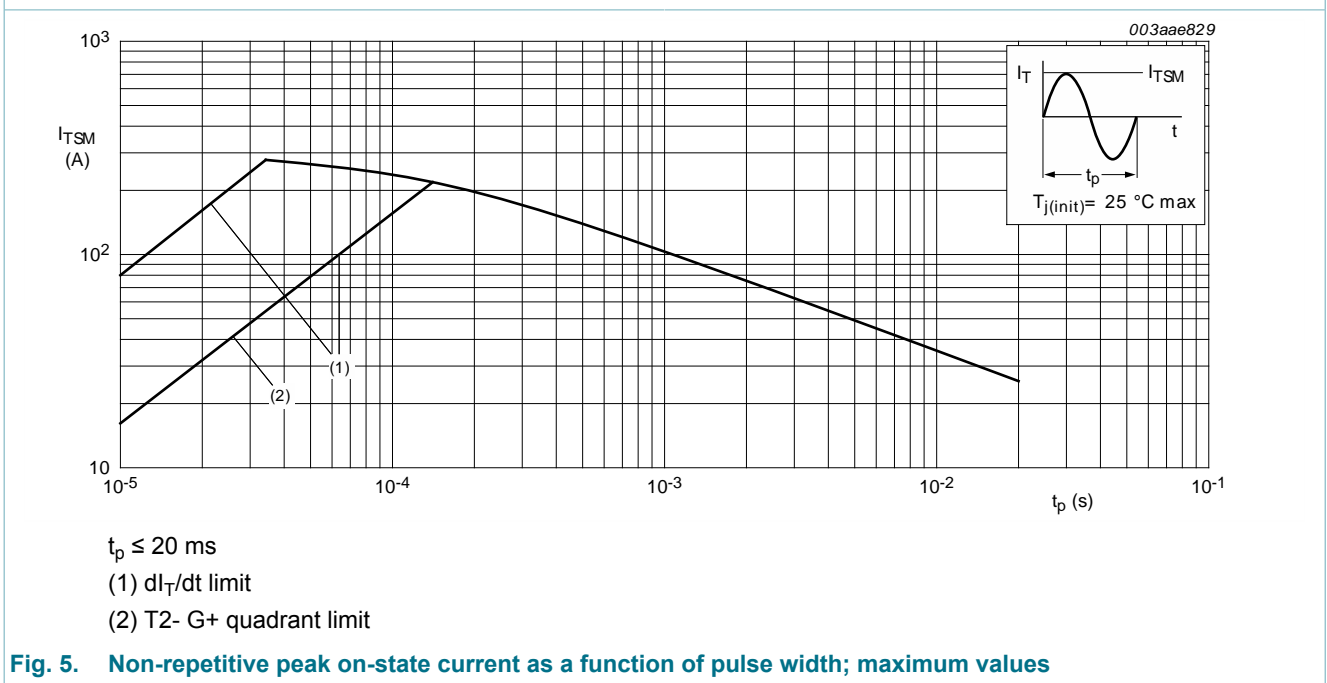


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	3.7	K/W
		full cycle; Fig. 6	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	100	-	K/W

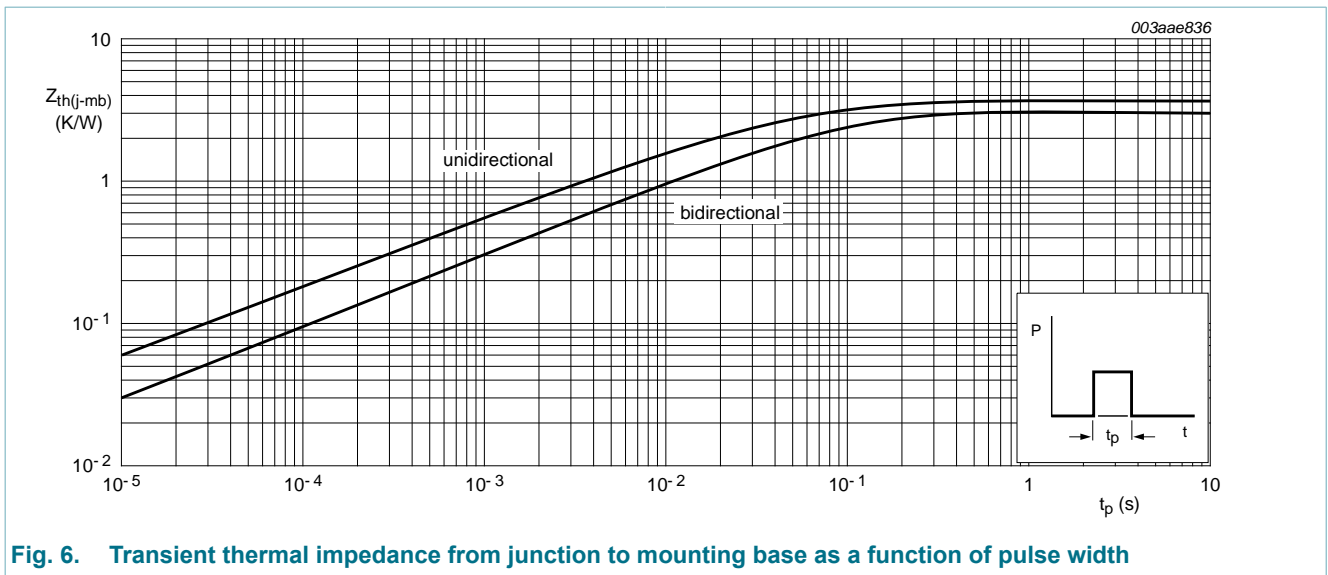
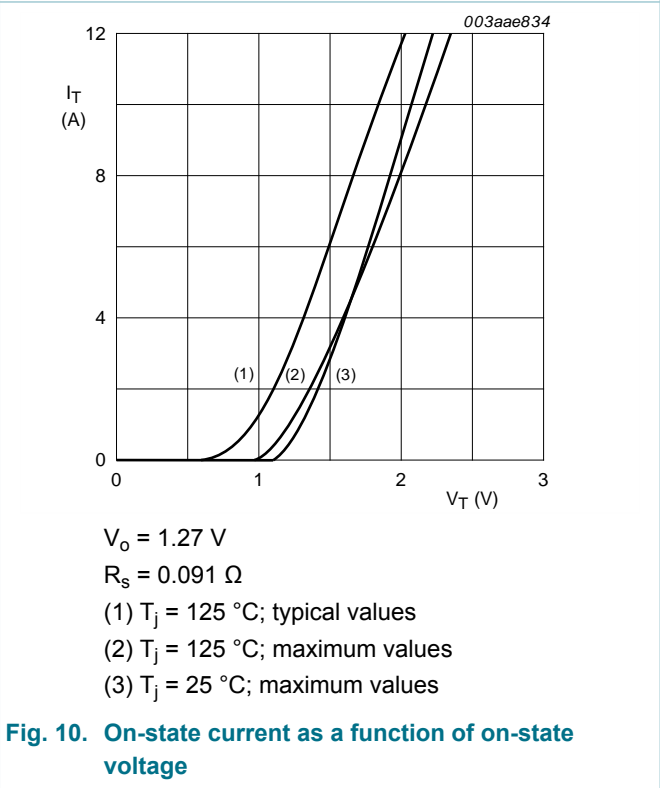
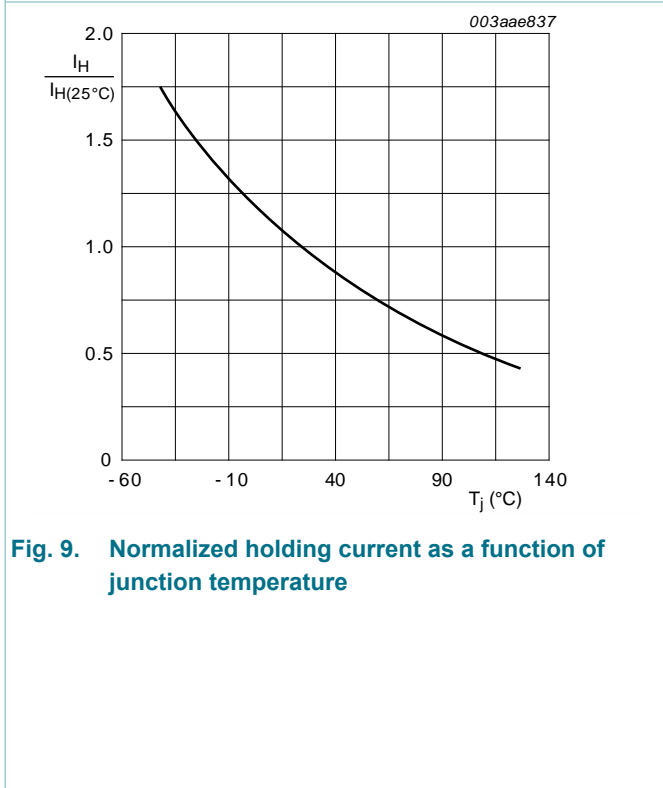
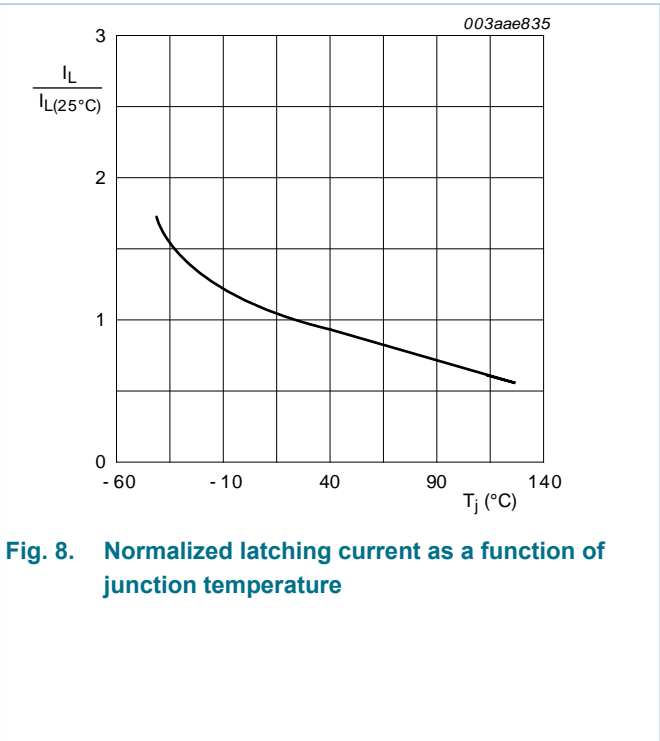
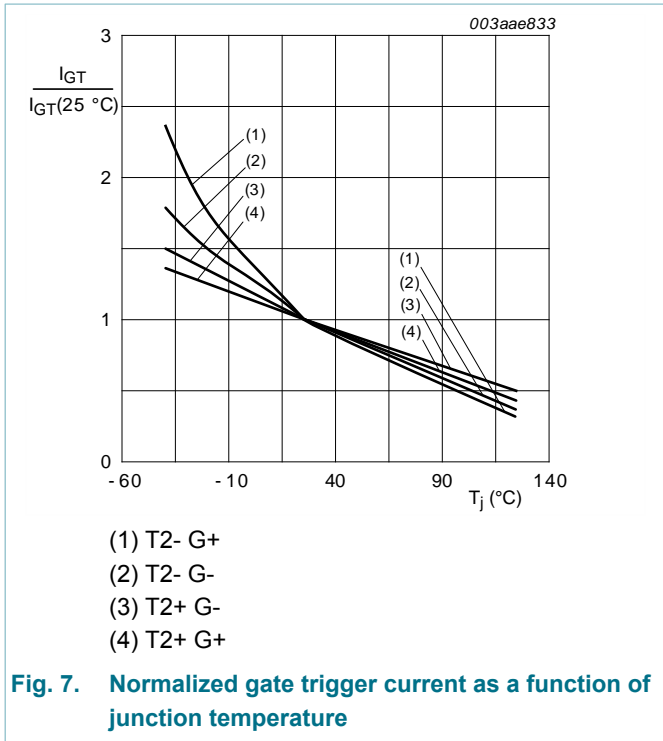


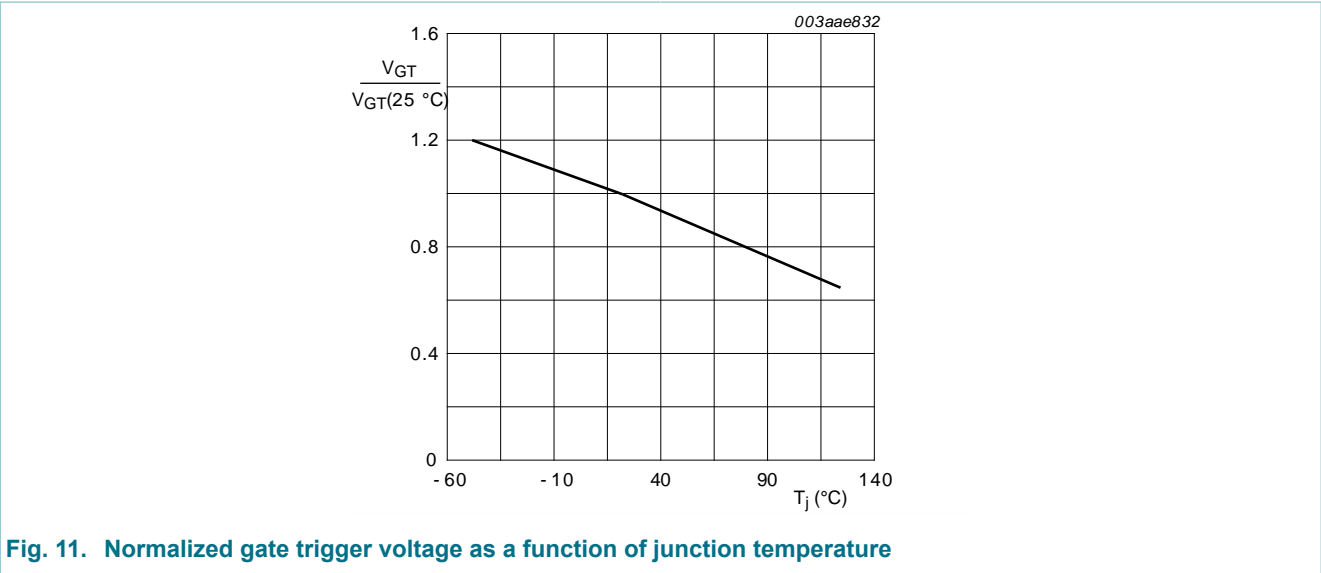
Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	-	2	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	-	2.5	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	-	2.5	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7	-	5	10	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8	-	1.6	10	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8	-	4.5	15	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8	-	1.2	10	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8	-	2.2	15	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9	-	1.2	10	mA
V _T	on-state voltage	I _T = 5 A; T _j = 25 °C; Fig. 10	-	1.4	1.7	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.25	0.4	-	V
I _D	off-state current	V _D = 600 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 125 °C; R _{GT1} = 1 kΩ; (V _{DM} = 67% of V _{DRM}); exponential waveform	-	5	-	V/μs
t _{gt}	gate-controlled turn-on time	I _{TM} = 6 A; V _D = 600 V; I _G = 0.1 A; dI _G /dt = 5 A/μs	-	2	-	μs





10. Package outline

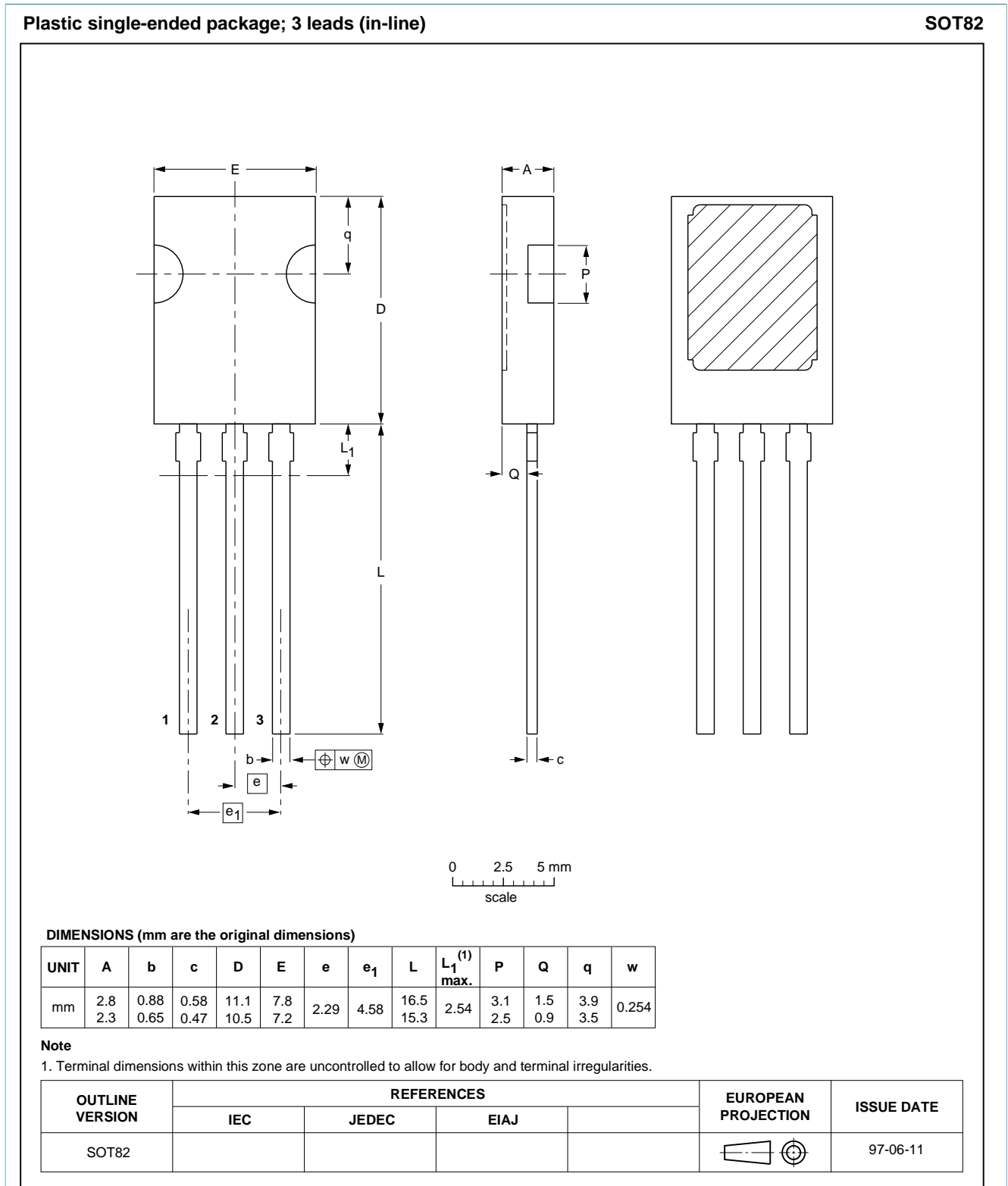


Fig. 12. Package outline SIP3 (SOT82)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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